

## Low-Power And Area-Efficient Shift Register Using Digital Pulsed Latches



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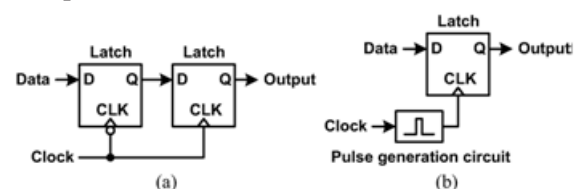
### ABSTRACT:

This paper proposes a low-power and area-efficient shift register using digital pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using a 0.18 $\mu$ m CMOS process with VDD = 1.8V. The core area is 6600 $\mu$ m<sup>2</sup>. The power consumption is 1.2mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops. In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the “data” input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the “bit array” stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input. More generally, a shift register may be multidimensional, such that its “data in” and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

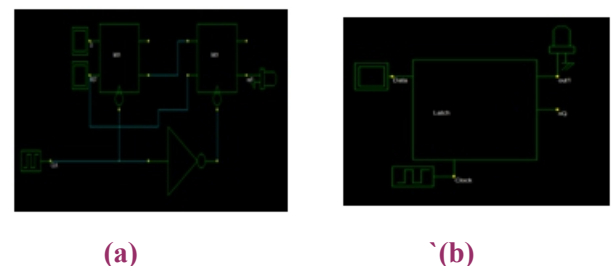
### 2.SHIFT REGISTERS:

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs.

An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop [6]–[9]. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.



**Figure 2: (a) Master-slave flip-flop. (b) Pulsed latch.**



**Figure 2.1: Schematic diagrams of (a) master-slave flip flop. (b) Pulsed latch.**

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Shift registers can have both parallel and serial inputs and outputs.

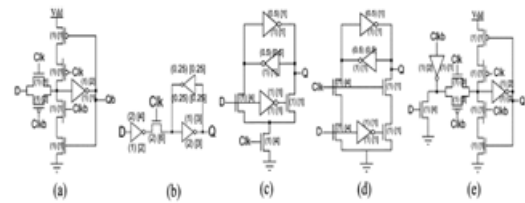
These are often configured as ‘serial-in, parallel-out’ (SIPO) or as ‘parallel-in, serial-out’ (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also ‘bi-directional’ shift registers which allow shifting in both directions:  $L \rightarrow R$  or  $R \rightarrow L$ . The serial input and last output of a shift register can also be connected to create a ‘circular shift register’. Previous work often measured energy consumption using a limited set of data patterns with the clock switching every cycle.

But real designs have a wide variation in clock and data activity across different TE instances. For example, low-power microprocessors make extensive use of clock gating resulting in many TEs whose energy consumption is dominated by input data transitions rather than clock transitions. Other TEs, in contrast, have negligible data input activity but are clocked every cycle. Shift registers, like counters, are a form of sequential logic. Sequential logic, unlike combinational logic is not only affected by the present inputs, but also, by the prior history. In other words, sequential logic remembers past events.

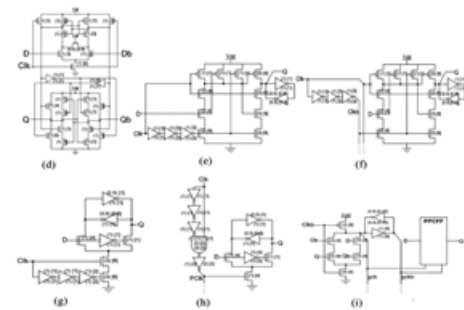
Pulsed latch structures employ an edge-triggered pulse generator to provide a short transparency window. Compared to master-slave flip-flops, pulsed latches have the advantages of requiring only one latch stage per clock cycle and of allowing time-borrowing across cycle boundaries. The major disadvantages of pulsed latch structures are the increased susceptibility to timing hazards and the energy dissipation of the local clock pulse generators.

Pulse generators can be shared among a few latch cells to reduce energy, if care is taken that the pulse shape does not degrade due to wire delay, signal coupling and noise. We measured designs both with individual pulse generators and with pulse generators shared among four latch bits, in which case we divide the pulse generator energy among the four latch instances.

HLFF [see Fig. 2(e)] operates as a pulsed transparent latch and is regarded as one of the fastest known flip-flop designs. HLFF with a shared inverter chain. SSAPL [see Fig. 2(g)] is a pulsed version of SSALA with individual pulse generators, while SSASPL [see Fig. 2(h)] has a shared pulse generator. Note that the two series transistors in SSAPL are replaced by a single transistor in SSASPL.



**Figure 2.2 High-enabled latch designs. Transistor sizes are shown for a low-power design (in parentheses: ( )) and a high-speed design (in brackets: [ ]). A transistor labeled with size.**



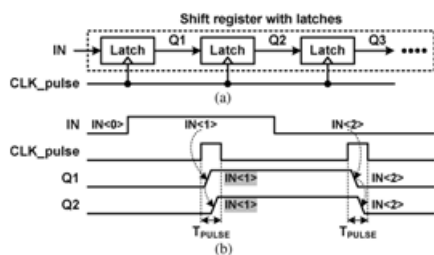
**Positive-edge-triggered flip-flop designs. Transistor sizes are labeled as in Fig. 1. (a) PPCFF. (b) SSAFF. (c) SAFF. (d) MSAFF. (e) HLFF. (f) HLSFF.**

(g) SSAPL. (h) SSASPL. (i) CCPPCFF. Traditionally, the power consumption of flip-flop and latch designs has been measured using an ungated clock and a small number of input activation patterns. Instead, we adopt a more accurate methodology in which all possible states (e.g., clock value, input value, output value) of the TE are enumerated and the energy consumption of each state transition is measured. Some designs perform extremely well in certain regimes, but extremely poorly in others. For example, in test2 the low power SSAFF design uses eight times less energy than the HLFF structure, but in test 3 it uses seven times more energy. Another good example of a TE specialized for an operating regime is CPNLA. This latch design is by far the best choice for test 3, but by far the worst choice in all other cases. Finally, CCPPCFF [see Fig. 2(i)] is a conditional clocking flip-flop based on the design presented in, which in turn is an improvement. The goal of this design is to reduce energy when the input data does not change by gating the clock within the flip-flop.

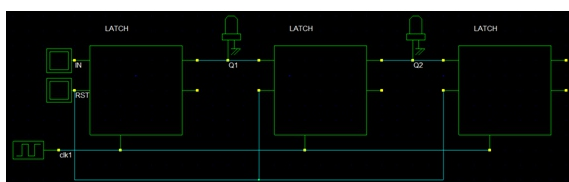
### 3. Proposed Shift Register

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6].

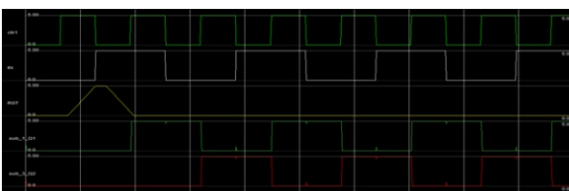
The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2.1(a) consists of several latches and a pulsed clock signal (CLK\_pulse). The operation waveforms in Fig show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 2.2(a). The output signal of the latch is delayed (TDELAYED) and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width (TPULSE), but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.



**Figure 3.1: Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.**



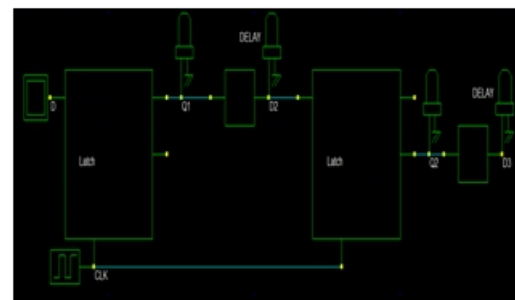
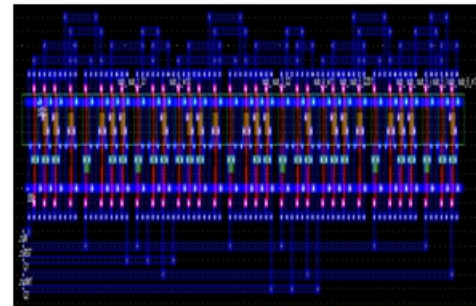
**(a)**



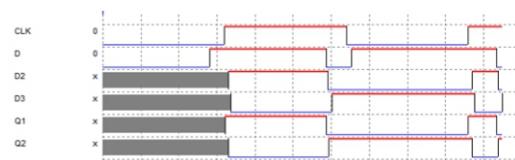
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**Figure 3.1.1: (a) Schematic. (b) Layout.**

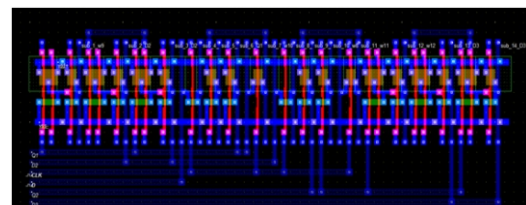
### 3.2 Shift register with latches, delay circuits, and a pulsed clock signal



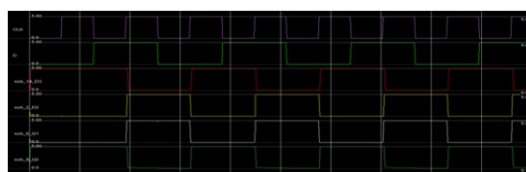
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**(c)**



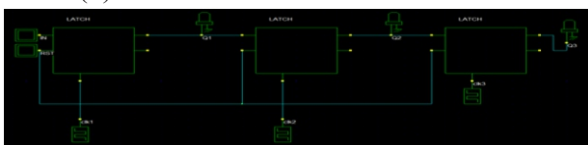
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**Figure 3.2.1: (a) Schematic. (b) Timing diagram. (c) Layout. (d) Simulation waveforms.**

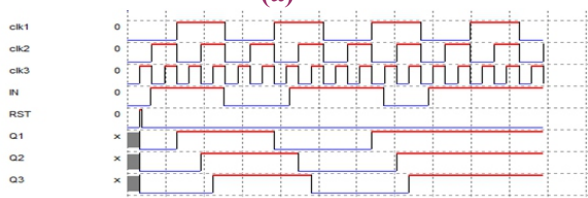


### 3.3: Shift register with latches and delayed digital pulsed clock signals Schematic Wave-forms

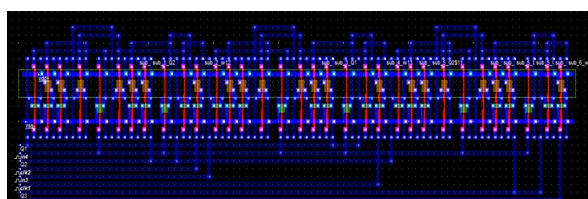
Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 3.3(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. Figure 3.4 shows an example of the proposed shift register. The proposed shift register is divided into  $M$  sub shift registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shift register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK\_pulse1:4 and CLK\_pulseT). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 2.4(b) shows the operation waveforms in the proposed shift register. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 2.5. Figure 3.4: Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.



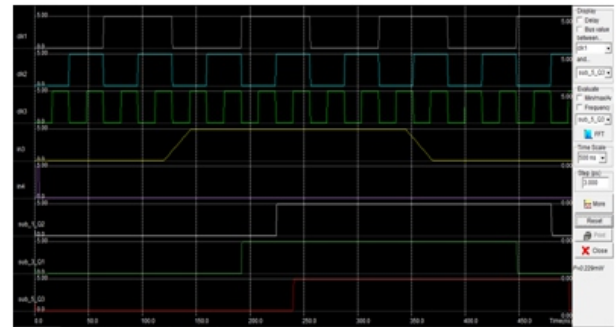
(a)



(b)



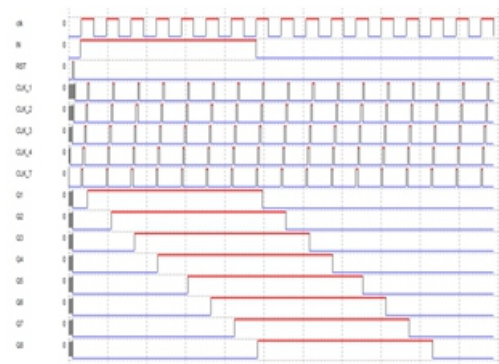
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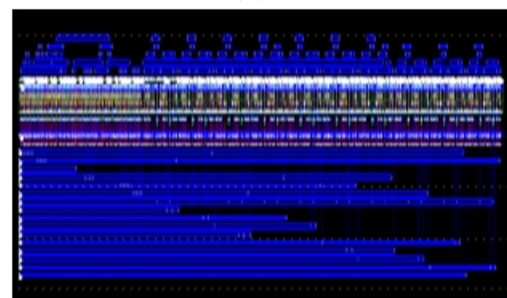
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Figure 3.4.1: (a) Schematic. (b) Timing diagram. (c) Layout. (d) Simulation waveforms.

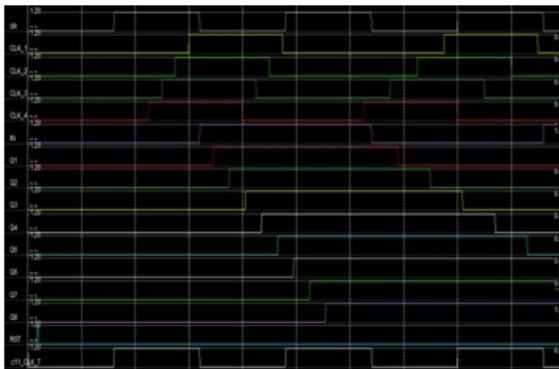
The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in Fig. 2.5 each pulsed clock signal is generated in a clock-pulse circuit consisting of a delay circuit and an AND gate. When an  $N$ -bit shift register is divided into  $K$ -bit sub shift registers, the number of clock-pulse circuits is  $K+1$  and the number of latches is  $N + (N/K)$ . A  $K$ -bit sub shift register consisting of  $K+1$  latches requires  $K+1$  pulsed clock signals.



(b)



(c)



(d)

Figure 3.5 (a) Schematic. (b) Timing diagram. (c) Layout. (d) Simulation waveforms.

An integer  $K$  for the minimum power is selected as a divisor of  $N$ , which is nearest to  $\sqrt{N/\alpha P}$ . In  $K$  selection, the clock buffers in Fig. 2.5 are not considered. The total size of the clock buffers is determined by the total clock loading of latches. Although the number of latches increases from  $N$  to  $N(1+1/K)$ , the increment ratio of the clock buffers is small. The number of clock buffers is  $K$ . As  $K$  increases, the size of a clock buffer decreases in proportion to  $1/K$  because the number of latches connected to a clock buffer ( $M=N/K$ ) is proportional to  $1/K$ . Therefore, the total size of the clock buffers increases slightly with increasing and the effect of the clock buffers can be neglected for choosing  $K$ . The maximum number of  $K$  is limited to the target clock frequency. As shown in Fig. 2.6 the minimum clock cycle time ( $T_{CLK\_MIN}$ ) is  $T_{CP} + K \cdot T_{DELAY} + T_{CQ}$ , where  $T_{CP}$  is the delay from the rising edge of the main clock signal ( $CLK$ ) to the rising edge of the first pulsed clock signal ( $CLK\_pulse1$ ),  $T_{DELAY}$  is the delay of two neighbor pulsed clock signals,  $T_{CQ}$  is the delay from the rising edge of the last pulsed clock signal ( $CLK\_pulse1$ ) to the output signal of the latch  $Q1$ .  $T_{CLK\_MIN}$  is proportional to  $K$ . As  $K$  increases, the maximum clock frequency ( $f_{CLK\_MAX} = 1/T_{CLK\_MIN}$ ) decreases in proportion to  $1/K$ . Therefore,  $K$  must be selected under the maximum number which is determined by the maximum clock frequency of the target applications.

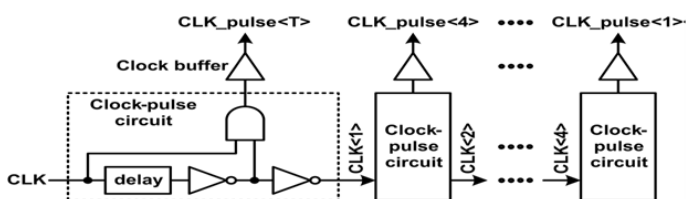
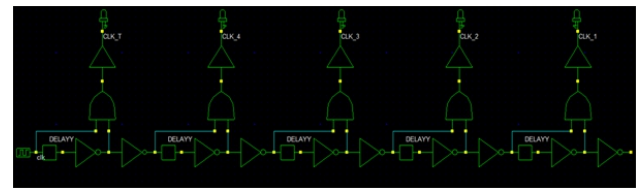
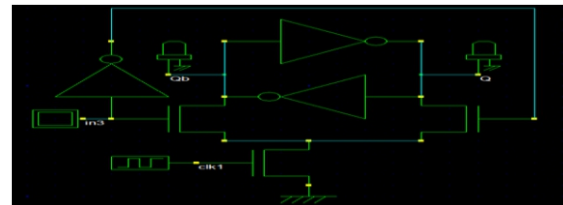


Figure 3.6: Delayed pulsed clock generator.



The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flops. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig. 2.7, which is the smallest latch, is selected.



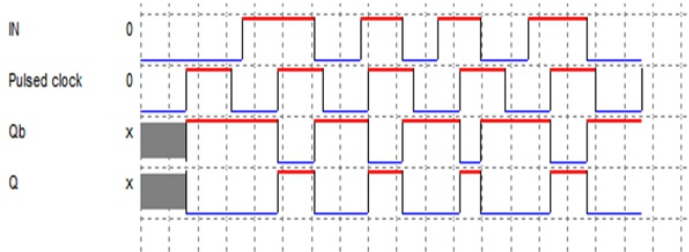
### Schematic of the SSASPL:

The original SSASPL with 9 transistors [6] is modified to the SSASPL with 7 transistors in Fig.2.7 by removing an inverter to generate the complementary data input ( $Db$ ) from the data input ( $D$ ). In the proposed shift register, the differential data inputs ( $D$  and  $Db$ ) of the latch come from the differential data outputs ( $Q$  and  $Qb$ ) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal.

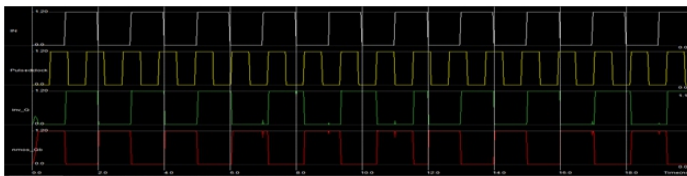
The SSASPL was implemented and simulated with a  $0.18\mu m$  CMOS process at  $V_{DD}=1.8V$ . The sizes ( $W/L$ ) of the three NMOS transistors ( $M1-M3$ ) are  $1\mu m/0.18\mu m$ . The sizes of the NMOS and PMOS transistors in the two inverters are all  $0.5\mu m/0.18\mu m$ . The minimum clock pulse width of the SSASPL to update the data is 62 ps at a typical process simulation (TT) and 54–76 ps at all process corner simulations (FF-SS).

The rising and falling times of the clock pulse are approximately 100 ps. The clock pulse shape can be degraded due to the wire delay, signal coupling, and supply noise. The clock pulse width (TPULSE) of 170 ps was selected by adding the timing margin to the minimum clock pulse width at the slowest simulation case.

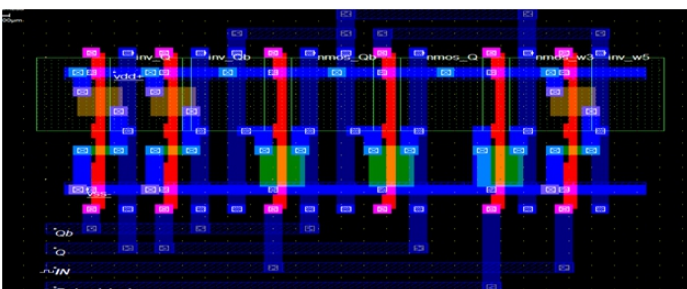
### Simulation waveforms of a shift register with the SSASPLs driven by delayed pulsed clock signals.



### Timing Diagram.



### Simulation Waveforms.



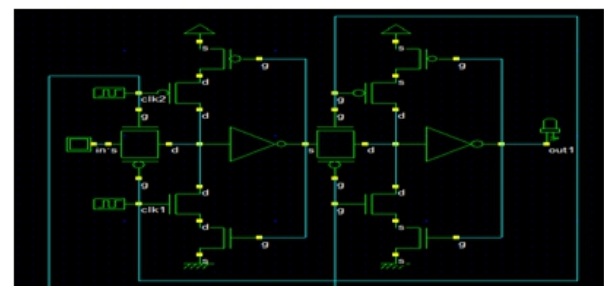
### Layout of the SSASPL.

Fig. 4.4 shows the layout of the SSASPL. Its area is  $19.2\mu\text{m}^2$ . The SSASPL consumes  $3.3\mu\text{W}$  at  $f_{\text{CLK}}=100\text{MHz}$ . The power is consumed in the clock loading and data path of the latch. The clock loading of an NMOS transistor (M1) consumes  $0.73\mu\text{W}$ . The data path consumes  $2.57\mu\text{W}$  when the data transition ratio is 0.5 and the output loading of the latch is only two NMOS transistors (M2) and (M3) of the next latch in the shift register. Each clock-pulse circuit occupies  $49.5\mu\text{m}^2$  and consumes  $27.6\mu\text{W}$  at  $f_{\text{CLK}}=100\text{MHz}$ . The word length of the sub shift register (K) in a 256-bit shift Register ( $N=256$ ) is selected by considering the area, power, speed. When considering the area optimization, the clock-pulse circuit without the clock buffer is 2.58 times larger than a latch ( $\alpha=2.58$ ). The optimal K is 8 which is a divisor of ( $N=256$ ) nearest to  $9.96(=\sqrt{N/\alpha}=\sqrt{256/2.58})$ . When considering the power optimization, the clock-pulse circuit consumes 8.35 times larger power than a latch ( $\alpha=8.35$ ).

The optimal K is 4 which is a divisor of  $N(=256)$  nearest to  $5.54(=\sqrt{N/\alpha}=\sqrt{256/8.35})$ . When considering the speed, the maximum clock frequency is limited to the minimum clock cycle time ( $\text{TCLK\_MIN} = \text{TCP} + \text{K} \cdot \text{TDELAY} + \text{TCQ}$ ). In the simulation,  $\text{TCP} = 180\text{ps}$ ,  $\text{TDELAY} = 220\text{ps}$ ,  $\text{TCQ} = 130\text{ps}$ . When  $K=4$  and  $K=8$ , the maximum operating frequencies are 840 MHz and 483 MHz for 5 and 9 pulsed clock delays, respectively.

### PERFORMANCE COMPARISON:

Table 5.1 shows the transistor comparison of pulsed latches and flip-flops. The transmission gate pulsed latch (TGPL) [7], hybrid latch flip-flop (HLFF) [8], conditional push-pull pulsed latch (CP3L) [9], Power-PC-style flip-flop (PPCFF) [10], Strong-ARM flip-flop (SAFF) [11], data mapping flip-flop (DMFF) [12], conditional pre-charge sense-amplifier flip-flop (CPSAFF) [13], conditional capture flip-flop (CCFF) [14], adaptive-coupling flip-flop (ACFF) [15] are compared with the SSASPL [6] used in the proposed shift-register. Fig. 5.12 shows the schematic of the PPCFF, which is a typical master-slave flip-flop, composed of two latches. The PPCFF consists of 16 transistors and has 8 transistors driven by clock signals. For a fair comparison, it uses the minimum size of transistors. The sizes of NMOS and PMOS transistors are  $0.5\mu\text{m}/0.18\mu\text{m}$  and  $1\mu\text{m}/0.18\mu\text{m}$  respectively. Its layout was drawn compactly by sharing all possible sources and drains of transistors. All circuits were implemented with a  $0.18\mu\text{m}$  CMOS process. The powers were measured at  $\text{VDD}=1.8\text{V}$  and  $f_{\text{CLK}}=100\text{MHz}$ .



(b)

Schematic of the PPCFF

### TRANSISTOR COMPARISON OF PULSED LATCHES AND FLIP-FLOPS



		Total number of transistors	Number of transistors connected to clock
Pulsed latch	SSASPL [6]	7	1
	TGPL [7]	10	4
	HLFF [8]	14	2
	CP3L [9]	26	6
Flip-flip	PPCFF [10]	16	8
	SAFF [11]	18	3
	DMFF [12]	22	5
	CPSA [13]	28	5
	CCFF [14]	28	5
	ACFF [15]	22	4

### PERFORMANCE COMPARISONS OF THE PPCFF AND SSASPL

**Table :PERFORMANCE COMPARISONS OF THE PPCFF AND SSASPL**

Type		PPCFF	SSASPL
Number of transistors	Total	16	7
	Clock	8	1
Area		37.5 $\mu\text{m}^2$ (6.7 $\mu\text{m} \times 5.6\mu\text{m}$ )	19.2 $\mu\text{m}^2$ (8.0 $\mu\text{m} \times 2.4\mu\text{m}$ ) (51.2%)
Power [ $\mu\text{W}$ ] @ $f_{\text{CLK}}=100\text{MHz}$	Total	8.29	3.30 (39.8%)
	Data path	3.87	2.57 (66.5%)
	Clock load	4.42	0.73 (16.5%)
Min. clock pulse width [ps]		-	62 @ TT 54-76 @ FF-SS
Clock pulse width ( $T_{\text{PULSE}}$ ) [ps]		-	170
Clock pulse interval [ps]		-	50
Pulsed clock delay ( $T_{\text{DELAY}}$ ) [ps]		-	220
Sizes of transistors (W/L) [ $\mu\text{m}/\mu\text{m}$ ]		NMOS=0.5/0.18 PMOS=1/0.18	M <sub>1</sub> -M <sub>3</sub> =1/0.18 NMOS=0.5/1.8 PMOS=0.5/1.8 in inverters

The total area of the N flip-flops and clock buffer for the N-bit conventional shift register is  $N \cdot \alpha$ , where  $\alpha$  is the total area of a flip-flop and a unit clock buffer for driving a flip-flop. The total area of  $N(1+1/K)$  latches and a clock buffer for the N-bit proposed shift register is  $N(1+1/K) \cdot \beta$ , where  $\beta$  is the total area of a latch and a unit clock buffer for driving a latch. The area of  $(K+1)$  clock-pulse circuits is  $(K+1) \cdot \gamma$ , where  $\gamma$  is the area of a clock-pulse circuit.

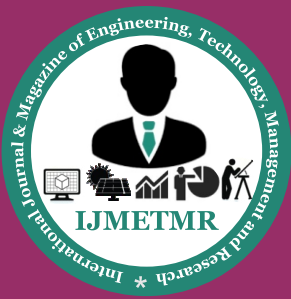
### CONCLUSION:

This paper proposed a low-power and area-efficient shift register using digital pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal.

A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register was fabricated using a 0.18 $\mu\text{m}$  CMOS process with  $V_{\text{DD}}=1.8\text{V}$ . Its core area is 6600 $\mu\text{m}^2$ . It consumes 1.2 mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops.

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