ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design Considerations of a Fault Current Limiting Dynamic Voltage Restorer (FCL-DVR)

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ABSTRACT

This paper proposes a new fault current limiting dynamic voltage restorer (FCL-DVR) concept. The new topology uses a crowbar bidirectional thyristor switch across the output terminals of a conventional back-to-back DVR. In the event of a load short, the DVR controller will deactivate the faulty phase of the DVR and activate its crowbar thyristor to insert the DVR filter reactor into the grid to limit the fault current. A fault condition is detected by sensing the load current and its rate of change. The FCL-DVR will operate with different protection strategies under different fault conditions. Design of the FCL-DVR involves selecting important parameters, such as DVR power rating, dc link voltage of the DVR, output filter reactors and capacitors, and grid-tied transformers is proposed. The design methodology of the proposed FCL-DVR is fully discussed based on power systems computer aided design (PSCAD)/electromagnetic transients including dc (EMTDC) simulation. A scaled-down experimental verification is also carried out. Both modeling and experimental results confirm the effectiveness of the new FCL-DVR concept for performing both voltage compensation and fault current limiting functions.

Keywords: ***Dynamic voltage restorer (DVR), fault current limiting (FCL), parameter design method, voltage compensation.***

INTRODUCTION

There are two major challenges that the modern power grid must deal with: voltage fluctuations and short circuit faults. With wide use of nonlinear loads, the grid suffers from voltage fluctuation, voltage unbalance, and other power quality problems. At the same time, many power loads become more sensitive to these disturbances. The rapid proliferation of renewable power generation sources in the grid has aggravated these power quality problems.

Furthermore, short-circuit faults remain one of the most common faults in the grid and cause great concerns for grid security and stability. A solid-state fault current limiter (FCL) can be used to limit fault currents in the grid. When a short-circuit fault occurs, the solid-state FCL inserts a high series impedance in the power loop and thus effectively limits the fault current. However, during normal operation of the grid the FCL operate in a no-load mode, resulting in compromised energy conversion efficiency and equipment utilization efficiency. On the other hand, a dynamic voltage restorer (DVR) can be used to compensate for the fluctuations of the grid voltage. For many power systems, it would be tremendously advantageous to provide both voltage compensation and fault current limiting functions by a single power electronic apparatus.

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In the control strategy of a conventional DVR is expanded to offer additional fault current interruption features. However, this approach requires a three-fold increase in power rating of the DVR, leading to a sharp increase in system cost. In this paper, a new concept of fault current limiting dynamic voltage restorer (FCL-DVR) is proposed. The new topology can operate in two operational modes: 1) compensation mode for voltage fluctuation and unbalance; and 2) fault current limiting mode. It should be noted that only one additional crowbar bidirectional thyristor switch is added across the output terminals of each phase of the conventional DVR, greatly simplifying its implementation. Furthermore, the new FCL-DVR can maintain the same power rating as the conventional DVR without FCL function.

This paper is organized as the following. In Section II, the topology, principle and the control strategy are proposed. In Section III, the design methodology of important system parameters of FCL-DVR is discussed. In Section IV, the FCL-DVR is validated by simulation and experimental results.

TOPOLOGY AND PRINCIPLE OF OPERATION

Topology:

The topology of the FCL-DVR is shown in Fig. 1. It is composed of three single phase bridges. Each single phase topology mainly comprises of a shunt transformer, a backto-back power converter, a series transformer, and a crowbar bidirectional thyristor. The input rectifier module of the backto-back converter is connected to the grid through a shunt transformer (e.g., T1) with Lz to eliminate the high frequency ripples, and rectifies the power from the grid to the dc link capacitor.

The output inverter module converts the power from the dc link capacitor to compensate voltage fluctuation, and is connected to the grid through a series transformer (e.g., T4) and a LC output filter. The input rectifier module and output inverter module are connected through the dc link capacitor Cd.

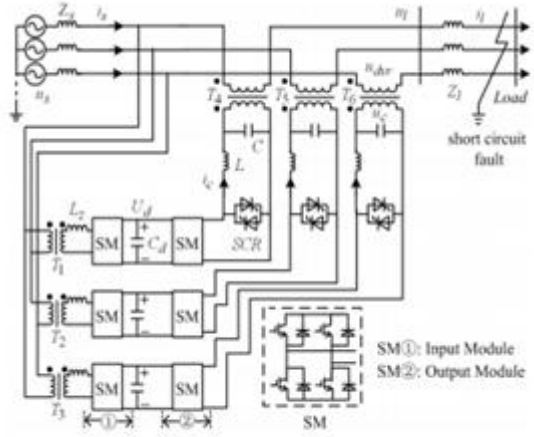

Fig. 1. Topology of FCL-DVR.

The crowbar bidirectional thyristor in each phase is across the output terminals of the output inverter module to provide short circuit fault current limiting function. us, udc, uc, uDVR, and ul represent the supply voltage, the dc link voltage, the output voltage of the FCL-DVR, the output voltage of FCL-DVR on the primary side of the series transformer, and the voltage of point of common coupling (PCC), respectively. is represents the supply current, and il is the load current. Zs and Zl are the equivalent impedances of the grid and the transmission line, respectively. As shown in Fig. 1, the major difference between the new FCL-DVR and a conventional DVR is the addition of three crowbar bidirectional thyristors.

The crowbar bidirectional thyristor for each phase will be deactivated or activated depending on the operation conditions. When the grid is under normal operation, the crowbar bidirectional thyristor is deactivated and the FCL-DVR operates in the voltage compensation mode to compensate voltage fluctuations. When a short circuit fault occurs, the crowbar bidirectional thyristor is activated to insert the output inductor into the main current path through the series transformer.

At the same time, the insulated gate bipolar transistors (IGBTs) of the pulse width modulation (PWM) inverter will be turned off to completely deactivate the inverter. The FCL-DVR thus operates in the fault current limiting mode. The short circuit fault current

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International Journal & Magazine of Engineering, Technology, Management and Research
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can be limited by L through the crowbar bidirectional thyristor. The maximum fault current can also be controlled by adjusting the conduction-angle of the thyristor. Therefore, both voltage compensation and fault current limiting functions can be provided by the FCL-DVR with the same power rating of a conventional DVR.

When a short circuit fault or a voltage sag situation occurs, the fluctuation of supply voltage will influence the stability of dc link voltage. If the three shunt transformers are delta connected on the high-voltage side, the voltage fluctuation on the low-voltage side is smaller than the Y-connection mode. Meanwhile, delta-connection can also suppress the 3rd harmonics caused by the fluctuation of dc link voltage. So in this paper, the high-voltage sides of the shunt transformers are delta-connected.

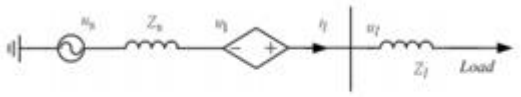

Fig. 2. Single-phase equivalent circuit of FCL-DVR when it operates in voltage compensation mode.

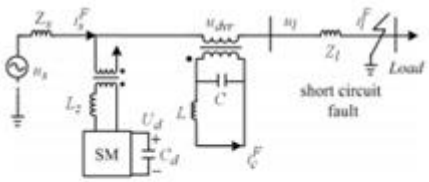

Fig. 3. Single-phase equivalent circuit of FCL-DVR when it operates in fault current limiting mode.

Principle of Operation

1) Voltage Compensation Mode: When FCL-DVR operates in the voltage compensation mode, the crowbar bidirectional thyristor is deactivated. The FCL-DVR operates as a conventional DVR, so it can be equivalent to a voltage controlled voltage source, as shown in Fig. 2. When voltage fluctuation or unbalance occurs, FCL-DVR can be controlled as a compensation voltage u1, which is in series with the supply voltage. So the load voltage can be maintained, and the power quality can be improved. The input module of back-to-back converter is used to supply the dc link voltage.

2) Fault Current Limiting Mode: When the FCL-DVR operates in the fault current limiting mode, the single-phase equivalent circuit of FCL-DVR is shown in Fig. 3. When a short circuit fault happens, the faulty phase of the inverter is deactivated, and the crowbar bidirectional thyristor is activated. Under this condition, the reactor L is inserted into the grid on the secondary side of the series transformer, so the fault current can be limited by the reactor. As the supply voltage almost sustained by the series transformer, the input rectifier module of the back-to-back converter can operate normally, making the FCL-DVR easy to recover after the fault condition is removed.

As shown in Fig. 3, in order to eliminate high frequency ripples the L and C are usually resonant at a high frequency, then $n2\omega 0L = 1/\omega 0C$. Where $\omega 0$ is the fundamental frequency, and n is usually greater than 10. Compared with the equivalent impedance of C, the equivalent impedance of L is very small. So the impact of filter capacitance can be neglected. The equivalent impedance of the secondary side of the series transformer is given by

$$Zeq2 = \omega 0L * \pi\, 2\pi - 2\alpha + \sin 2\alpha \quad (1)$$

where α is the trigger delay angle of the crowbar thyristors. The equivalent impedance of L on the primary side is

$$Zeq = k2Zeq2 \quad (2)$$

where k is the ratio of series transformer.

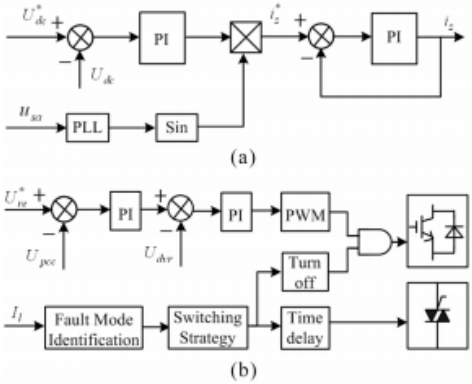

Fig. 4. Control block diagram of the FCL-DVR. Control block diagram of (a) rectifier to maintain the dc link voltage and (b) inverter and crowbar bidirectional thyristor.

When the FCL-DVR operates in the fault current limiting mode, the supply current is given by

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$$I_s^F \approx I_c^F/k \approx I_l^F \approx \frac{U_s}{Z_s + Z_{eq} + Z_l}. \quad (3)$$

From (3), it can be seen that the short circuit current can be limited by the output reactor. As Zs and Zl are usually smaller than Zeq, fault current is mainly limited by Zeq. The fault current can be limited to the reference value by selecting the parameters of k, L, and adjusting the conduction-angle of the crowbar bidirectional thyristor.

SIMULATION AND EXPERIMENTAL RESULTS

Simulation Case Study

Power system computer aided design (PSCAD)/electromagnetic transients including dc (EMTDC) simulation is carried out to verify the validity of the proposed topology and design methodology. The supply voltage is set at 10 kV with a 1 MW resistive load. The FCL-DVR is designed to compensate a voltage fluctuation of 20% of the supply voltage. The maximum fault current is allowed to be six times of the nominal load current. The parameters are summarized in Table.

Voltage Compensation Function of FCL-DVR

Fig.(a) and (b) shows the voltage compensation performance of the FCL-DVR for voltage fluctuation and unbalance, respectively. Us, UL, IL, Udc, and UDVR are the supply voltage, load voltage at the point of common coupling (PCC), the load current, the dc link voltage, the output voltage of FCL-DVR in the primary side of the inverter. As shown in Fig. 9(a), voltage sag happens between 0.5 and 0.6 s with a depth of 20%. When the FCL-DVR is put into operation at 0.5 s, the inverter of the FCL-DVR output a compensation voltage UDVR within one cycle (of 50 Hz) by absorbing active power from the rectifier through the dc link capacitor. The load voltage at the point of common coupling UL can be maintained without interruption. So the load can operate normally with little influence by the supply voltage sag. In the process of voltage compensation, the proposed

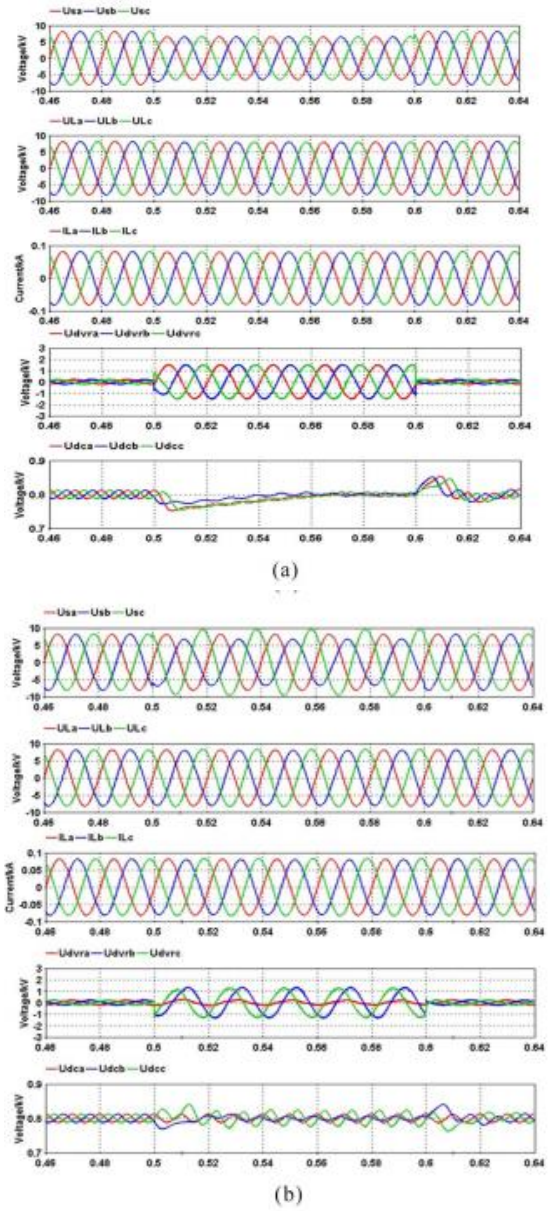

Fig. Simulation results of voltage compensation operation of FCL-DVR. Waveforms of grid voltages, PCC voltages, load currents, FCL-DVR output voltages, and dc link voltages of the FCL-DVR during (a) voltage fluctuation event and (b) unbalanced voltage event.

Control method could limit the fluctuation of dc link voltage to less than 6%. In Fig. (b), three phase unbalance occurs between 0.5 and 0.6 s. The voltage of phase-A is not changed; the voltage of phase-B drops 1 kV; the voltage of phase-C rise 1 kV; and

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phase angle keeps invariant. The FCL-DVR put into operation at 0.5 s. As the FCL-DVR can be operated at phase-splitting compensation mode, the three phase inverter of FCL-DVR can output unbalance voltage to compensate the supply voltage. When the FCL-DVR is adopted, UL almost keep unchanged, and the dc link voltage has a fluctuation when power grid voltage swells or sags, but soon will be able to stabilize around 800 V.

CONCLUSION

A new FCL-DVR concept is proposed to deal with both voltage fluctuation and short current faults. The new topology uses a crowbar bidirectional thyristor switch across the output terminals of a conventional back-to-back DVR. In the event of load short, the DVR controller will deactivate the faulty phase of the DVR and activate its crowbar thyristor to insert the DVR filter reactor into the grid to limit the fault current. The FCL-DVR will operate with different protection strategies under different fault conditions.

Based on theoretical analysis, PSCAD/EMTDC simulation and experimental study, we conclude the following.

1) With the crowbar bidirectional thyristor across the output terminal of the inverter, the proposed FCL-DVR can compensate voltage fluctuation and limit fault current.

2) The FCL-DVR can be used to deal with different types of short faults with minimum influence on nonfault phases. The FCL-DVR has the same power rating as a conventional DVR.

3) The delta-connection mode of the shunt transformers minimizes the influence of dc link voltage fluctuations and suppresses the 3rd harmonics.

4) The proposed control method can detect faults within two cycles.

5) The design methodology based on the analysis of the relationship between main circuit parameters and compensation capacity could be helpful to the design of FCL-DVR.

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