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Realization of BIST Architecture Using SRAM Cells Based on Input Vector Monitoring

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ABSTRACT:
Built in Self test (BIST) strategies constitute a class of plans that give the ability of performing at-speed testing with high blame scope, while at the same time they unwind the dependence on costly outside testing hardware. Input vector checking simultaneous implicit individual test (BIST) plans perform testing amid the typical operation of the circuit without forcing a need to set the circuit disconnected to play out the test. These plans are assessed in view of the equipment overhead and the simultaneous test idleness (CTL), i.e., the time required for the test to finish, though the circuit works regularly. In this brief, we introduce a novel information vector checking simultaneous BIST plot, which depends on observing a set (called window) of vectors achieving the circuit contributions amid typical operation, and the utilization of a static-RAM like structure to store the relative areas of the vectors that achieve the circuit contributions to the inspected window; the proposed plan is appeared to perform altogether superior to beforehand proposed plans concerning the equipment overhead and CTL exchange off.

I. INTRODUCTION:
Built in self test(BIST) systems constitute a class of plans that give the ability of performing at-speed testing with high blame coverage, whereas at the same time they unwind the dependence on costly outside testing hardware. Hence, they constitute an appealing answer for the issue of testing VLSI gadgets [1].BIST methods are ordinarily ordered into disconnected and online.

Offline designs work in either ordinary mode(during which the BIST hardware is idle)or test mode. During test mode, the inputs produced by a test generator module are connected to the contributions of the circuit under test(CUT) and the reactions are caught into a reaction verifier(RV).Therefore, to play out the test, the typical operation of the CUT is slowed down and, consequently, the execution of the framework in which the circuit is included, is debased.

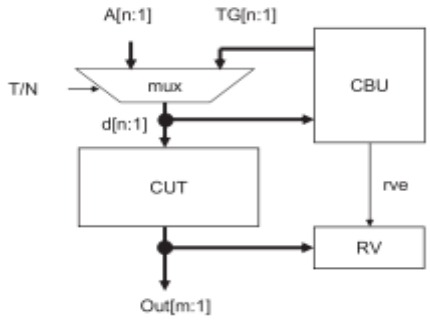

Fig. 1. Input vector monitoring concurrent BIST

II. EXISTING SYSTEM:
Input vector checking simultaneous BIST systems [2]–[10] have been proposed to maintain a strategic distance from this execution corruption. These structures test the CUT simultaneously with its typical operation by abusing input vectors appearing to the contributions of the CUT; if the approaching vector has a place with a set called dynamic test set, the RV is empowered to catch the CUT reaction. The square graph of an info vector checking simultaneous BIST design is appeared in Fig. 1. The CUT has n sources of info and m yields and is tried thoroughly; consequently, the test set size is N = 2n.

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The procedure can work in either ordinary or test mode, contingent upon the estimation of the flag named T/N. Amid ordinary mode, the vector that drives the contributions of the CUT (meant by d[n:1] in Fig. 1) is driven from the ordinary info vector (A[n:1]). An is likewise headed to a simultaneous BIST unit (CBU), where it is contrasted and the dynamic test set. In the event that it is found that A matches one of the vectors in the dynamic test set, we say that a hit has happened. For this situation, An is expelled from the dynamic test set and the flag reaction verifier empower (rve) is issued, to empower the m-arrange RV to catch the CUT reaction to the information vector [1]. At the point when all information vectors have performed hit, the substance of RV are inspected. Amid test mode, the contributions to the CUT are driven from the CBU yields signified TG[n:1]. The simultaneous test inactivity (CTL) of an information vector checking plan is the interim (included either number of clock cycles or time units) required to finish the test while the CUT works in typical mode.

III. PROPOSED SCHEME:

Give us a chance to consider a combinational CUT with n input lines, as appeared in Fig. 2; thus the conceivable information vectors for this CUT are 2n. The proposed plan depends on observing a window of vectors, whose size is W, with W = 2w, where w is a whole number w<n. Every minute, the test vectors having a place with the window are monitored, and if a vector plays out a hit,the RV is empowered. The bits of the info vector are isolated into two particular sets involving w and k bits, separately, with the end goal that w+k=n. The k(high order)bits of the information vectors how whether the information vector has a place with the window under thought. The remaining bits demonstrate the relative area of the incoming vector in the present window. In the event that the approaching vector has a place with the current window and has not been gotten amid the examination of the present window, we say that the vector has played out a hit and the RV is timed to catch the CUT's reaction to the vector. When all vectors that have a place with the present window have achieved the CUT inputs, we continue to look at the following window. The module executing the thought is appeared in Fig.2. It works in one out of two modes, ordinary, and test, contingent upon the estimation of the flag T/N. Whenever T/N = 0 (ordinary mode) the contributions to the CUT are driven by the typical info vector. The contributions of the CUT are likewise headed to the CBU as takes after: the k (high request) bits are headed to the contributions of a k-organize comparator ;alternate contributions of the comparator are driven by the yields of a k-arrange test generator TG.

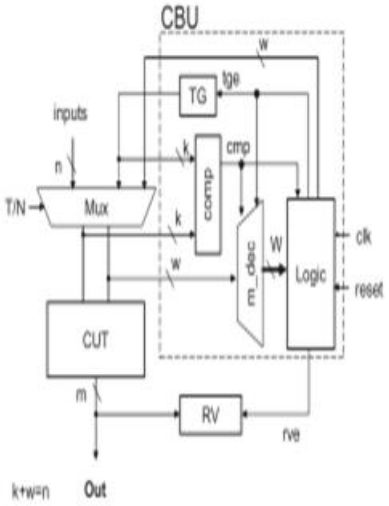

Fig. 2.Proposed Architecture

The proposed plot utilizes an altered decoder(denoted as m_dec in Fig.2) and a rationale module in light of a static-RAM (SRAM)- like cell, as will be clarified right away. The outline of the m_dec module for w=3 is appeared in Fig.3 and works as takes after. At the point when test generator enable(tge)is empowered, all yields of the decoder are equivalent to one. Whenever comparator(cmp) is disabled(and tge is not empowered) all yields are crippled. At the point when tge is crippled and cmp is empowered, the module works as a typical deciphering structure.

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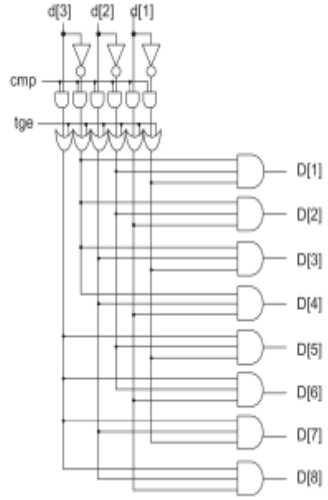

Fig.3.Modified decoder design used in the proposed architecture

The architecture of the proposed scheme[D[f] for the specific case n=5, k=2,and w=3, is shown in Fig.4.

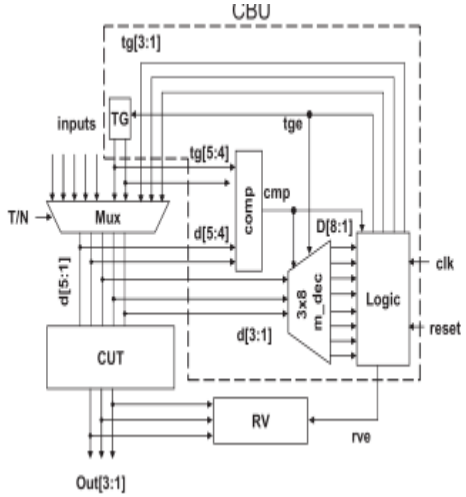

Fig.4.Proposedarchitectureforn=5,w=3,and k=2

The module marked rationale in Fig. 4 is appeared in Fig. 5. It involves W cells (working in a manner like the SRAM cell), a sense intensifier, two D flip-flops, and a w-organize counter (where w = log 2 W). The flood flag of the counter drives the tge motion through a unit flip-flounder delay. The signs clk∗ and clock (clk) are empowered amid the dynamic low and high of the clock, respectively.

In the spin-off, we have accepted a clock that is dynamic amid the second 50% of the period, as appeared in Fig. 5.

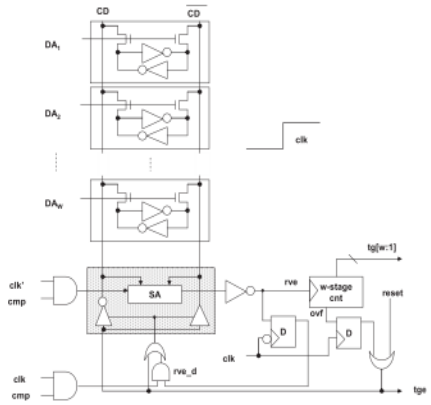

Fig.5. Design of the logic module

In the continuation, we depict the operation of the rationale module, displaying the accompanying cases: 1) reset of the module; 2) hit of a vector (i.e., a vector has a place in the dynamic window and achieves the CUT contributions interestingly); 3) a vector that has a place in the present window achieves the CUT sources of info yet not surprisingly; and 4) tge operation (i.e., all cells of the window are filled and we will continue to look at the following window).

A. Rest Of The Module:

Toward the start of the operation, the module is reset through the outside reset flag. At the point when reset is issued, the tge flag is empowered and every one of the yields of the decoder (Fig. 3) are empowered. Henceforth, DA1, DA2 , ... , DAW are one; moreover, the CD∗ flag is empowered; along these lines, a one is composed to the correct hand side of the cells and a zero an incentive to one side hand side of the cells.

B. Hit of Vector (i.e., Vector Belongs in the Active Window and Reaches the CUT Inputs surprisingly)

Amid typical mode, the contributions to the CUT are driven from the ordinary sources of info.

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The n sources of info are additionally headed to the CBU as takes after: the w low-arrange information sources are headed to the contributions of the decoder; the k high-arrange data sources are headed to the contributions of the comparator. At the point when a vector having a place with the present window achieves the contributions of the CUT, the comparator is empowered and one of the yields of the decoder is empowered. Amid the main portion of the clock cycle (clk∗ and cmp are empowered) the tended to cell is perused; in light of the fact that the read esteem is zero, the w-organize counter is activated through the NOT door with yield the reaction verifier empower (rve) flag. Amid the second 50% of the clock cycle, the left flip-slump (the one whose clock information is upset) empowers the AND entryway (whose other info is clk and cmp), and empowers the supports to compose the esteem one to the tended to cell.

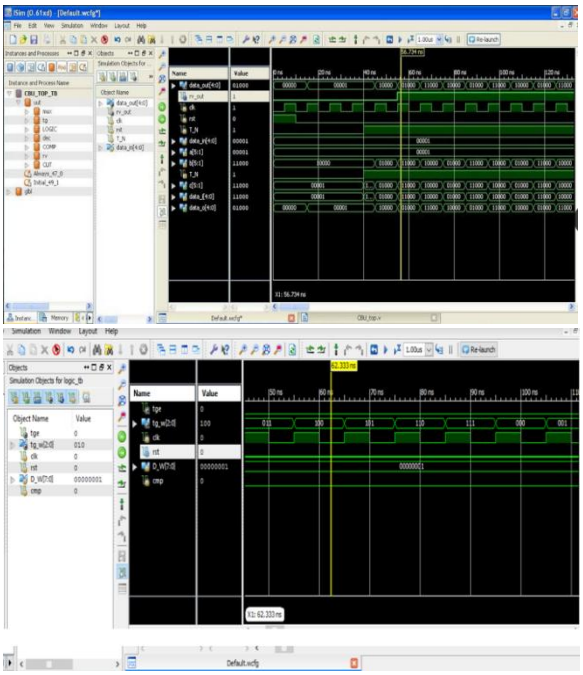
C. Vector That Belongs in the Current Window Reaches the CUT Inputs But Not For the First Time:

If the phone relating to the approaching vector contains a one (i.e., the particular vector has achieved the CUT contributions amid the examination of the present window before), the rve flag is not empowered amid the primary portion of the clock cycle; consequently, the w-organize counter is not activated and the AND door is not empowered amid the second 50% of the clock cycle.

D. tge Operation (i.e., All Cells of the Window are Filled and We Will Proceed to Examine the Next Window)

When every one of the phones are full (esteem equivalent to one), then the estimation of the w-arrange counter is each of the one Hence, the actuation of the rve flag causes the counter to flood; consequently in the following clock cycle (through the unit slump delay) the tge flag is empowered and every one of the cells (since every one of the yields of the decoder of Fig. 3 are empowered) are set to zero. When changing from ordinary to test mode, the w-organize counter is reset. Amid test mode, the w-bit yield of the counter is connected to the CUT sources of info. The yields of the counter are additionally used to address a cell. In the event that the cell was vacant (reset), it will be filled (set) and the RV will be empowered. Something else, the cell stays full and the RV is not empowered.

IV. RESULTS:



V. CONCLUSION:

BIST plans constitute an alluring answer for the issue of testing VLSI gadgets. Input vector observing simultaneous BIST plans perform testing amid the circuit ordinary operation without forcing a need to set the circuit disconnected to play out the test, consequently they can go around issues showing up in disconnected BIST strategies. The assessment criteria for this class of plans are the equipment overhead and the CTL, i.e., the time required for the test to finish, while the circuit works ordinarily. In this brief, a novel information vector monitoring simultaneous BIST engineering has been introduced, in view of the utilization of a SRAM-cell like structure for putting away the data of whether an information vector has

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showed up or not amid ordinary operation. The proposed plan is appeared to be more proficient than already proposed input vector observing simultaneous BIST procedures regarding equipment overhead and CTL.

REFERENCES:

[1]E. J. McCluskey, "Built-in self-test techniques," IEEE Design Test Comput., vol.2, no.2, pp.21–28, Apr.1985.

[2]I.Voyiatzis, A. Paschalis, D.Gizopoulos, N.Kranitis, and C.Halatsis, "A concurrent BIST architecture based on a self-testing RAM," IEEE Trans.Rel., vol.54, no.1, pp.69–78, Mar.2005.

[3]I.Voyiatzis and C. Halatsis, "A low-cost concurrent BIST scheme for increased dependability," IEEE Trans. Dependable Secure Comput.,vol.2, no.2, pp.150–156, Apr.2005.

[4] K. K. Saluja, R. Sharma, and C. R. Kime, "A concurrent test- in technique for digital circuits," IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol.7, no.12, pp.1250–1260, Dec.1988.

[5] R. Sharma and K. K. Saluja, "Theory, analysis and implementation of an on-line BIST technique," VLSI Design, vol.1,no.1, pp.9–22, 1993.

[6] K. K. Saluja, R. Sharma, and C. R. Kime, "Concurrent com- parative built-in testing of digital circuits," Dept. Electr. Comput. Eng., Univ. Wisconsin, Madison, WI, USA, Tech. Rep.ECE-8711,1986.

[7]I.Voyiatzis,T.Haniotakis,C.Efstathiou,andH.Antonopoulou,"Acon- current BIST architecture based on monitoring square windows," in Proc. 5thInt. Conf. DTIS, Mar.2010,pp.1–6.

[8]M.A.Kochte, C.Zoellin, and H.J.Wunderlich," Concurrent self-test with partially specified patterns for low test latency and overhead," in Proc.14thEur.TestSymp., May2009, pp.53–58.

[9]S.Almukhaizim and Y.Makris, "Concurren terrorde tection methods for asynchronous burst mode machines," IEEE Trans.Comput.,vol.56, no.6,pp.785–798,Jun.2007.

[10]S.Almukhaizim, P.Drineas, and Y.Makris," Entropy-drivenparity tree selection for low cost con current error detection," IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 25, no. 8, pp. 1547–1554, Aug.2006.