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# Low Power Test Data Compression Techniques for Digital VLSI Circuits

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## Abstract:
The always expanding test data volume and test power consumption are the two noteworthy issues in testing of digital integrated circuits. The sweep based testing technique is generally utilized as a part of industry to test digital ICs with programmed test supplies (ATEs). Be that as it may, the real issue in the sweep based testing is, it requires huge memory to store the examples and in addition its reaction in ATEs. The business ATEs has restricted memory and I/O channel limit and it is hard to store the test designs as it seems to be. The bigger test data volume requests the prerequisite of bigger memory to store the examples and reaction in the ATE and in addition draws out circuit's testing time, hence critical increment of the testing cost. Along these lines, it is important to pack the test data before it is put away on ATE. Likewise, the power dispersal of the digital ICs amid test mode is higher when contrasted with its typical mode of operation. This powerful scattering amid test mode influences the circuit dependability because of raised normal power amid stacking and emptying of the test boosts and its reaction. It adds to the warm load which can bring about auxiliary harm to silicon, holding wires, or bundle. The pinnacle power prompts to mistaken data move in catch period of test mode, which refutes the testing procedure and prompts to pointless yield misfortune. In this way, it is important to create procedures to diminish the test data volume and power consumptions to test complex framework on-a-chips (SoCs). Productive systems for test data lessening can diminish the testing time, test power and ATE memory necessities. This postulation displays a few test data pressure strategies to accomplish high pressure proportion and low test power for output based test applications.

The proposed systems, for example, low-power particular example pressure (LP-SPC), multistage nine-coded and exchanging recurrence coordinated equivalent run-length encoding (9C-AFDER), multistage nine-coded and run-length based Huffman coding (9C-RLHC) and rotating measure up to run-length (AERL) filling accomplish high pressure proportion, low test power, lessened testing time with little zone overhead. Trials are led on bigger ISCAS'89 benchmark circuits to approve the viability of the proposed strategies in Testing.

## 1.2 SCAN TESTING:
The sweep testing is a method utilized as a part of DFT which makes testing less demanding by giving a basic approach to set and watch each flip-tumble in an IC. In sweep based testing, all practical flip-flops (FFs) are supplanted with output flip-flops (SFFs) to expand the controllability and perceptibility of the circuits as appeared in Figure 1.1. It works in three modes: ordinary, move and catch modes. In typical mode, all test signals get to be idle, and the sweep configuration works in the utilitarian design. In move mode, SFFs go about as at least one output chains (framed by interfacing the SFFs into single or various move registers). The test vectors produced utilizing programmed test design generators are stacked into output chains by move in and the test reaction acquired in light of the combinational segment of the circuit move out through sweep chains. In catch mode, the whole SFFs work as ordinary useful flip-slumps and load the combinational bit test reaction for the connected test vector. In this technique, the complexities of testing successive circuits are lessened by method for testing the combinational

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part of the circuits utilizing combinational ATPG apparatus rather than complex consecutive ATPG instrument. Amid the testing procedure, the test examples are connected.

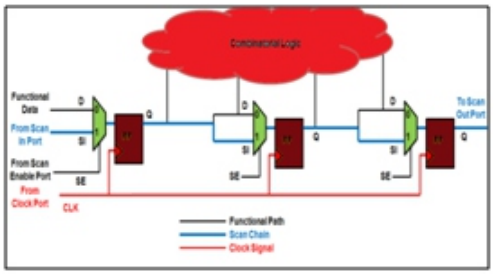

Figure 1.1: Scan Testing

To the circuit under test (CUT) and the yield reactions are broke down, i.e. the yield reactions are contrasted and its predefined blame free reactions. Figure 1.2 demonstrates the technique of utilization of test example to the circuit under test where the D flip-flops encouraged back the yields to the information sources. The select contribution of the MUX is the output empower (Scan−en) bit. At the point when Scan−en is low, the circuit works in typical mode. The contribution for DFF originates from mix rationale and the yield from DFF can be sent to the combinational rationale. The combinational rationale in a full-check circuit has two sorts of data sources (yields) called essential information sources (yields) and pseudo essential data sources (yields) as appeared in Figure 1.2. Essential data sources (PIs) and essential yields (POs) are allude to the outside contributions to the circuit and outer yields from the circuit separately. Then again, the pseudo essential sources of info (PPIs) and pseudo essential yields (PPOs) are alluding to the sweep cell yields and data sources separately. In the ordinary mode, the Scan−en bit is low and the flip-flops introduce in the plan go about as consecutive components that criticism the yield to the information. While in the test mode, the Scan−en bit is made high and the DFFs are supplanted with SFFs. In test mode, all the SFFs in the chain together shape a long move enroll. The info and yield to the output chain are known as the Scan in and Scan out separately. Every information drives a solitary.

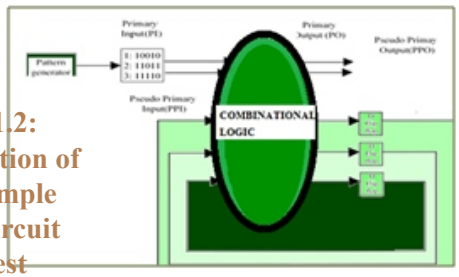


Figure 1.2: Application of test example to the circuit under test

Check chain amid full-filter mode and the yield is watched. The Scan in information bits are moved into the sweep chain. Contribution to SFF is neither taken from the mix rationale nor given to the combinational rationale. A clock flag controls all the FFs in the chain amid both the move and catch stages. Figure 1.3 demonstrates a solitary output chain (intense bolt) in the circuit, with Scan In and Filter Out ports. We consider the sweep flip-failures to be controlled by the Scan Enable piece and they work when it turns out to be high. At first all the SFFs are at the obscure state (X). Give the main sweep access vector be 100101011. At every clock cycle, one piece gets moved in. For the most part, the output move recurrence is much lower than the useful recurrence of the circuit. The higher the test recurrence, the shorter will be the test time Now we shift the complete test vector from LSB to MSB, into the scan-chain so that the Scan Enable bit was forced to high as shown in Figure 1.4. After shift in, we force the Scan Enable to 0 and the test vector that was shifted in, is applied to the combination logic that are driven by the scan flip-flops. Thus the 2nd, 3rd, and 4th combinational

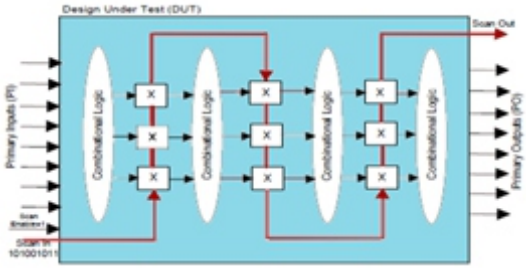


Figure 1.3: Working of scan-chain – stage -1

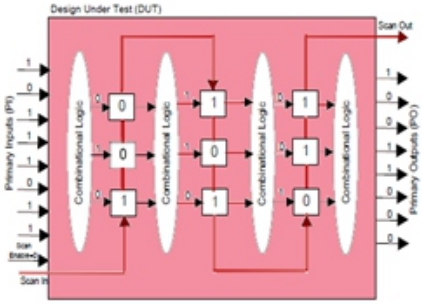


Figure 1.4: Working of scan-chain stage --2

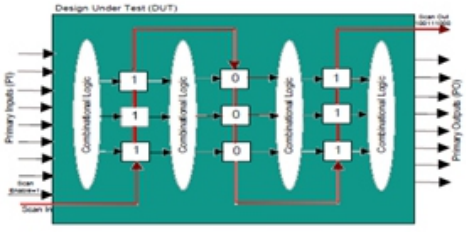


Figure 1.5: Working of scan-chain – stage -3

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Rationale has their constrained test inputs. For the first combinational rationale, we constrain the PI as the test info and afterward we measure the PO which is the yield originating from the fourth combinational rationale. With the particular sources of info connected to the combinational rationale, the combinational rationale has produced their yields. The yield of the fourth combinational rationale can be seen from the PO. For the other combinational rationale, the yield values must be pushed into the sweep flip-slumps and must be moved out. With a specific end goal to push the yield estimations of combinational rationale 1, 2 and 3 into SFFs, flip the framework clock. When flip the framework clock, all D flip-flops (filter flip-lemon) will catch the qualities at their D input. At that point the caught combinational rationale reactions are moved out. While doing that, the following test vector 111000111 is moved all the while by setting the Scan−en to1 as appeared in Figure 1.2. At long last the test reaction for first test vector is totally moved out, and in the meantime we examine in the new test vector input. The procedure proceeds along these lines until all the test vectors are connected.

## Conclusion:

A few productive low-power test data pressure strategies are proposed for concurrent lessening of test data volume and test power in output based test applications. The proposed low-power specific example pressure (LP-SPC) strategy depends on the way that the test set with more unspecified bits can accomplish higher pressure proportion. The power lessening method depends on cautious mapping of the unspecified bits in pre-registered test sets to 0 and 1. It prompts to critical investment funds in pinnacle and normal power without requiring a slower examine clock. We have additionally given decompression engineering basic example change rationale for on-chip decompression, where test design decouples the inner sweep chain from the ATE. We have appeared through investigation and analyses that the LP-SPC procedure can lesser the test application time.

## Future Scope:

We can broaden these systems for multi-check based implanted center to upgrade both test data pressure and the test application time. The high rate of X-bit gives a chance to discover filter chain sharing from various centers, so that the relating test sets can be blended and afterward communicated to different chains in parallel testing. By sharing output chain contributions among a few centers it is conceivable to decrease test data volume and abbreviate test application time fundamentally, since centers that share chains are tested simultaneously.

## References:

•El-Maleh, A., S. Al Zahir, and E. Khan (2011). Test data pressure in view of geometric shapes. PCs and Electrical Engineering 37(3), 376–391.

•Ichihara, H., Y. Iwamoto, Y. Yoshikawa, and T. Inoue (2011). Test pressure in light of lossy picture encoding. In Proceedings of the Asian Test Symposium, pp. 273–278.

•Brother, A. B. also, N. Nicolici (2010). Time-multiplexed packed test of soc designs. IEEE Trans. Large Scale Integr, (VLSI) Syst. 18(8), 1159–1172.

•Koenemann, B., C. Barnhart, B. Keller, T. Snethen, O. Farnsworth, and D. Wheater (2001). A smartbist variation with ensured encoding. In Proceedings of the Asian Test Symposium, pp. 325–330.

•Krishna, C. also, N. Touba (2002). Lessening test data volume using lfsr reseeding with seed pressure. In Proceedings of thee International Test Conference, pp. 321–330.

•Li, L. also, K. Chakrabarty (2004). Test set inserting for deterministic bist using a reconfigurable interconnection arrange. IEEE Trans. Comput.- Aided Design Integrated Circuits Syst. 23(9), 1289–1305.

•Usha, M., D. Kankar, and D. Niranjan (2010). Run-length-based test data pressure methods: How a long way from entropy and power limits? an overview. VLSI Design 2010(9).

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