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An Area Efficient Parallel Distributed Arithmetic Based VLSI Architecture for Design of 2D-DCT

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Abstract:
The paper describes the outline of 2D-discrete cosine change (DCT) which is generally utilized as a part of picture and video pressure calculations. The target of this paper is to plan a completely parallel distributed arithmetic (DA) architecture for two dimensional (2D) DCT to be implemented in Xilinx. DCT requires extensive measure of scientific calculations including multiplications and collections. The multipliers consume expanded power and region; henceforth multipliers are totally disposed of in the proposed plan. distributed arithmetic (DA) architecture is a technique for alteration at bit stream for whole of item or vector dot item to conceal the multiplications. DA is especially reasonable for FPGA plans as it decreases the measure of a increase and aggregate equipment. The speed is expanded in the proposed plan with the completely parallel approach. In this work, existing DA design for 2D-DCT and the proposed region effective completely parallel DA design for 2D-DCT are figured it out. The simulation and synthesis is performed utilizing Xilinx ISE.

Keywords: DCT, Parallel Architecture Distributed Arithmetic, Register banks, adders and multipliers

1. Introduction:

A discrete cosine transform (DCT) expresses a sequence of finitely many data points in terms of a sum of cosine functions oscillating at different frequencies.

DCTs are important to numerous applications in science and engineering, from lossy compression of audio and images (where small high frequency components can be discarded), to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical in applications such as compression. The cosine functions are much more efficient where as for differential equations the cosines express a particular choice of boundary conditions. As like Fourier-related transform, DFT, discrete cosine transforms (DCTs) express a function or a signal in terms of a sum of sinusoids with different frequencies and amplitudes. And which operates on a function at a finite number of discrete data points.

However, this visible difference is merely a consequence of a deeper distinction. A DCT implies different boundary conditions than the DFT or other related transforms. Frequency analysis of discrete time signals is most convenient in DCT. Discrete cosine transform is the most popular transform technique for image compression and is adopted on various standardized coding schemes. Some applications require real-time manipulation of digital images. Because this, fast algorithms and specific circuits for DCT have been developed. Among the methods for two-dimensional DCT, the indirect method based on row-column decomposition is the best method for hardware implementation.

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The energy compaction property of the DCT is well suited for image compression since, as in most images, the energy is concentrated in the low to middle frequencies, and the human eye is more sensitive to the middle frequencies. A large majority of useful image contents change relatively slowly across images, i.e., it is unusual for intensity values to alter up and down several times in a small area, for example, within an 8 x 8 image block. Translate this into the spatial frequency domain, it says that, generally, lower spatial frequency components contain more information than the high frequency components which often correspond to less useful details and noises. The Discrete Cosine Transform, transforms data into a format that can be easily compressed. The characteristics of the DCT make it ideally suited for image compression algorithms.

These algorithms let you minimize the amount of data needed to recreate a digitized image. Reducing digitized images into the least amount of data possible has some advantages such as Less memory required to store images, Less time may be needed to analyze images, Channel bandwidth efficiency increased when transmitting images. Performing the DCT on a digitized image creates a data array that can be compressed by data compaction algorithms. Then, data can be stored or transmitted in its compacted form. The image quality depends on the amount of quantization used in the compaction algorithm. To reproduce the original image, the data is retrieved from memory, uncompacted, and an inverse DCT is performed.

2. Related Work:

Discrete cosine transform (DCT) is a widely used tool in image and video compression applications [1]. Recently, the high-throughput DCT designs have been adopted to fit the requirements of real-time applications [2]–[11]. The multiplier-based DCTs were presented and implemented in [2] and [3].To reduce area, ROM-based distributed arithmetic (DA)was applied in DCT cores[4]–[6].

Uramotoet al.[4] implemented the DA-based multipliers using ROMs to produce partial products together with adders that accumulated these partial products. In this way, instead of multipliers, the DA-based ROM can be applied in a DCT core design to reduce the area required. In addition, the symmetrical properties of the DCT transform and parallel DA architecture can be used in reducing the ROM size in [5] and [6], respectively. Recently, ROM-free DA architectures were presented [7]–[11]. Shams et al. employed a bit-level sharing scheme to construct the adder-based butterfly matrix called new DA (NEDA) [7]. Being compressed, the butterfly-adder-matrix in [7] utilized 35 adders and 8 shift-addition elements to replace the ROM. Based on NEDA architecture, the recursive form and arithmetic logic unit (ALU) were applied in DCT design to reduce area cost [8], [9].

Hence the NEDA architecture is the smallest architecture for DA-based DCT core designs, but speed limitations exist in the operations of serial shifting and addition after the DA-computation. The high-throughput shift-adder-tree (SAT) and adder-tree (AT), those unroll the number of shifting and addition words in parallel for DA-based computation, were introduced in [10] and [11], respectively. However, a large truncation error occurred. In order to reduce the truncation error effect, several error compensation bias methods have been presented [12]–[14] based on statistical analysis of the relationship between partial products and multiplier-multiplicand. However, the elements of the truncation part outlined in this work are independent so that the previously described compensation methods cannot be applied.

3. Existing ECAT ARCHITECTURE:

From (2), the shifting and addition computation can be written as follows:

$$y = \sum_{j=0}^{Q-1} y_j 2^{-j}$$

In general, the shifting and addition computation uses a shift-and-add operator [7] in VLSI implementation in

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order to reduce hardware cost. However, when the number of the shifting and addition words increases, the computation time will also increase. Therefore, the shift-adder-tree (SAT) presented in [10] operates shifting and addition in parallel by unrolling all the words needed to be computed for high-speed applications. However, a large truncation error occurs in SAT, and an ECAT architecture is proposed in this brief to compensate for the truncation error in high-speed applications. In Fig. 1, the Q P-bit words operate the shifting and addition in parallel by unrolling all computations. Furthermore, the operation in Fig. 1 can be divided into two parts: the main part (MP) that includes P most significant bits (MSBs) and the truncation part (TP) that has Q least significant bits (LSBs). Then, the shifting and addition output can be expressed as follows:

$$Y = MP + TP.\,2^{-(p-2)}$$

The output Y will obtain the _-bit MSBs using a rounding operation called post truncation (Post-T), which is used for high-accuracy applications. However, hardware cost increases in the VLSI design.

In general, the TP is usually truncated to reduce hardware costs in parallel shifting and addition operations, known as the direct truncation (Direct-T) method. Thus, a large truncation error occurs due to the neglecting of carry propagation from the TP to MP. In order to alleviate the truncation error effect, several error compensation bias methods have been presented [12]–[14]. All previous works were only applied in the design of a fixed-width multiplier.

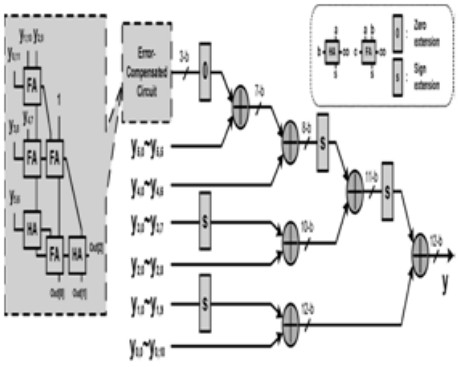

Fig 1. ECAT architecture

The proposed ECAT architecture is illustrated in Fig. 2 for (P,Q)=(12,6) (case 3), where block FA indicates a full-adder cell with three inputs (a, b, and c) and two outputs, a sum (s) and a carry-out (co). Also, block HA indicates half-adder cell with two inputs (a and b) and two outputs, a sum (s) and a carry-out (co).

4.Proposed Architecture:

The hardware architecture of the 2D DCT is shown in figure 2. The design has a 64-bit data input and 112-bit output. Each input coefficient is equal to 8 bits. So, the eight coefficients (64-bit) of each row are shifted into the register during the first clock cycle. In the next stage, the adders and subtractors perform the first butterflies. In order to keep full accuracy, the outputs of the butterflies should be 9 bits long. Then, the data are loaded into parallel-in serial-out registers that repackage the data into 4-bit addresses that serially feed the ROM and Accumulators, from RAC0 to RAC7, with MSB first. The RAC's help in the calculation of the DCT using the pre-determined values stored in the ROM's. The result of 1D-DCT is obtained up to this stage. In order to obtain results for 2D-DCT a transpose is taken to the 1DDCT output matrix and then the same process as in the calculation of 1D-DCT is used to find the final 2D-DCT values.

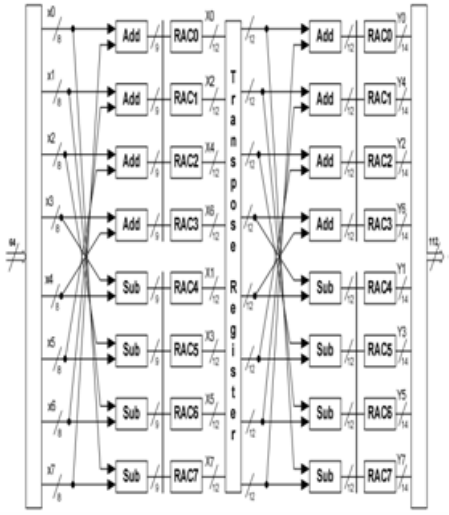

fig 2. 2D DCT Architecture

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A straightforward architecture of the RAC by using DA structure is depicted in figure 3. The serial inputs limit the performance of such structure, but a better performance can be obtained by using more hardware resources. In the proposed strategy, DA is actualized with an increment in asset by processing it in a completely bit-parallel way. This implies each section of bits is encouraged into the framework in the meantime. In a completely parallel approach each section of information bit has relating LUT and the outcomes will join speedier. The key components required to execute the DA, if data sources are spoken to with 8 bits are a 8 component LUT furthermore, a decoder, a viper/subtractor, and a shifter. These components are assembled together to frame the DA structure as appeared in figure 4. Multiplexer inputs every segment of information bits in parallel to the each LUT. The substance of first LUT of the slightest critical section of bit gets summed with the moved substance of the following LUT of the following piece. Similarly the moved substance of each LUT are summed up to shape the DCT coefficient.

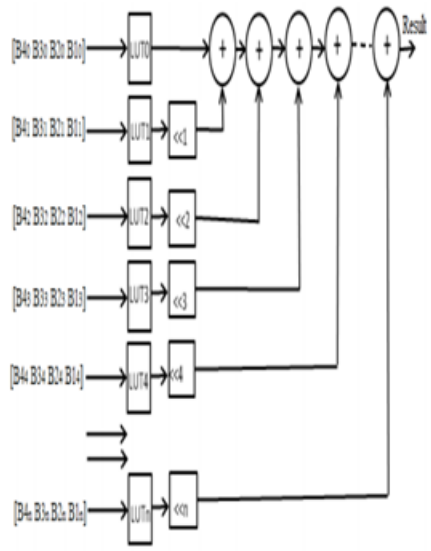
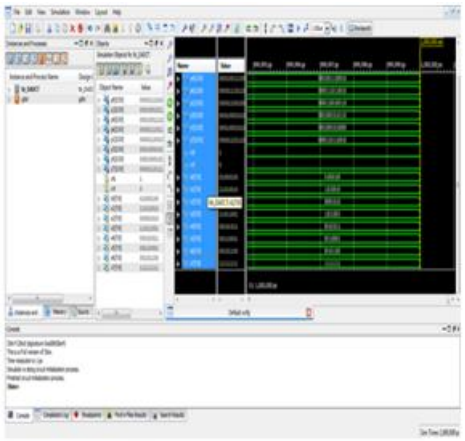


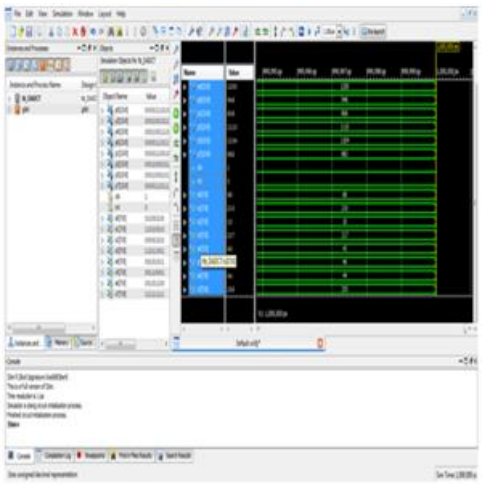
Fig 3. Fully Parallel RAC Structure

5. Results:

DA design of 2D-DCT for the current and proposed strategy is composed utilizing VHDL. The recreation is performed utilizing Xilinx ISE.

The recreation result containing 2D-DCT qualities is appeared in Figure 5 and in Figure 6. The VHDL code is orchestrated With Xilinx ISE test system. The re-enactment consequences of both the traditional and proposed structures were checked for precision and are contrasted and each other. Both created similar outcomes furthermore the proposed strategy's comes about united speedier than the current strategy and consequently observed to be time effective.





6. Conclusion:

The fundamental point of this paper is to outline engineering for discrete cosine change which is utilized as a part of picture and video pressure frameworks. The outline proposed in this paper is a territory effective completely parallel appropriated math (DA) engineering for 2D-DCT.

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Completely parallel circulated number juggling design is utilized to actualize augmentation without the utilization of multiplier. By the proposed DA engineering, decrease in region also, increment in speed is accomplished for 2D-DCT contrasted with the current strategy.

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