

Berger Checks and Fault Tolerant Reversible Arithmetic Component Design

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Abstract:

In order to continue the revolution in the computer hardware performance, we need to reduce the energy dissipated in each logic operation. Energy dissipation can be reduced by preventing information loss. This is achieved by designing the circuits using reversible logic gates. It has wider applications in the fields of quantum computing, nanotechnology, and many more. Fault Tolerant logic has become a very important technique in the present day electronics, in order to minimize the errors in the circuit. Fault Tolerant gates with error detection capability, turns down the need for any external hardware to test the circuit. In this paper, we have proposed a reversible Fault Tolerant Adder/Subtractor and also a Berger check prediction circuit to check all unidirectional and multiple errors for all reversible Adders/ Subtractors. This is the first attempt in the literature to implement a Berger check logic using reversible gates. The performance parameters of both reversible Berger check logic and the Fault Tolerant reversible logic has been compared and analyzed. Fault Tolerant logic, though it doesn't require any external hardware, the quantum cost is found to be 25% more than Berger check logic and garbage outputs required is 75% more, similarly ancilla inputs is 25%, gate count is 45% and delay of circuit is 30% more than the proposed Berger check circuit. Hence, the Berger check circuit is found to more efficient in terms of quantum cost, delay and gate count.

Keywords:

Fault Tolerant; Berger check prediction; Adder/Subtractor; error detection; quantum cost.

INTRODUCTION:

Reversible logic has wide applications in the field of quantum computing, low-power design, nanotechnology, optical information processing and bio informatics. Landauer proved that combinational logic circuits dissipate heat in an order of $kT \ln 2$ joules for every bit of information that is lost [1]. Reversible logic circuits do not lose information as it is possible to regenerate inputs from observed outputs. Ben net showed that $kT \ln 2$ energy dissipation would not occur, if a computation were carried out in a reversible way [2]. A circuit is said to be reversible if for each input there exists a unique output that is, number of inputs must be equal to number of outputs [3]. A reversible circuit has neither feedback nor fan-out. Fault detection can generally be done in three methods: parity preserving method, parity generation method and dual rail online error detection methods. Among these, the most widely used method is parity preservation technique. It is implemented at the gate level. Hence there is no extra cost in design and verification effort [4]. Parity check is one of the widely used mechanisms for detecting single level faults. Thus, parity preserving circuit design is important for the development of Fault Tolerant reversible systems in nanotechnology [5]. Unidirectional error detecting codes like Paritycode, Hamming code, Reed Solomon code, Berger code and Bose Lin code can be used to construct a Fault Tolerant circuit. Parity code is the simplest and cheapest error detecting code [6] as it requires only one error-check bit to append to the information bits.

This error-check bit is computed in such a way that the number of 1's in information bits along with parity bit is made odd or even. Hardware overhead is very less and computation speed is high [7]. But it can detect only single errors or all odd number of errors in the information bits. The modified version of parity code is Hamming code. But when compared to parity code, it requires additional hardware overhead. This technique also detects only single errors and double errors and not all unidirectional errors. Reed Solomon code is a polynomial based error detection code [8] providing error correction capability but at the cost of increased area and speed overhead when compared to Hamming code and cannot detect all unidirectional errors. Berger code and Bose-Lin codes are systematic and separable codes. Bose-Lin codes have fixed number of check bits and is not dependent on number of information bits [9]. It can detect unidirectional errors. On the other hand, Berger codes are optimal, in terms of the number of check bits required for I information bits, among all separable codes that detect unidirectional errors [10]. No extra decoders are required to extract the information bits, when needed for processing from the code word. They detect all multiple, unidirectional errors. It is least redundant code among all unidirectional error detection (AUED) codes [11]. In this paper, we have used Berger code method to design a circuit which will make any Full Adder/ Subtractor Fault Tolerant with optimized garbage output, ancilla input and quantum cost. Also, Fault Tolerant reversible Full Adder/ Subtractor are also designed using existing Fault Tolerant gates and the results are compared with the one pre-existed in the literature and also with the Berger check method. In this paper, we emphasize on the fact that, though Fault Tolerant circuits using Fault Tolerant gates requires no additional hardware to detect all unidirectional errors, it is found that the circuit with Berger check implementation has better performance in terms of quantum cost, garbage output and ancilla inputs.

II. PRELIMINARIES:

A. Reversible Gates and Parameters:

Some of the reversible gates are NOT gate, CNOT/ FEYNMAN gate, TOFFOLI gate, FREDKIN gate and PERES gate. Important parameters of any reversible circuit are as follows:

Gate count (GC): The number of gates used to realize reversible circuit.

Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.

Ancilla Inputs (AI): The number of inputs kept constant at either 0 or 1.

Quantum Cost (QC): The cost of the circuit in terms of cost of a primitive gate.

Delay (Δ): It corresponds to number of primitive quantum gates in the critical path of the circuit.

B. Fault Tolerant / Parity Preserving Reversible Gates:

Parity checking is one of the most widely used techniques for error detection in digital logic systems [3]. A reversible gate will be parity preserving if the parity of the inputs matches the parity of the outputs. Mathematically, a reversible gate having 'n' input lines and 'n' output lines will be parity preserving if and only if:

$$I_1 \oplus I_2 \oplus \dots \oplus I_n = O_1 \oplus O_2 \oplus \dots \oplus O_n$$

Where I_i and O_j are the input and output lines respectively.

C. Berger Codes:

The Berger code is a separable and unordered code, is sensitive to propagation delays of individual bits in a code word. Berger codes were introduced by J.M. Berger in 1961 [12].

The codes are optimal systematic codes that detect all unidirectional errors [13]. Berger codes are formed by appending a special set of bits, called the check bits to each word of information. The check bits are created based on the number of 1's in the original information. A Berger code of length 'n' will have 'I' information bits and 'K' check bits [10] where

$$K = \lceil \log_2(I+1) \rceil \dots \dots \dots (1)$$

$$\text{And } n = I + K \dots \dots \dots (2)$$

D. Literature Survey:

Reliable computing and quantum computing is one of the emerging areas in today's world. Berger codes can detect stuck-at faults and skews in asynchronous systems which is a part of reliable computing [13]. On the other hand, reversible logic is a growing technique in low power applications such as quantum computing. Work proposed in [14] discusses different concurrent error detecting arithmetic and logic units using Berger codes such as signed and unsigned addition and subtractions, 16 logical operations, shift operations, multiplication and division. Authors in [10] used Berger code as a means of incorporating CED (Concurrent Error Detection) into a self-checking register file.

A Berger check prediction circuit is an external circuit that needs to be built to test errors. In the mean while, Fault Tolerant reversible circuits are those which do not require any additional hardware, but has an inherent property of detecting errors. Several Fault Tolerant Adders and Subtractors has been proposed in the literature. Fault Tolerant Full Adder using Fredkin gate with Feynman gate to preserve the parity has been proposed in [4]. In the same way reversible Full Adder has been proposed using IG gate and F2PG gate by the authors in [15] and [5] respectively. In the literature, this is the first attempt of designing a reversible Berger check prediction circuit using reversible gates. Also, a reversible Fault Tolerant circuit has been designed with optimized parameters.

The designed circuits are analyzed in terms of performance parameters to detect unidirectional errors. In case of parity preserving technique, if multiple errors occurs on the same line then it cannot detect them, as one error may cancel other. Hence this technique cannot detect multiple errors.

III. DESIGN

A. Existing Efficient Adder and Subtractor:

An efficient reversible Full Adder and Subtractor has been designed by authors in [16] which is as shown in Fig. 1 and Fig.2 respectively. We use this design as a basic circuit for reversible Adder and Subtractor. Proposed Berger check circuit is implemented on this to detect any unidirectional and multiple errors present. Fig. 1. a. 1-bit Reversible Full Adder proposed in [16] b. Equivalent Representation

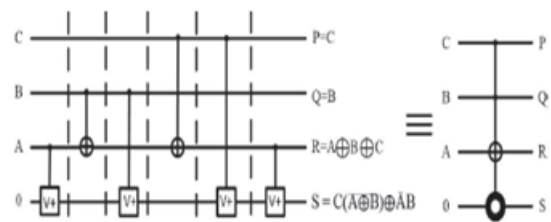


Fig. 2.a. 1-bit Reversible Full Subtractor proposed in [16] b. Equivalent Representation

B. Berger Check Reversible Circuit Design:

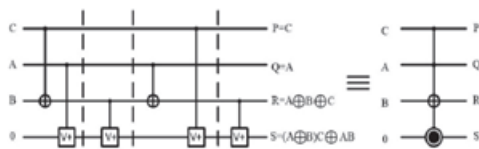
The reversible 1-bit Full Adder/Subtractor proposed in [16] has a quantum cost of 6 and a delay of 6Δ, which is very efficient compared to all other designs in the literature. Berger check circuit proposed in this paper is based on following logic:

Let two n-bit numbers be $X = X_n \dots X_2 X_1$ and $Y = Y_n \dots Y_2 Y_1$. Let the sum and internal carries be $S = S_{n-1} \dots S_1 S_0$ and $C = C_n \dots C_2 C_1$, where $X_i, Y_i, S_i, C_i \in \{0, 1\}$.

Let $N(X)$ denote the number of 1's in the binary representation of X that is $N(X_i) = X_i$.

Hence the Berger check prediction equation [14] is as follows: $N(X) + N(Y) + C_{in} = N(S) + N(C) + C_{out}$(3a)

where C_{in} is the carry input and $C_{out} = C_n$.



The modified form of equation 3a is as shown below:
 $N(S) = N(X) + N(Y) + C_{in} - N(C) - C_{out}$(3b)

Berger check logic can detect both unidirectional and multiple errors. If there are multiple errors in the circuit such as flipping of two bits of same type, then there will be in equality in equation 3a. Hence error is detected. But Berger check prediction algorithm fails when both 1 and 0 are flipped in the data word [17]. In such a case, errors are not detected. The Berger check circuit shown in Fig 3 requires 5 ancilla inputs and produces 2 garbage outputs. The quantum cost of the circuit is 30 with a delay of 22 Δ . Hence when this circuit is combined with Full Adder/Subtractor, the total quantum cost of the circuit is found to be 72 for reversible Full Adder and 80 for reversible Full Subtractor. In this design, a Berger code check prediction circuit has been designed using Peres gate and Toffoli gate. The proposed Berger check circuit works for both reversible Full Adder and Full Subtractor as depicted in Fig 3.

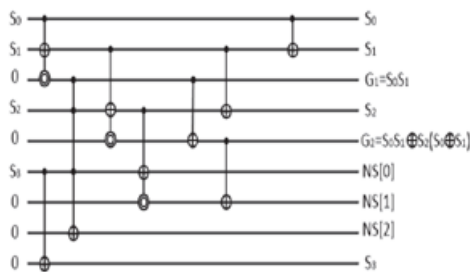


Fig. 3. Berger check circuit for Reversible Full Adder/Subtractor

The Berger check circuit is designed based on equation 3b. The output of Full Adder/Subtractor is given as inputs to the Berger Check circuit with S_0 , S_1 , S_2 and

S_3 being sum/difference. The output $(N(S))$ is generated in binary form represented by $NS[2]$ to $NS[0]$. The obtained $N(S)$ from the Berger circuit is compared with theoretically calculated $N(S)$ from equation 3b to detect errors, if any.

C Parity Preserving Reversible Circuits:

A novel Fault Tolerant reversible Full Adder and Subtractor has been designed using Fault Tolerant gates such as Fredkin gates and Feynman double gates as shown in Fig. 4 and Fig. 5 respectively. Table I shows performance parameters comparison of Fault Tolerant Adder designs in the literature.

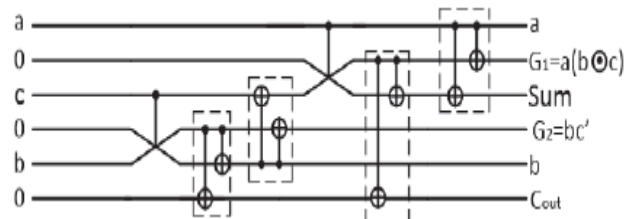


Fig. 4.1-bit reversible Full Adder design using Fault Tolerant gates

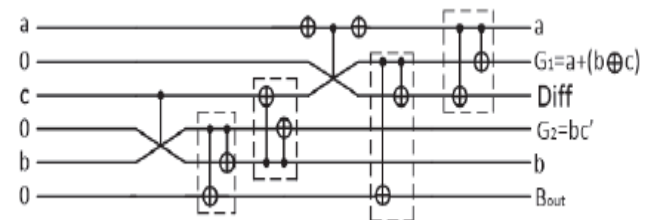


Fig. 5.1-bit reversible Full Subtractor design using Fault Tolerant gates

TABLE. I. COMPARISON OF 1-BIT REVERSIBLE FAULT TOLERANT FULL ADDER

Designs	AI	GO	QC	Δ
[1]	3	1	26	15 Δ
[2]	2	3	14	14 Δ
[3]	2	3	14	14 Δ
[4]	2	3	14	14 Δ
[5]	2	3	20	20 Δ
[15]	2	3	14	14 Δ
Proposed (Design 2)	3	2	18	18 Δ

The proposed design 2 requires 3 ancilla inputs and produces 2 garbage outputs with a delay of

18 Δ for n -bit Full Adder/Subtractor. For Fault Tolerant reversible Full Subtractor, 2 NOT gates are required in addition to Fault Tolerant reversible Full Adder. The design methodology for both Full Adder and Full Subtractor remains the same. Since Fault Tolerant gates used are parity preserving, all unidirectional errors are detectable with no additional hardware needed.

IV. RESULTS AND DISCUSSIONS:

Proposed Berger check circuit is an additional circuit to detect unidirectional errors in reversible Full Adder/Subtractor. It is found that the proposed Berger check prediction Fault Tolerant Full Adder/Subtractor (Design 1) is more efficient than the proposed Reversible Fault Tolerant Full Adder/Subtractor (Design 2). The quantum cost of circuit in Design 1 is 54 where as in design 2, it is 72. The comparison of 4-bit Reversible Fault Tolerant Full Adder and Subtractor are as depicted in Table II and Table III respectively.

TABLE II. COMPARISON OF 4-BIT REVERSIBLE FULL ADDER

Parameter	Design 1 Fault Prediction using Berger Code (Adder + Berger Check Circuit)	Design 2 Fault Tolerant Circuit
AI	4+5=9	12
GO	0+2=2	8
QC	24+30=54	72
Δ	24+22=46 Δ	66 Δ
GC	4+9=13	24

TABLE III. COMPARISON OF 4-BIT REVERSIBLE FULL SUBTRACTOR

Parameter	Design 1 Fault Prediction using Berger Code (Subtractor + Berger Check Circuit)	Design 2 Fault Tolerant Circuit
AI	4+5=9	12
GO	0+2=2	8
QC	24+30=54	80
Δ	24+22=46 Δ	66 Δ
GC	4+9=13	32

The proposed Fault Tolerant reversible Full Adder in design 2 is found to be more optimized in terms of garbage outputs and delay when compared to other works in the literature. The number of garbage outputs in proposed design 2 which is 33.33% less than in [2, 3, 4, 5, and 6]. Though the garbage output in [1] is 1, the quantum cost of the same is 31% more than the proposed design. The comparison of 4-bit reversible Full Adders using Berger check circuit and Fault Tolerant circuit is as shown in Table IV. The generalized parameters of the proposed designs to n -bit are as shown in Table V.

TABLE IV. COMPARISON OF 4-BIT REVERSIBLE FULL ADDERS USING BERGER CHECK CIRCUIT AND FAULT TOLERANT CIRCUIT

Designs	AI	GO	QC	Δ
[5]	8	12	80	80 Δ
[3]	8	12	56	56 Δ
[15]	8	12	56	56 Δ
Proposed (Design 2)	12	8	72	66 Δ
Proposed (Design 1)	9	2	54	46 Δ

TABLE V. COMPARISON OF N-BIT REVERSIBLE FULL ADDERS/SUBTRACTORS USING BERGER CHECK CIRCUIT AND FAULT TOLERANT CIRCUIT

Parameter	Existing Full Adder/Subtractor		Design 2 (Fault Tolerant Full Adder)	Design 2 (Fault Tolerant Full Subtractor)
	Without Proposed Berger Check Circuit	With Proposed Berger Check Circuit		
AI	n	$2^{n-1}+1$	$3n$	$3n$
GO	$n-1$	$2n-3$	$2n$	$2n$
QC	$6n$	$2^{n+1}+2n+2+2^{n-2}(n-1)$	$18n$	$20n$
GC	n	$2^{n-1}+2n-3$	$6n$	$8n$
Δ	$6n$	$2^n + 2^{n-1} + 6n - 2$	$16n+2$	$16n+2$

V. SIMULATION RESULTS:

The corresponding simulation results of the proposed adder/subtractors are shown below. All the synthesis and simulation results are performed using Verilog HDL.

The synthesis and simulation are performed on Xilinx ISE 14.4. The simulation results are shown below figures.

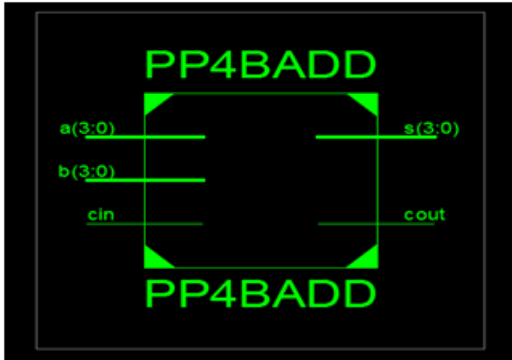


Figure 6: RTL schematic of Top-level of proposed reversible 4bit adder

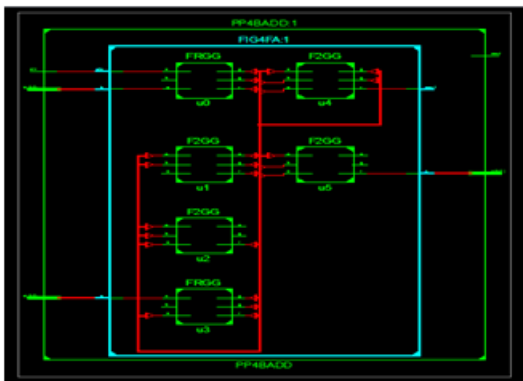


Figure 7: RTL schematic of Internal block of proposed reversible 4bit adder

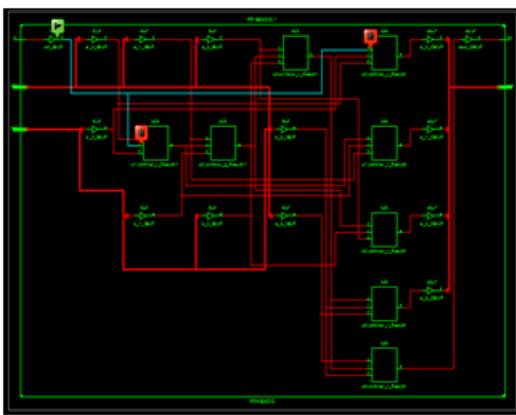


Figure 8: Technology schematic of Internal block of proposed reversible 4bit adder

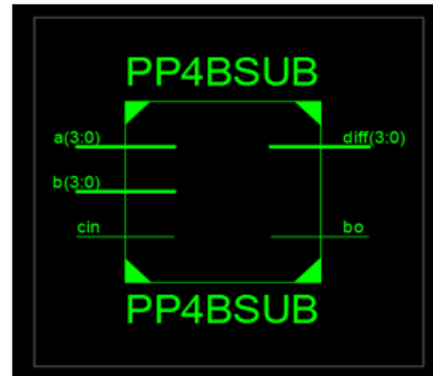


Figure 9: RTL schematic of Top-level of proposed reversible 4bit subtractor

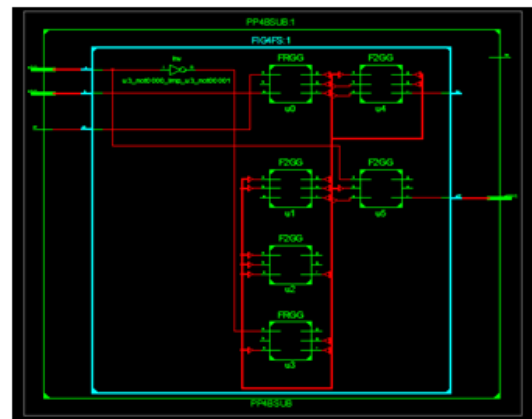


Figure 10: RTL schematic of Internal block of proposed reversible 4bit subtractor

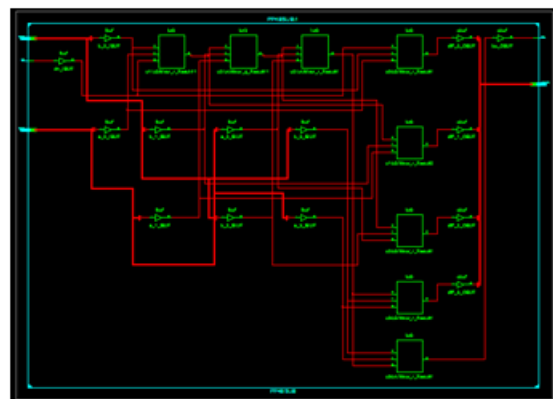


Figure 11: Technology schematic of Internal block of proposed reversible 4bit subtractor

PP4BSUB Project Status (11/24/2016 - 14:51:12)			
Project File:	BCFTR_xise	Parser Errors:	No Errors
Module Name:	PP4BADD	Implementation State:	Synthesized
Target Device:	xc3s500e-fpg320	• Errors:	
Product Version:	ISE 14.4	• Warnings:	
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Mixx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	4	4656	0%
Number of 4 input LUTs	8	9312	0%
Number of bonded IOBs	14	232	6%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu Nov 24 14:49:14 2016			
Translation Report					

Figure 12: Synthesis report of proposed reversible 4bit adder

PP4BSUB Project Status (11/24/2016 - 14:51:12)			
Project File:	BCFTR_xise	Parser Errors:	No Errors
Module Name:	PP4BSUB	Implementation State:	Synthesized
Target Device:	xc3s500e-fpg320	• Errors:	No Errors
Product Version:	ISE 14.4	• Warnings:	12 Warnings (12 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Mixx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
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Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu Nov 24 14:51:10 2016	0	12 Warnings (12 new)	0

Figure 13: Synthesis report of proposed reversible 4bit subtractor



Figure 14: simulated outputs for proposed reversible 4bit adder



Figure 15: simulated outputs for proposed reversible 4bit subtractor

VI. CONCLUSION AND FUTURE SCOPE:

In this paper, we have proposed a Berger check prediction circuit for reversible Full Adder/Subtractor as design 1 and Fault Tolerant reversible Full Adder/Subtractor using Fault Tolerant gates as design 2. It is found that the performance parameters of design 1 is much more efficient than design 2 in terms of quantum cost, garbage outputs, ancilla inputs and delay. The Berger check prediction method to detect errors is proved to be a very efficient technique compared to existing one. The proposed designs are verified by creating libraries in Verilog model and its functionality is verified using Xilinx tool. Thus we conclude that the Berger check logic has been found to be more efficient when compared to other method to detect all unidirectional and multiple errors.

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