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An Arithmetic and Logic Unit Using GDI Technique

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Abstract:
This paper presents a design of a 4-bit arithmetic logic unit (ALU) by taking vantage of the concept of gate diffusion input (GDI) technique. ALU is the most crucial and core component of central processing unit as well as of numbers of embedded system and microprocessors. In this, ALU consists of 4x1 multiplexer, 2x1 multiplexer and full adder designed to implements logic operations, such as AND,OR, etc. and arithmetic operations, as ADD and SUBTRACT.GDI cells are used in the design of multiplexers and full adder which are then associated to realize ALU. The simulation is carried out DSCH3.5 and Microwind3.5 simulator using 65nm technologies and compared with previous designs realized with Pass transistor logic and CMOS logic.

The simulation shows that the design is more efficient with less power consumption, less surface area and is faster as compared to pass transistor and CMOS techniques.

Keywords -- ***GDI technique, ALU, Pass transistor gate.***

I.INTRODUCTION

In the era of growing technology and scaling of devices up to nano meter regime, the arithmetic logic circuits are to be designed with compact size, less power and propagation delay. Arithmetic operations are indispensable and basic functions for any high speed low power application digital signal processing, microprocessors, image processing etc. Addition is most important part of the arithmetic unit rather approximately all other arithmetic operation includes addition. Thus, the primary issue in the design of any arithmetic logic unit is to have low power high performance adder cell. There are various topologies and Methodologies proposed to design full adder cell efficiently. This paper utilizes the concept of GDI technique in the design of ALU and its sub blocks as Multiplexer and Full adder. The rest of paper is organized as follows Section II describes previous works. Section III consists of the description of Gate Diffusion Input Technique. In section IV Arithmetic Logic Unit design, its operation and schematic is explained. Section V describes simulation result and analysis. At last conclusion is made in section VI.

II. PREVIOUS WORKS

There are different types and designs of full adder which is discussed in various papers at state of the art level and process and circuit level. Twelve state of the art full adder cells are: conventional CMOS, CPL, TFA, TG CMOS,C2MOS, Hybrid, Bridge, FA24T, N-Cell, DPL and Mod2f. R. Shalem, E. John, and L.K. John, proposed a conventional CMOS full adder consisting of 28 transistors [1]. Later, the number of transistor count is reduced to have less area and power consumption. A. Sharma, R Singh and R. Mehra, Member, IEEE, have improved performance with Transmission Gate Full adder using CMOS nano technology where 24 transistors are used [2]. The Complementary Pass transistor Logic (CPL) full Adder contains the 18 transistors. The power consumption of this structure is 2.5µw [3].

A Transmission Function Full Adder (TFA) based on the transmission function theory has 16 transistors. The power consumption of this structure is 12µw. N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. The power consumption of this structure is 1.62µw. Mod2f Full Adder contains the 14 transistors, generates full swing XOR and

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XNOR signals by utilizing a pass transistor based DCVS circuit. The power consumption of this structure is 2.23µw [3]. Saradindu Panda, N. Mohan Kumar, C.K. Sarkar, optimized the full adder circuit to 18 Transistor using Dual Threshold Node Design with Submicron Channel Length [4]. T. Vigneswaran, B. Mukundhan, and P.Subbarami Reddy, designed 14 transistor high speed CMOS full adder and significantly improved threshold problem to50% [5].

Gate Diffusion Input Technique is a new method of reducing power dissipation, propagation delay with less area.T. Esther Rani, M. Asha Rani, Dr.RameshwarRao, designed an area optimized low power arithmetic and logic unit in which Arithmetic Logic Unit is implemented using logic gates, pass transistor logic, as well as GDI technique [6].Manish Kumar, Md. Anwar Hussain, and L.L.K. Singh explained a Low Power High Speed ALU in 45nm UsingGDI Technique and Its Performance Comparison [7]. We have designed ALU in different way by using GDIcells to implement multiplexers and full adder circuit. The input and output sections consist of 4x1 and 2x1 multiplexers and ALU is implemented by using full adder.

III. GATE DIFUSSION INPUT TECHNIQUE

Morgenshtein has proposed basic GDI cell shown in Fig.1 [8]. This is a new approach for designing low power digital combinational circuit.GDI technique is basically two transistor implementation of complex logic functions which provides in-cell swing restoration under certain operating condition. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND.

Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design.

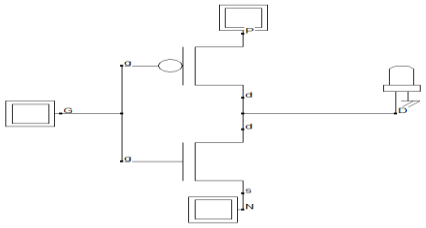

Fig. 1. Basic GDI Cell

There are three inputs in a GDI cell - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N and Prespectively. Table 1 shows different logic functions implemented by GDI logic [8] based on different input values. So, various logic functions can be implemented with less power and high speed with GDI technique as compared to conventional CMOS design.

TABLE 1. LOGIC FUNCTIONS OF BASIC GDI CELL

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

Multiplexer

Multiplexer is a digital switch. The multiplexer has numbers of input data lines and one output line. The selection of a particular input line is controlled by a set of selection line. There are '2n' input lines and 'n' selection lines whose bit combinations determine which input is selected. Fig 2 shows implementation of basic 2x1multiplexer using GDI cell. The 4x1 multiplexer has four inputs, two selection lines and one output. Depending on the two selection lines, one output is selected at a time among the four input lines. Fig. 3 shows implementation of 4x1multiplexer using GDI cell.

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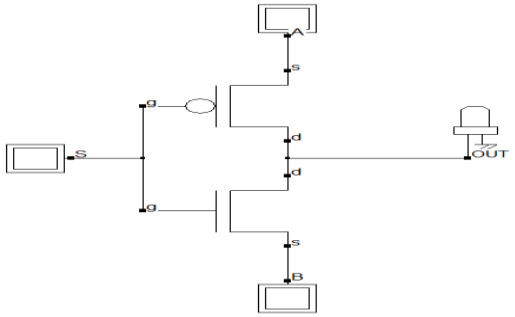

Fig. 2. 2x1 Multiplexer using GDI technique

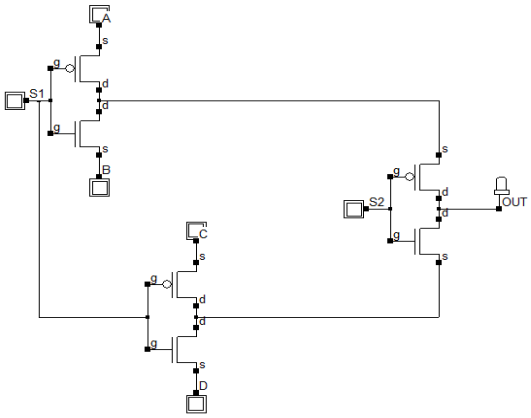

Fig 3. 4x1 Multiplexer using GDI technique

XOR Gate

The main building block of full adder circuit is XOR gate which gives sum output. So the overall performance of full adder circuit can be improved by optimizing XOR gate.Fig.4 shows the implementation of XOR gate using GDItechnique [9]. It uses less number of transistors as compared to conventional design of XOR gate using CMOS logic Units.

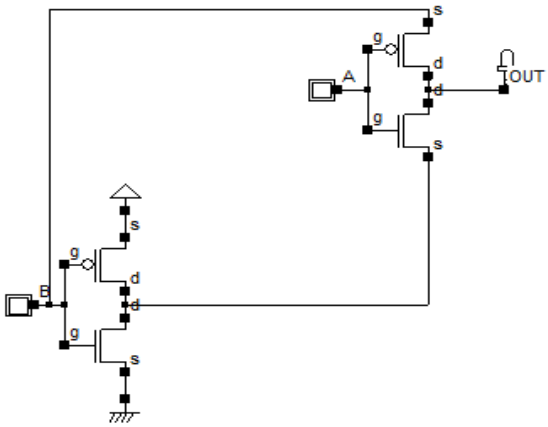

Fig. 4. GDI Based XOR Gate

Full Adder

The Full Adder circuit adds three one-bit binary numbers (A, B & C) and outputs two one-bit binary numbers, a sum(S) and a carry (Cout). The full adder is usually a component in cascade of adders, which add 4, 8, 16 etc. binary numbers. Implementation of full adder circuit using GDI technique which is a basic building block of arithmetic and logic unit has been shown in Fig. 5.

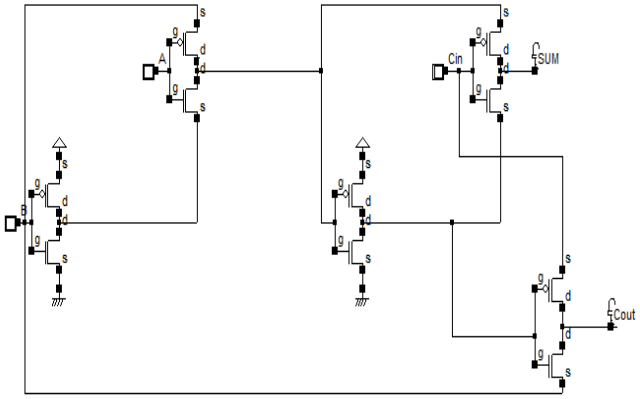

Fig. 5. GDI based 1-bit full adder cell

IV. DESIGN OF ARITHMETIC AND LOGIC UNIT (ALU)

An arithmetic logic unit (ALU) is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. It is responsible for performing arithmetic and logic operations such as addition, subtraction, increment, and decrement, logical AND, logical OR, logical XOR and logical XNOR.

ALU consists of eight 4x1 multiplexers, four 2x1multiplexers and four full adders. The 4-bit ALU is designed in 250nm, n-well CMOS technology. When logic ‘1’andlogic ‘0’ are applied as an input INCREMENT and DECREMENT operations takes place respectively. An INCREMENT operation is analyzed as adding ‘1’ to the addend and DECREMENT is seen as a subtraction operation [6].

Two’s complement method is used for SUBTRACTION in which complement of B is used.

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The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR. Fig. 6 shows the block diagram of 4-bit ALU where first stage to fourth stage is cascaded with the CARRY bit. Symbolic representation of 4-bit ALU has been visualized infig. 7. The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results.

TABLE II. OPERATIONS OF ALU

S2	S1	S0	Cin	FUNCTION	OPERATION
0	0	0	0	A+B	ADD
0	0	0	1	A+B+1	ADD WITH CARRY
0	0	1	0	A+B'	SUTRACT WITH BORROW
0	0	1	1	A-B	SUBTRACT
0	1	0	0	A	TRANSFER A
0	1	0	1	A+1	INCREMENT A BY 1
0	1	1	0	A-1	DECREMENT A BY 1
0	1	1	1	A'	COMPLEMENT A

S2	S1	S0	Cin	FUNCTION	OPERATION
1	0	0	0	A&B	AND
1	0	1	0	A|B	OR
1	1	0	0	A^B	XOR
1	1	1	0	A'	COMPLEMENT

The multiplexer at the output stage selects the appropriate output and route it to output port. Table II shows the truth table for the operations performed by the ALU based on the status of the select signal. The operation being performed and the inputs and outputs being selected are determined by set of three select signals incorporated in the design. Fig 8.shows multiplexer logic at input port and Fig 9. Shows multiplexer logic at output port. The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results. The multiplexer at the output stage selects the appropriate output and route it to output port. Table 2 shows the truth table for the operations performed by the ALU based on the status of the select signal.

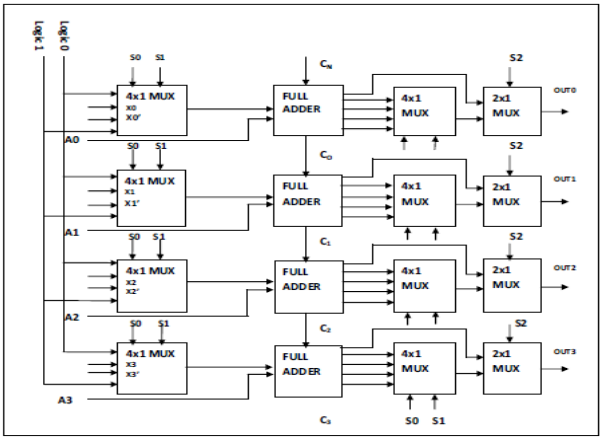

Fig. 6. 4-bit Arithmetic and Logic Unit

The schematic of ALU is designed using schematic editor of DSCH3.5 and Micro wind 3.5. It shows connectivity between the components and describes aspect ratios of the transistor that can be modified along with the design. Figure 10 represents the complete schematic view of ALU. The 4-bit ALUconsists of two 4-bit inputs, three selecting lines, and one carry input, one carry output and four output bits.

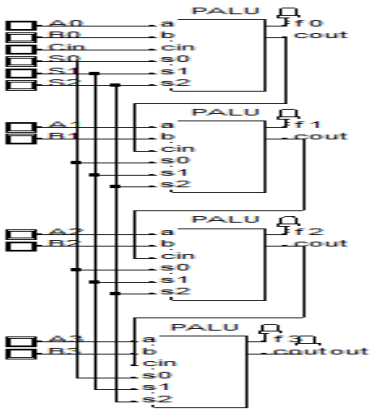

Fig 7. Schematic of 4-bit ALU

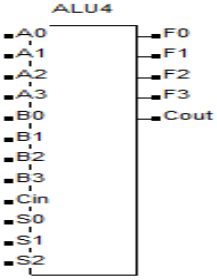

Fig .8.Symbol of 4-bit ALU

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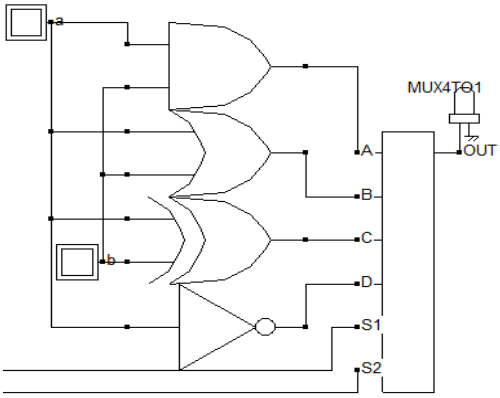

Fig .9. Block diagram of multiplexer logic at the output stage

This paper presents a new approach using concept of Gate Diffusion Input Technique to design an arithmetic and logic unit. In an ALU, for appropriate selection of input to perform particular operation and for obtaining output accordingly multiplexer is the most applicable device. In earlier designs of ALU, the multiplexer unit is either implemented by conventional CMOS logic or by pass transistor logic which proven to have high power consumption. The approach gives better result than previous designs in terms of power consumption, propagation delay as well as area.

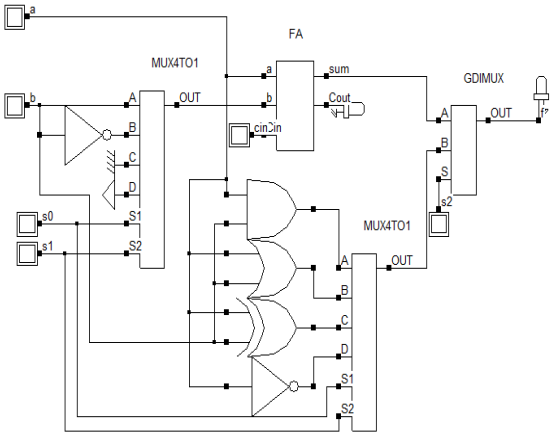

Figure 10. Schematic of 1-bit ALU

V. SIMULATONS RESULTS AND ANALYSIS

This section describes performance of the proposed design using Microwind3.5 and DSCH 3.5 tool on 65nm technology. The simulated output of 4-bit ALU as shown in following figures

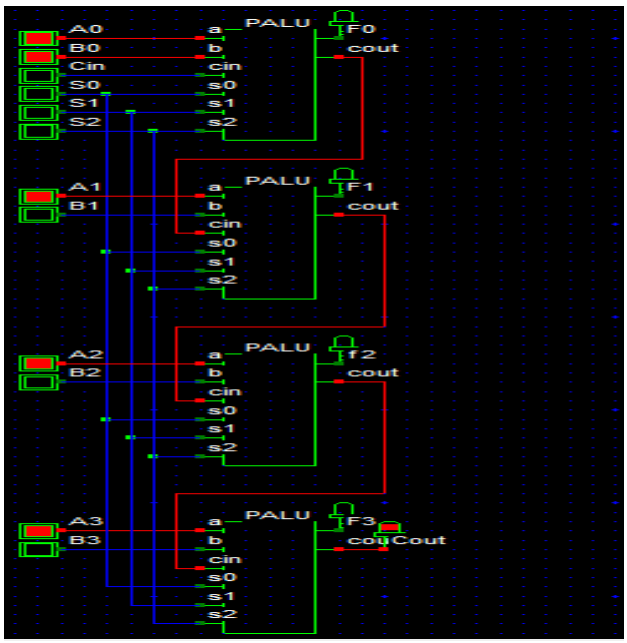

Fig 11. Schematic of 4-Bit ALU

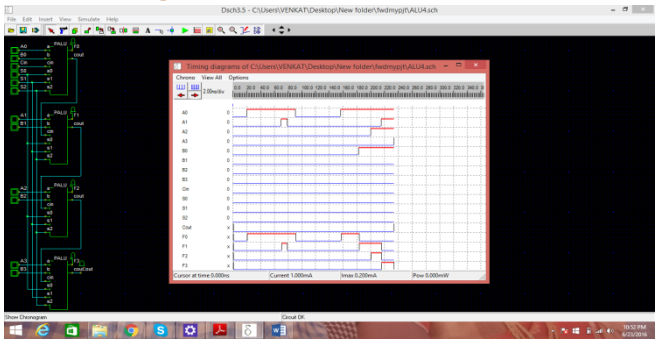

Fig 12.Timing Diagram of 4-Bit ALU

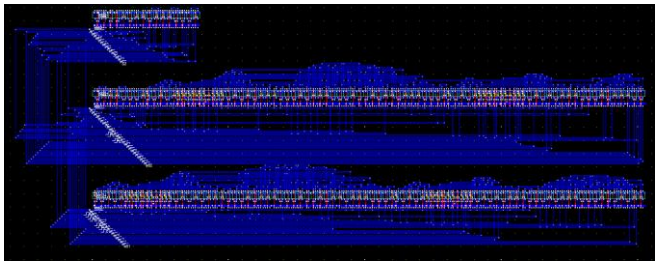

Fig 13.Layout of 4-Bit ALU

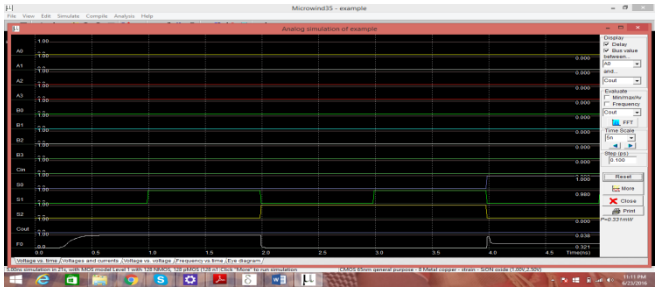

Fig 14. Simulated Output of 4-Bit ALU

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TABLE III. ANALYSIS RESULT OF DIFFERENT BLOCK OF ALU

S. No.	Design	Cell	Power (μW)	No. of Trans-istor
1	CMOS	2x1 MUX	4.6073	6
2		4x1MUX	15.123	18
3		Conventiona l Full adder	16.675	28
4	Pass Transistor Gate	2x1 MUX	1.6079	4
5		4x1MUX	4.225	8
6		Full adder	11.998	24
7	GDI	2x1 MUX	1.394	2
8		4x1MUX	2.987	6
9		Full adder	10.190	10

TABLE IV. POWER CONSUMPTION OF 4-BIT ALU

S.No.	Design	No. of Transistors	Power(μW)
1	ALU with CMOS Gate	592	4204.5
2	ALU with transmission Gate and 10 Transistor full adder	416	1197.5
3	Proposed ALU with GDI based Full adder	232	1030.5

VI. CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by P = CLf VDD2. The power supply is directly related to dynamic power. The numbers of power supply to ground connections are reduced in GDIimplementation which reduces the dynamic power consumption. This work presents a 4-bit ALU designed in250nm technology for low power and minimum area withed technique. Various topologies of multiplexer and full adder implementation is studied and compared. The 2x1multiplexer, 4x1 multiplexer, 1-bit full adder with 10-transistors designed using GDI technique is chosen for lowering power consumption and minimum possible area. Power dissipation, propagation delay and the number of transistors of ALU were compared using CMOS, nMOSPTL and GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques.

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