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A New Approach to Design Fault Coverage Circuit with Efficient Hardware Utilization for Testing Applications

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Abstract:
A New Fault Coverage Test Pattern Generator using a Linear Feedback Shift Register (LFSR) called FC-LFSR can perform Fault Analysis and reduce the power of a circuit during test by generating three intermediate patterns between the random patterns by reducing the Hardware Utilization. The Goal of having Intermediate patterns is to reduce the transitional activities of Primary Inputs (PI), which eventually reduces the switching activities inside the Circuit under Test (CUT), and hence power consumption is reduced without any penalty in the hardware resources. The experimental results for c17 benchmark, with and without fault confirm the fault coverage of the circuit being tested.

Keywords:
LFSR, Optimization, Low Power, Test Pattern Generation, BIST.

I. INTRODUCTION:

Power dissipation is a challenging problem for today's System-on-Chips (SoCs) design and test. The power dissipation in CMOS technology is either static or dynamic. Static power dissipation is primarily due to the leakage currents and contribution to the total power dissipation is very small [1]. The dominant factor in the power dissipation is the dynamic power, which is consumed when the circuit nodes switch from 0 to 1. During switching, the power consumed due to the short circuit current flow and the charging of load capacitances given by equation:

$$P = 0.5VDDE(sw)\,CLFCLK \quad (1)$$

Where VDD is supply voltage, E(sw) is the average number of output transitions per 1/ FCLK, FCLK is the clock frequency and CL is the physical capacitance at the output of the gate. Dynamic power dissipation contributed to total power dissipation. From the equation, dynamic power depends on three parameters: supply voltage, clock frequency and switching activity. To reduce the dynamic power dissipation by using first two parameters only at the expense of circuit performance. However, power reduction using the switching activity does not degrade the performance of the circuit. Power dissipation during testing is one of most important issue. Latest advances in semiconductor technology have led to transistor scaling of transistor dimensions, allowing a large number of devices to be fabricated on a single chip [2].

The high integration has made power consumption. In addition, the ever-increasing utilization of portable computing devices and communication systems requires low power dissipation in VLSI circuits. The power dissipation of a system in test mode is more than in normal mode. Low correlation between consecutive test vectors (e.g. among pseudorandom patterns) increases switching activity and eventually power dissipation in the circuit. The same happens when applying low correlated patterns to scan chains. Increasing switching activity in scan chain results in increasing power consumption in scan chain and combinational block.

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The extra power (average or peak) can cause problems such as instantaneous power surge causes circuit damage, formation of hot spots, difficulty in performance verification and reduction of the product yieldand lifetime. Large and complex chips require a huge amount of test data and dissipate a significant amount of power during test, which greatly increases the system cost [3]. There are many test parameters should be improved in order to reduce the test cost. Parameters include the test power, test length (test application time), test fault coverage, and test hardware area overheadAutomatic test equipment (ATE) is the instrumentation used in external testing to apply test patterns to the CUT, to analyze the responses from the CUT, and to mark the CUT as good or bad according to the analyzed responses. External testing using ATE has a serious disadvantage, since the ATE(control unit and memory) is extremely expensive and cost is expected to grow in the future as the number of chip pins increases.

As the complexity of modern chips increases, external testing with ATE becomes extremely expensive. Instead, Built-In Self-Test (BIST) is becoming more common in the testing of digital VLSI circuits since overcomes theproblems of external testing using ATE. BIST test patterns are not generated externally as in case of ATE. BIST perform self-testing and reducing dependence on an external ATE. BIST is a Design-for-Testability (DFT) technique makes the electrical testing of a chip easier, faster, more efficient and less costly [4]. The important to choose the proper LFSR architecture for achieving appropriate fault coverage and consume less power. Every architecture consumes different power for same polynomial.

II. PATTERN GENERATOR:

The BIST contains two major components: test patterngenerator and response checker. Both of these components use Linear Feedback Shift Register (LFSR) [5].

The paperdescribed the three different pattern generation techniques byusing LFSR can be designed to reduce the powerconsumption during test in the following ways. A digital pattern generator is a piece of electronic test equipment or software used to generate digital electronics stimuli. Digital electronics stimuli are a specific kind of electrical waveform varying between two conventional voltages that correspond to two logic states (‘low state’ and ‘high state’, ‘0’ and ‘1’). The main purpose of a digital pattern generator is to stimulate the inputs of a digital electronic device. For that reason, the voltage levels generated by a digital pattern generator are often compatible with digital electronics I/O standards – TTL, LVTTL, LVCMOS and LVDS, for instance. Digital pattern generators are sometimes referred to as ‘pulse generator’ or ‘pulse pattern generator’, which may be able to function as digital pattern generators as well [6]. Hence, the distinction between the two types of equipment may not be clear.

A digital pattern generator is a source of synchronous digital stimulus; the generated signal is interesting for testing digital electronics at logic level - this is why they are also called 'logic source'. A pulse generator is of purpose to generate electrical pulse of different shapes; they are mostly used for tests at an electrical or analog level. Another common name for such equipment is 'digital logic source' or 'logic source'. Digital pattern generators are today available as stand-alone units, add-on hardware modules for other equipment such as a [logic analyzer] or as PC-based equipment. Stand-alone units are self-contained devices that include everything from the user interface to define the patterns that should be generated to the electronic that actually generates the output signal. Some test equipment manufacturers propose pattern generators as add-on modules for logic analyzers (see for example the PG3A module for Tektronix' TLA7000 series of logic analyzers) [7]. In this case, the pattern generator is the 'generation counterpart' to the analysis functionality offered by logic analyzers.

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PC-based digital pattern generators are connected to a PC through peripheral ports such as PCI, USB and/or Ethernet (see for example the 'Wave Generator Xpress' from Byte Paradigm, connected through USB). They use the PC as user interface for defining and storing the digital patterns to be sent. As integrated circuit, feature size continues to shrink and wireless and portable devices grow, power consumption not only becomes one of the key issues to be considered during functional operation, but also has to be addressed during manufacturing tests. High power consumption during the functional operation implies:

- Higher design and manufacturing costs due to the extra effort to calibrate power grids in order to meet the power supply requirement.
- Higher system costs due to packaging and cooling requirements.
- Shorter device life cycle and lower device reliability.
- Shorter battery life for portable devices.

III. IMPLEMENTATION OF BIST:

The reduction of the power consumption in a test-per-clock BIST environment is commonly achieved by reducing the switching activity in the CUT. Furthermore, it has been demonstrated in [5] that the switching activity in a time interval (i.e.the average power) dissipated in a CUT during BIST is proportional to the transition density at the circuit inputs. Thereby, several low power test pattern generators have been proposed to reduce the activity at circuit inputs (see above description in part 2.2). Among these techniques, the DS-LFSR proposed in [5] consists in using two LFSRs, a slow LFSR and a normal speed LFSR, as TPG. Inputs driven by the slow LFSR are those which may cause more transitions in the circuit. Although this technique reduces the average power consumption while maintaining a good fault coverage level, the peak power consumption cannot be reduced in practice (a full bit changing may occur at circuit inputs every d clock cycles where d = normal clock speed / slow clock speed).

This point represents a severe limitation of the method as the peak power consumption is a critical parameter that determines the electrical limits of the circuit and the packaging requirements. A typical BIST architecture consists of Test Pattern Generator (TPG) usually implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register(MISR), CUT and BIST control unit as shown in figure 1.

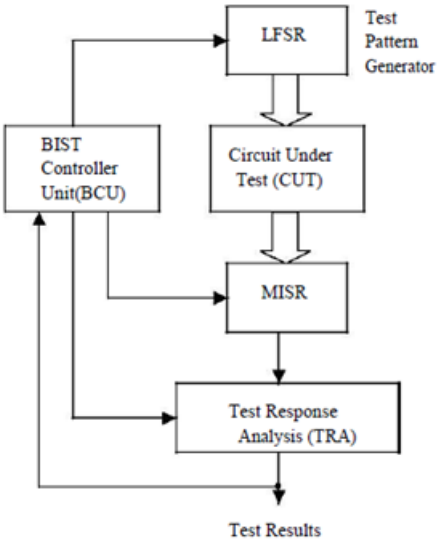

Figure 1: BIST Architecture

CUT: It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (P0) delimit it.

TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.

MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures with every small probability of alias.

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TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not.

BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs.

In BIST, LFSR generates pseudorandom test patterns for primary inputs (PIs) or scan chains input. MISR compacts test responses received from primary output or scan chains output. Test vectors applied to a CUT at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The result in more switching's and power dissipation in test mode. The low power/energy BIST technique proposed in this paper is based on a modified clock scheme for the pseudo-random TPG. Basically, a clock whose speed is half of the normal speed is used to activate one half of the D flip-flops in the TPG (i.e. a modified LFSR) during one clock cycle. During the next clock cycle, the second half of the D flip-flops is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with a master clock CLK and have the same but shifted in period.

The clock CLK is the clock of the circuit in the normal mode and has a period equal to T. The basic scheme of the proposed low power test pattern generator with the corresponding clock waveforms are depicted in Figure 1. As one can observe, a test vector is applied to the CUT at each clock cycle of the test session. However, only one half of the circuit inputs can be activated during this time. Consequently, the switching activity in a time interval (i.e. the average power) as well as the peak power consumed in the CUT are minimized. Moreover, the power consumed in the TPG is also minimized since only one-half of the D flip-flops in the TPG can be activated in a given time interval.

Another important feature of the proposed solution is that the total energy consumption during BIST is reduced since the test length produced by the modified LFSR is roughly the same than the test length produced by a conventional LFSR-based TPG to reach the same or sometimes a better fault coverage.

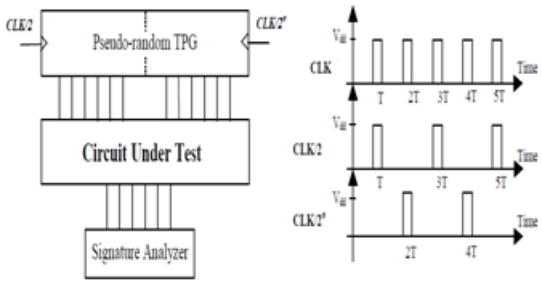

Figure 2: Basic scheme of the low power test pattern generator

The low power TPG:

The idea behind the use of such a low power TPG is to reduce the number of transitions on primary inputs at each clock cycle of the test session, hence reducing the overall switching activity generated in the CUT. Let us consider a CUT with n primary inputs. A n-stage primitive polynomial LFSR with a clock CLK would be used in a conventional pseudorandom BIST scheme. Here, we use a modified LFSR composed of n D-type flip-flops and two clocks CLK/2 and CLK/2_ , and constructed as depicted in Figure 2 (n=6 in the example of Figure 2).

As one can observe, this modified LFSR is actually a combination of two n/2-stage primitive polynomial LFSRs, each of them being driven by a single clock CLK/2 or CLK/2_ . The D cells belonging to the first LFSR (referred to as LFSR-1 in the sequel) are interleaved with the cells of the second LFSR (referred to as LFSR-2 in the sequel), thus allowing to better distribute the signal activity at the inputs of the CUT.

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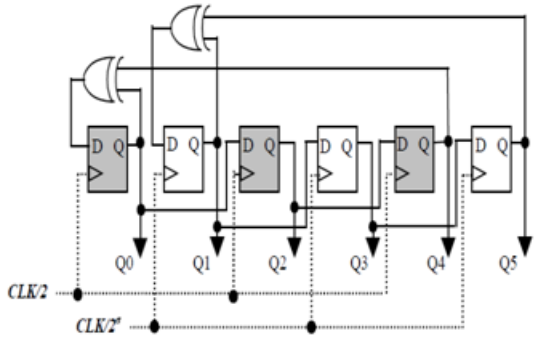

Figure 3: An example of the modified LFSR TPG

In order to better describe the functioning of the low power TPG, the timing diagram of the test sequence generated by the example TPG shown in Figure 2 is reported in Table 1. Assume that the seed <001> has been chosen for both LFSRs, such that the first vector applied to the CUT at time T is <100001>. Only LFSR-1 is active during the first clock cycle (LFSR-2 is in stand-by mode).

This is illustrated in the two last columns of Table 1 in which a8 grey cell represents the active LFSR in the corresponding clock cycle. During the next clock cycle, LFSR-2 is active (LFSR-1 is in stand-by mode) and vector <110000> is applied to the CUT. The advantage of the modified LFSR composed of two interleaved n/2-stage LFSRs (over a simpler structure composed of two separated n/2-stage LFSRs) is that it allows to better distribute the signal activity at the circuit inputs during the BIST session [8].

This is particularly important for circuits in which the input cones of the primary outputs are highly non-overlapping. In this case, two separated LFSRs would activate only one part of the circuit in a given time interval, instead of the whole circuit with the proposed structure in which two LFSRs are interleaved. Shorter test lengths to reach a target fault coverage can hence be predicted with the proposed interleaved LFSR structure.

IV. IMPLEMENTATION OF LOW TRANSITION TEST PATTERN:

The basic idea behind low power BIST is to reduce the PI activities. The paper proposes a new transition test pattern generation technique, which generates three intermediate test patterns between each two consecutive random patterns generated by a conventional LFSR. The proposed test pattern generation method does not decrease the random nature of the test patterns. The technique reduces the PI‟s activities and eventually switching activities in the circuit under test. Let us assume that Ti and Ti+1are two consecutive test patterns generated by a pseudorandom pattern generator (e.g. a conventional LFSR). The new low transition LFSR (LTLFSR)generates three intermediate patterns (Ti1, Ti2and Ti3) between Ti and Ti+1.

The total number of signal transition occurs between these five vectors are equivalent to the number of transition occurs between the two vectors. Hence, the power consumption is reduced. Additional circuit is used for few logic gates in order to generate three intermediate vectors. The area overhead of the additional components to the LFSR is negligible compared to the large circuit sizes. The three intermediate vectors (Ti1, Ti2and Ti3)are achieved by modifying conventional flip-flops outputs and low power outputs.

V. IMPLEMENTING ALGORITHM FOR LT-LFSR

The proposed approach consists of two half circuits. The algorithm steps says the functions of both half circuits is

Step1: First half is active and second half is idle and gives out is previous, the generating test vector is Ti.

Step2: Both halves are idle First half sent to the output and second half’s output is sent by the injection circuit, the generating test vector is Ti1.

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Step3: Second half is active First half is in idle mode and gives out as previous, the generating test vector is Ti2.

Step4: Both halves are in idle mode, First half is given by injection circuit and Second half is same as previous, the generating test vector is Ti3.

After completing step 4 again goes to step1 for generating test vector Ti+1.The first level of hierarchy from top to down includes logic circuit design for propagation either the present or next state of flip- flop to second level of hierarchy. Second level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output which provides more power reduction compared to having only one of the RInjection and Bipartite LFSR techniques in a LFSR due to high randomness of the inserted patterns.

VI. RESULTS:

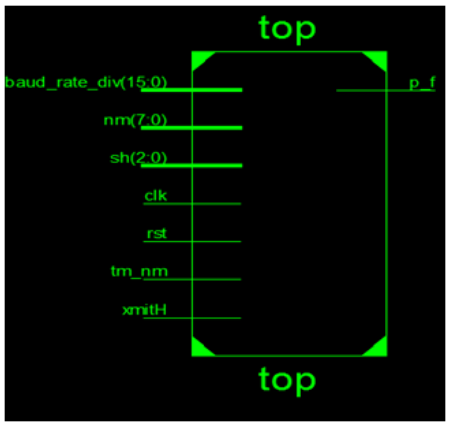

Figure 4: RTL Schematic for Top Module

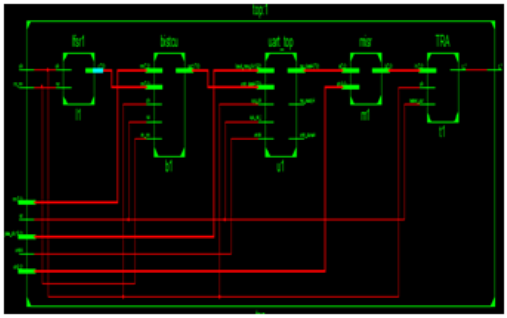

Figure 5: RTL Schematic for Detailed Architecture

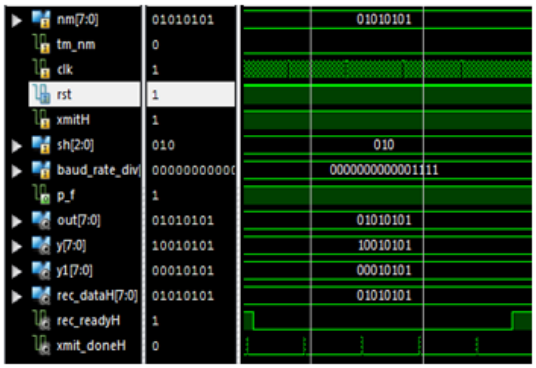

Figure 6: Simulation Results for Proposed System (Normal Mode)

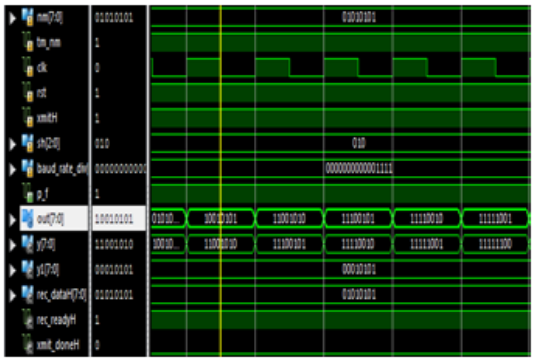

Figure 7: Simulation Results for Proposed System (Test Mode)

VII. CONCLUSION:

The proposed approach is a new low power pattern generation technique is implemented using a modified conventional LFSR. Comparisons of the number of test patterns (NP) required to hit target fault coverage (FC), the average and peak power of LT-LFSR, LPATPG and modified clock scheme. The used 50 different seeds for 10 different polynomials in the experiment. The performance of LT-LFSR is seed and polynomial-independent. The required number of patterns provides target FC does not quadruples, and preserving randomness. By using this low transition test pattern generator using LFSR for Test Pattern Generation (TPG) technique we conclude that power dissipation is reduced during testing. The transition is reduced by increasing the correlation between the successive bits, reduces the average and peak power of a circuit during the test mode.

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By increasing the correlation between the test patterns in the CUT and eventually the power consumption is reduced. Additional intermediate test patterns inserted between the original random patterns reduces the PI activities, average and peak power of combinational and sequential circuits during the test mode with do not effect on FC.

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