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High efficiency design of Current fed topology-based inverter

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Abstract –

A new modular DC-DC converter topology. As modular topology, the converter can be used for several energy sources. Each converter module is based on a three-level DC-DC converter, which contains two output capacitors. The first module shares the second capacitor in common with the first capacitor of the next module. In this way, N-module can be utilized for N-energy source. Recently developed ZSI and its derivatives overcome these problems by allowing shoot-through and providing output AC voltage with buck-boost capability. This paper proposes a CurrentFed DC/DC Topology (CFT) based inverter which shows similar gain characteristic and advantages as the ZSI. The proposed inverter requires only one LC-pair which is one less than the impedance network of ZSI. The proposed inverter is derived from CFT. Steady-state analysis and implementation of the proposed inverter are described. The PWM control strategy of the inverter is explained. An experimental prototype is built to validate the proposed inverter circuit. A 127 V (rms) AC-output is obtained from 353 V DC-link with 35.3 V DC-input and a 5.18 V (rms) ACoutput is obtained from 57.6 V DC-link voltage with 28.8 V DC-input to verify boost and buck mode of operation, respectively.

Index Terms- Current-Fed Switched Inverter, SBI, Shoot through, EMI.

I. Introduction

In the recent decades the power generation sector has seen large penetration by renewable energy systems (RES) mainly due to rapid depletion of fossil fuels and technological growth in renewable sector. Renewable sources like solar photovoltaic, fuel cell, etc., are low voltage sources and thus needs high boost inversion to meet the conventional line voltage of 110 V/ 230 V 50/60 Hz AC. Series connection of several sources is another available option but it can cause poor harvest of available energy when solar insolation is locally intermittent (partial shading condition) in the case of solar PV. As AC output of the traditional voltage source inverter (VSI) is always lower than the input DC-link voltage, a front-end DC-DC boost converter or a back-end high step-up transformer is added to get the necessary boost inversion.

Inverters with step-up transformers having a high turnsratio are generally bulky and modularity of the design is lost due to its weight and space requirement. Thus, the alternate way is to go for a transformer-less, more efficient and modular solution [1]-[3]. In transformer-less applications, conventionally, an inverter is cascaded with a high boost DC/DC converter [4]. Maximum gain of conventional boost, cascaded boost converters, or quadratic boost converters is limited which is achieved at extremely high duty-ratio (D), i.e., at near unity dutyratio.

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When a boost converter operates at near unity dutyratio, the diode and the output capacitor has to sustain a current of high amplitude with very small pulse-width. This results in severe reverse recovery of the diode, increased conduction loss and production of electromagnetic interference (EMI). Also, at extreme duty-ratio operation, regulation of output voltage during load change becomes difficult as an increase in duty-ratio will result in decreased gain after peak gain point [5]. Converter with coupled inductor can deliver high gain without extreme duty-cycle operation, but the switching surge voltage due to leakage of the inductors result in associated losses and requirement of high-voltage-rated devices. Use of regenerative snubber or active voltage clamp circuits [6], [7] can prevent production of switch surge and minimize leakage loss but these methods increase circuit complexity and extra loss in the snubber or clamp circuit. Single switch high gain DC/DC converters using four terminal switched cells and switched-capacitor cells are presented in [8]. Though high gain at reduced switch stress is obtained, the number of passive circuit components and diodes are higher than the conventional boost topologies.

One of the major problems associated with the two-stage DC-AC conversion is that the inverter may fail due to electromagnetic noise (EMI) [9]. EMI can cause shoot-through of inverter leg leading to flow of short circuit current, and damaging the inverter switches [10]. DC/DC converters which operate at near-unity duty-ratio are more prone to create EMI due to short pulsed current [11-13]. Thus, conventional VSI needs dead-time compensation circuit. Introducing dead-time in the switching signal introduces waveform distortion which again requires complex dead-time compensation circuitry to nullify the distortion.

II. REVIEW OF THE CURRENT FED SWITCHED INVERTER TOPOLOGY

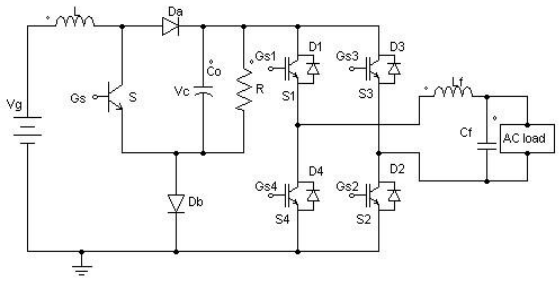

Fig 1: CFSI topology

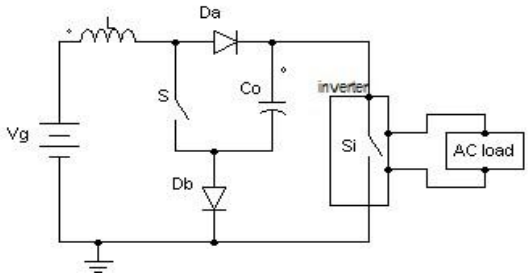

Fig 2: Simplified CFSI topology

The current fed switched inverter [14] is shown in Fig. 1. The main components of CFSI are one active switch (S), two diodes (D_a, D_b), one capacitor (C_o) and one inductor (L) and which are connected in between voltage source V_g and the inverter bridge. A low pass LC filer is used at the output of the inverter bridge to filter the switching frequency components in the inverter output voltage.

The CFSI topology inserts the shoot- through state (gating upper and lower switches of a phase leg) in its operation to boost the input voltage V_g to V_c. Therefore, the inverter is able to buck and boost the input voltage to a desired output voltage. Since the shoot-through state is present, reliability of the inverter is improved. Thus, inverter provides efficient single stage dc-ac inversion as well as buck boost power conversion. Similar to ZSI and SBI, inverter input is a switched voltage.

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Consider the Fig. 2 for better understanding the operation of the inverter. Here, the H-bridge inverter is represented by a single switch Si and turning on of Si represents the shoot-through state. Initially, the capacitor C_o is charged to the voltage V_g and the initial inductor current is zero before switching signals are started [15]. The two operation intervals of

CFSI are

(1) shoot-through interval

(2) non-shoot-through interval

During shoot-through interval (D interval), switches S and Si (S_1-S_4 or S_3-S_2) are turned on and diodes D_a and D_b become reverse biased as they are now in parallel with C_o. In this interval, source V_g and capacitor C_o charge inductor L together. Equivalent circuit of CFSI in D interval is shown in the Fig 3. Equations of inductor voltage and capacitor current in D interval are given in (1) & (2).

$$v_L = V_g + V_C \quad (1)$$

$$i_c = -I_i \quad (2)$$

During non-shoot-through interval (D' interval), switches S and Si are turned off, which forces diodes D_a and D_b to turn on. Inductor charges C_o and power is delivered to the ac load through the inverter. Here, turning off switch Si denotes the power interval or zero interval of the inverter (turning on of switches S_1-S_2 or S_4-S_3). Fig 4 shows the equivalent circuit of CFSI in D' interval and equations of inductor voltage and capacitor current in D' interval are given in (3) & (4).

$$v_L = V_g - V_C \quad (3)$$

$$i_c = I_L - I_i \quad (4)$$

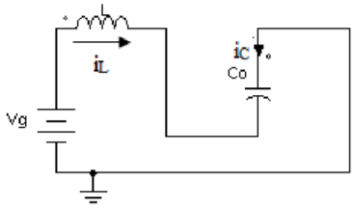

Fig 3: equivalent circuit of CFSI in D interval

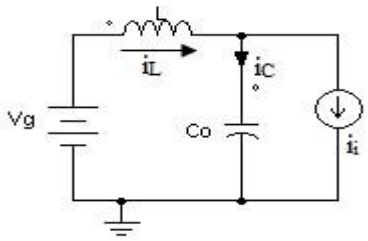

Fig 4: Equivalent circuit of CFSI in (1-D) interval

In steady state equilibrium, using inductor volt-second balance and capacitor charge-second balance, we get

$$B_{CFSI}(D) = \frac{V_C}{V_g} = \frac{1}{1-2D}$$

$$I_L = \frac{1-D}{1-2D} I_i \quad (5)$$

From equation (5) it is clear that this topology gives maximum gain at duty cycle close to 0.5. The equation of peak ac output is

$$V_{ACpeak} = M \times V_c = \frac{M}{1-2D} V_g \quad (6)$$

where M is the modulation index of the inverter.

The relation between duty ratio and modulation index is given by

$$D < 1 - M \quad (7)$$

So, the value of M is depending on the value of D. To avoid this limitation of CFSI, the new topology is proposed in this paper which is named as Improved Current Fed Switched Inverter.

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III. IMPROVED CURRENT FED SWITCHED INVERTER

In order to improve the modulation index value, a combination of switch-diode-capacitor is connected in front of the H- bridge inverter as shown in figure 5. The shoot-through state is avoided and the switch ST is capable of doing the same function of the shoot-through state. Initially, the capacitor C_o is charged to the voltage V_g and the initial inductor current is zero before switching signals are started. The two operating intervals of the new topology are

1. D interval
2. (1-D) interval

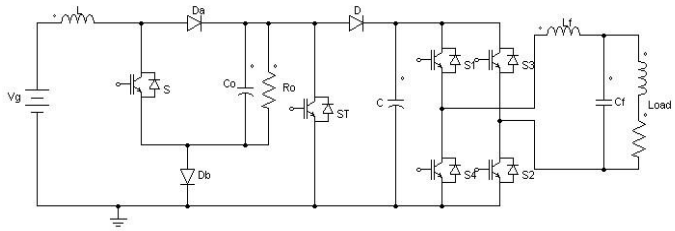

Fig 5: improved current fed switched inverter topology

During D interval, switches S and ST are ON state and D1 and D2 become reverse biased as they are now in parallel with C. In this interval, source V_g and capacitor C_o charge inductor L together. In D interval, either S1 & S2 or S3 & S4 are turned on and capacitor C is feeding the load. During (1-D) interval switches *S* and *ST* are turned off, which forces diodes D1 and *D2* to turn on, and the inductor charges C_o and power are delivered to the ac load through the inverter. There is no zero interval is present in the inverter. The gain is same as that of CFSI. The inductor current ripple and capacitor voltage ripple are given by

$$\Delta i_L = \frac{V_g + V_c}{L} D T_S$$

$$\Delta v_c = \frac{I_L}{C} D T_s$$

Sine PWM technique is used here for controlling the switches. Figure 6 shows the generation of the PWM control signals of the proposed inverter. Similar to unipolar sine-triangle PWM, gate signals G_{s1} and G_{s2} are generated by comparing the sinusoidal modulation signals $V_m(t)$ and $-V_m(t)$ with high-frequency carrier signal $V_{\text{tri}}(t)$. In order to generate the switching signals for the switches S and ST by comparing V_{ST} and $-V_{ST}$ with $V_{\text{tri}}(t)$. The relation between the V_{ST} and D is given by

$$D = \left(1 - \frac{V_{ST}}{\hat{V}_{tri}}\right) \quad (10)$$

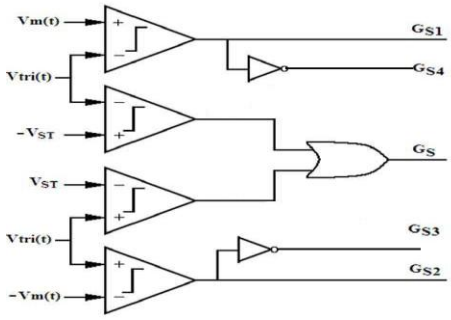

Fig 6. Generation of the PWM control signals

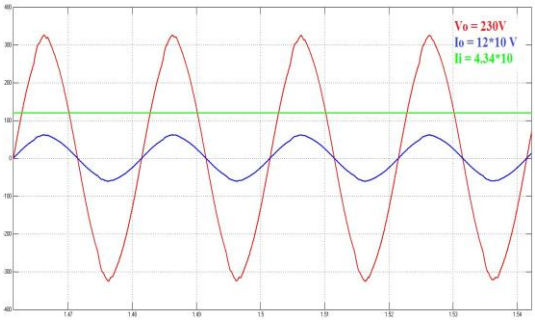

Fig 7: simulation waveforms of output voltage, output current and input current

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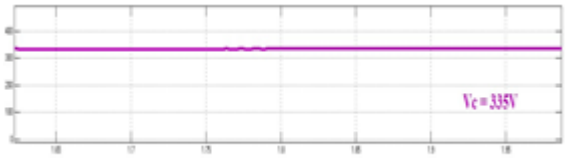

Fig 8: dc-link voltage Vc

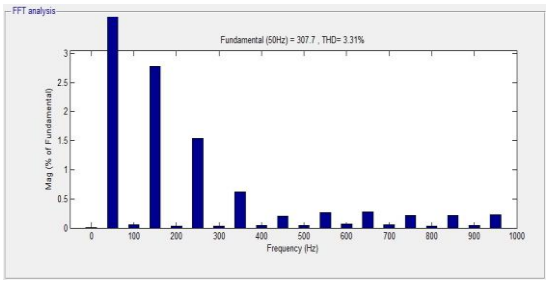

Fig 9: THD and harmonic order of output voltage

IV. SIMULATION RESULTS

A 12V input voltage and 230V output voltage improved current fed switched inverter circuit with power rating of 1000VA is designed and simulated to verify the proposed concept. The simulation of the improved current fed switched inverter (fig. 5) is carried out in MATLAB/ SIMULINK. The parameters are used as follows: input voltage V_g =12V, V_{out}=230V, modulation frequency f_m=50Hz, carrier frequency f_{tri}=9.5kHz, inductor L=225µH, capacitor C_o=3878µF, output filter inductor L_f=4.6mH, output filter capacitor C_f=10µF. Figure 7 shows the simulation result of improved CFSI. The output voltage is a sinusoidal signal with rms voltage of 230V. The value of D is 0.483 and modulation index is 0.9. The output current obtained is 4.34A. Here, the output current and input voltages are multiplied by a factor of 10 for better visibility. Figure 8 shows the voltage across the capacitor C which is called the dc-link voltage and the value of Vc is 335V. THD and harmonic order of the output voltage is shown in figure 9. The THD content in the output voltage of the proposed inverter is 3.31%.

V. CONCLUSION

Proposed inverter is a single stage high-boost inverter with continuous input which is suitable for the renewable applications. Gain of the inverter is same as that of the ZSI and CFSI. Modulation index of the proposed topology varies from 0 to 1. PWM control strategy is used for the inverter. Simulations results of improved current fed switched inverter are also presented in this paper. Theoretical values are verified by the simulation results.

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