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Design and Synthesis of Reversible Decoder and Encoder Using Verilog HDL

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Abstract

Reversible logic is the arising research for analysis in present era. The aim of this study is to apprehend altered types of combinational circuits like full-adder, full-subtractor, multiplexer and comparator application reversible decoder ambit with minimum breakthrough cost. Reversible decoder is advised application Fredkin gates with minimum Breakthrough cost. There are abounding reversible logic gates like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and abounding more. Reversible logic is authentic as the logic in which the amount achievement curve are according to the amount of ascribe curve i.e., the n-input and k-output Boolean action F(X1, X2, X3,…, Xn) (referred to as (n, k) function) is said to be reversible if and alone if (i) n is according to k and (ii) anniversary ascribe arrangement is mapped abnormally to achievement pattern. The gate has to run advanced and astern that is the inputs can as well be retrieved from outputs. When the accessory obeys these two altitudes again the additional law of thermo-dynamics guarantees that it dissipates no heat. Fan-out and Feed-back are not accustomed in Logical Reversibility.

INTRODUCTION

In present VLSI Technology, Power Consumption has become a very important factor for consideration. By using Reversible Decoder for designing Combinational circuits power consumption is reduced to an optimum when compared to conventional decoder based combinational circuits. Reversible Logic finds its own application in Quantum computing, Nano-technology, optical computing, computer graphics and low Power VLSI. Ralf Launduer told that heat dissipation in circuits is not because of the process involved in the operation, but it is due to the bits that were erased during the process [1]. He introduced that losing of a single bit in the circuit causes the smallest amount of heat in the computation which is equal to KTln2 joules where K is Boltzmann constant and T is Temperature.

The amount of heat dissipated in simple circuits is very small but it becomes large in the complex circuits which imply propagation delay also. Later in 1973 C. H. Bennett described that the Power dissipation due to the bit loss can be overcome if each and every computation in circuit was carried out in reversible manner [2]. Quantum networks are designed of quantum logic gates. As each gate perform a unitary operation, KTln2 Joules energy dissipation wouldn't occur if the computation is carried out in reversible manner.

Thus computation done in reversible manner doesn't require erasing of bits. The amount of heat dissipated in the system holds a direct relationship to the number of bits erased or lost during the computation [3-5]. Currently, energy losses due to irreversibility are dwarfed by the overall power dissipation, but this may change if power dissipation improves. In particular, reversibility is important for nanotechnologies where switching devices with gain are difficult to build [5-8].

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Finally, reversible circuits can be viewed as a special case of quantum circuits because quantum evolution must be reversible. Classical (non-quantum) reversible gates are subject to the same "circuit rules," whether they operate on classical bits or quantum states. In fact, popular universal gate libraries for quantum computation often contain as subsets universal gate libraries for classical reversible computation.

PROPOSED METHOD

REVERSIBLE DECODER OF 4:16

The Design of Combinational and Sequential Circuits has been ongoing in research. Various proposals are given for the design of combinational circuits like adders, subtractors, multiplexers, decoders etc., in the existing method the author has given a novel design of 4x16 decoder whose Quantum Cost is less than the previous design. Replacing fredkin gates for designing 2×4 decoder reversible gates like peres gate, TR gate, NOT gate and CNOT gate are used as shown in figure. The whole design is done using Fredkin, CNOT, Peres gates which give better Quantum Cost when compared to the other reversible Logic gates. The number of gates required to design 4x16 decoder are 18 in which there are 12 fredkin gates, one peres gate, one TR gate, one NOT gate and 3 CNOT gates. The sum of all the quantum costs of each gate gives total quantum cost of 4x16 decoder. Different Reversible Decoder circuits like 2×4, 3×8, 4×16, 5x32, 6x64 are designed using Fredkin Gates (mainly), Feynman gates and Peres gate. Some combinational circuits like comparator adder, subtractor, multiplexers etc., are designed using these decoders. The concept of duplicating a single output to required number of outputs using Feynman gate is introduced where Fan-out was not allowed in reversible computation.

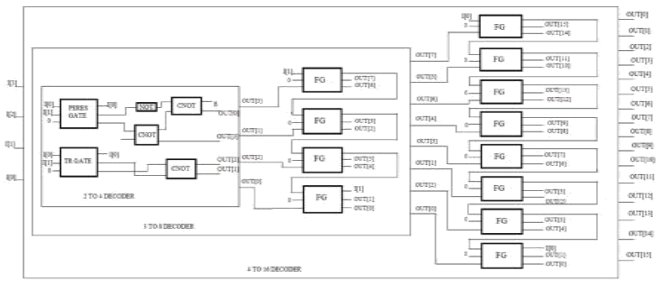

Fig 1: Circuit diagram of Reversible 4×16 decoder

MUITIPLEXER 8:1

Here in place of and, or gates we are using Reversible and , Reversible or gates by using Fredkin gate implemented in Fig 6.

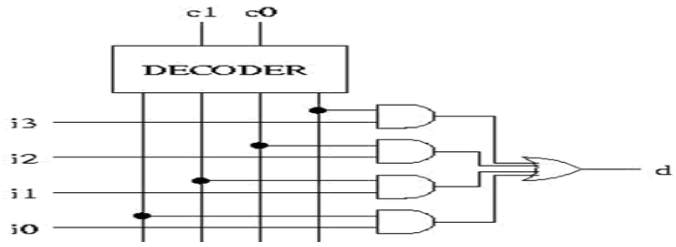

Fig 2: MUX design using Decoder

ADDER

Here also in place of OR gate we are using reversible or gate by using Fredkin gate

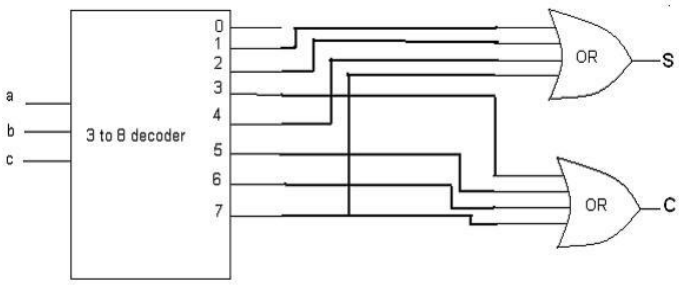

Fig 3: Adder using Decoder

REVERSIBLE ENCODER:

The proposed 16:4 Reversible Encoder is shown in figure. It uses twenty three Feynman gates(FG) and five Fredkin gate(FRG).It has sixteen inputs A,B,C,D,E,F,G,H,I,J,K,L,M,N,O,P and four outputs Y1, Y2, Y3 & Y4 and also has 12 garbage outputs g1, g2, g3, g4, g5, g6, g7, g8, g9, g10, g11, g12. The operation of circuit is given in Table. This proposed 16:4 Encoder has Quantum cost of 48.

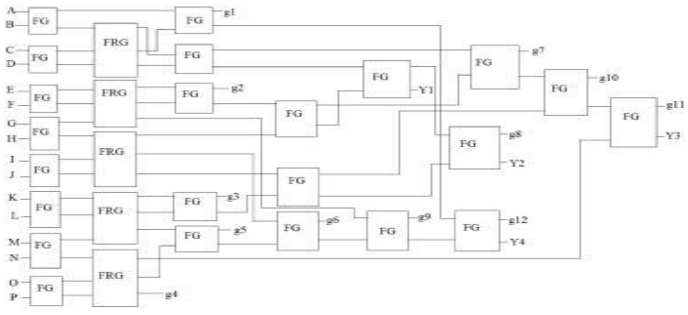

Fig 4: Proposed 16:4 Reversible Encoder

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GENERAL CONCEPT OF ADDER BACKGROUND

Many instructions accommodate add. Load, abundance and annex use adder for abode calculation. Arithmetic instructions use adder for add, subtract, accumulate and divide. There are abounding altered kinds of adders. Due to achievement requirement, a lot of of the accepted top achievement processors apply one of the accepted alongside adders. These alongside adders, such as Backpack Look Ahead (CLA), Brent-Kung Adder (BKA), Kogge-Stone Adder (KSA) and Backpack Baddest Adder (CSA), all acquire commensurable asymptotic achievement I261 proportional to log (N), breadth N is the amount of $.25 of the adder. Accuracy of such circuits can be traded off to advance the ability and acceleration by speculation. Thereby, such adders are referred as inexact speculative adder (ISA). Various optimized versions of such ISA acquire been appear and these works concentrated mostly on acceptable the accurateness of their results.

INEXACT SPECULATIVE ADDER (ISA):

The ISA improves performance, activity ability and absurdity administration through an optimized speculative aisle and with a able dual-direction absurdity advantage technique. A abrupt architecture alignment is presented forth with after-effects and a allusive assay of adder architectures.

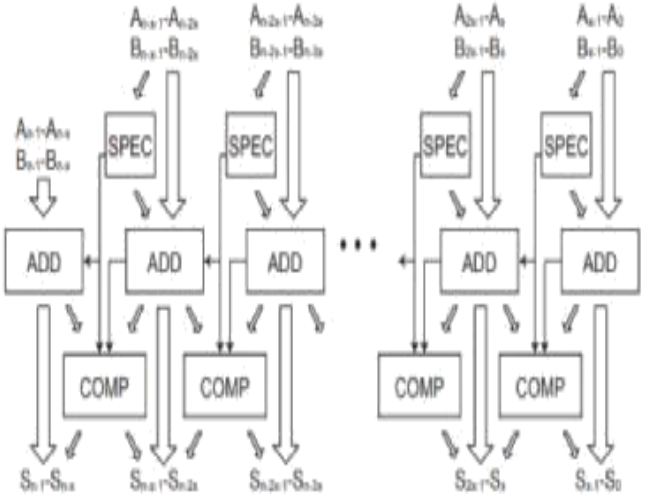

Fig 5: General Block diagram of the Inexact Speculative Adder

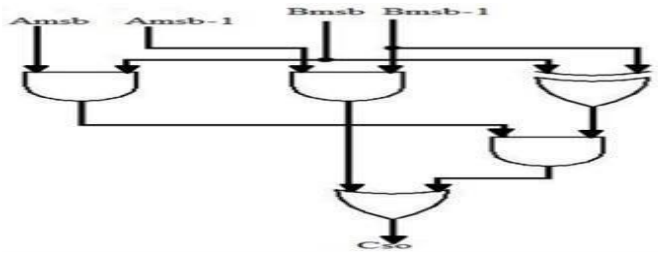

Fig 6: Logic level representation of speculator

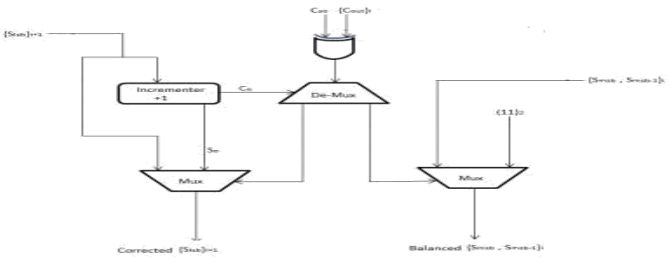

Fig 7: Implementation of the compensator block

Speculative adders accomplishment the actuality that the archetypal backpack advancement alternation of an accession does not amount the accomplished breadth of the adder, authoritative it is accessible to appraisal an average backpack application a bound amount of antecedent stages. Thus, the backpack advancement chain, which is the analytical aisle of the adder, can be breach in two or added beneath paths, adequate constraints over the absolute design, abbreviation affected glitching power, and convalescent the Energy-Delay-Area Product (EDAP) above the speculative bound of exact adders.

The structural diagram of the ISA adder is depicted in Fig. 5. The ISA splits the backpack advancement alternation in assorted paths accomplished concurrently. Anniversary aisle consists of a backpack charlatan block (SPEC), a sub-adder block (ADD) and an absurdity advantage block (COMP). For anniversary SPEC-ADD-COMP path, the SPEC block generates a fractional backpack arresting that the sub-adder ADD uses as a carry-in to accomplish a bounded sum. The COMP block compensates adulterated sums either by acclimation the bounded sum or by abbreviation absurdity consequence as in [3]. The aboriginal speculative path, operating on the atomic cogent $.25 (LSBs) of the adder, does not

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accept neither SPEC nor COMP blocks back it uses anon the ISA carry-in.

THE SPECULATIVE CARRY SELECTION ADDER (SCSA)

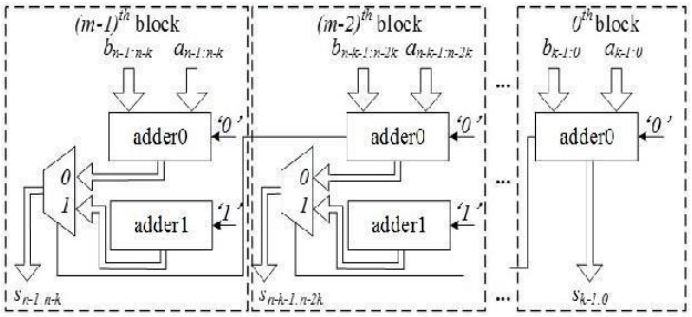

Fig 8: The Speculative Carry Selection Adder (Scsa)

The backpack belief of the SPEC block is generated from a few $.25 in a backpack look- ahead access sourced by either a changeless or a activating input. The latter, acclimated in ETBA, can analogously deliver the errors at the amount of accouterments and adjournment overhead. If a bear alternation covers the abounding SPEC block, the exact backpack cannot be speculated from the fractional artefact and the achievement backpack is estimated at the ascribe backpack value. Long bear sequences are aberrant in the case of compatible ascribe administration [2], appropriately the anticipation of belief accountability decreases by accretion the admeasurements of the SPEC block. The sub- adder ADD calculates block sums locally from the speculated backpack of the SPEC block.

Without compensation, an centralized overflow acquired by an inconsistent backpack could advance to a massive error. Therefore, the COMP block detects those belief faults by comparing the backpack generated from the SPEC with the carry-out advancing from the above-mentioned ADD block.

The COMP block is implemented in amid two bounded ADD blocks. In case of adulterated speculation, it attempts to absolutely actual a accumulation of LSBs of the bounded sum. The abounding alteration consists in incrementing or decrementing the accumulation of LSBs, and is alone accessible if it does not advance to accession centralized overflow. If alteration is not possible, the COMP block can cast a accumulation of the a lot of cogent $.25 (MSBs) of the antecedent sub-adder sum to abbreviate the absurdity magnitude. The accomplished accession arithmetic, illustrated in Fig. 2, is a 5-step process: 1. A carry-in is speculated from a actual abbreviate backpack advancement alternation for anniversary sub-adder block. 2. The sub-adder calculates the bounded sum based on this speculated carry-in. 3. Comparison of the speculated carry-in and the above-mentioned sub adder carry-out allows apprehension of adulterated speculation. 4. In case of amiss speculation, alteration of the bounded sum is attempted. 5. If alteration is not possible, absurdity consequence is bargain by acclimation the above-mentioned sum bits.

ADDERS CHARACTERIZATION

In this breadth we accommodate a assuming of the spatial and timing complication of the advised reversible cessation speculative adders, application either Han-Carlson or Kogge-Stone topologies. Results for non-speculative adders are as well reported, for comparison. This will be accomplished with the advice of simplistic hypotheses on breadth and acceleration of active gates, with the aim of accepting an analytic allegory (albeit approximated) amid the assorted topologies. Accurate ethics of area, acceleration and ability for 65 nm technology will be presented in the next breadth for a quantitative appraisal of reversible cessation speculative adders. Results of absurdity amount assay will aswell be appear at the end of this section.

SPATIAL AND TIMING COMPLEXITY

In adjustment to appraisal adder complexity, we accomplish some simplistic hypotheses We accept that the spatial complication of speculative prefix processing and absurdity alteration is proportional to the amount of active atramentous beef (AO gates). Absurdity apprehension spatial complication is artlessly estimated bold that it is composed by a set of AND gates followed by a timberline of two-input OR to compute the absurdity arresting.

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The carry- select and carry-skip adders accommodate a accommodation amid a carry-ripple and a CLA adder. The n bit slices of a carry-select adder are disconnected into IC blocks of possibly altered lengths. Each block is evaluated conditionally with block-carry-in amount 0 and 1. When the block-carry-in amount to a block has been assigned its final value, it is acclimated to baddest the sum $.25 from one of the two codicillary blocks. At this point in time, the block-carry-out can aswell be evaluated, which in about-face selects the sum $.25 and carry-out for the next block. The added amount of a carry-select adder over a carryripple adder is the alike carry-chain and baddest logic, which is O(n). The analytical aisle for a carry-select adder is the best of the carry-chain in the better block and the carry select chain. The block sizes are called to adjust these two paths: longest carry-chain and carry-select chain. This, in general, will depend on the technology of implementation, which determines factors such as fan-out per gate and the about delays of baddest logic and carry-chain logic. We accept as assemblage gate a basal 2-input gate, such as AND gates and OR gates, while we calculation atramentous beef (AO gates) as two assemblage gates.

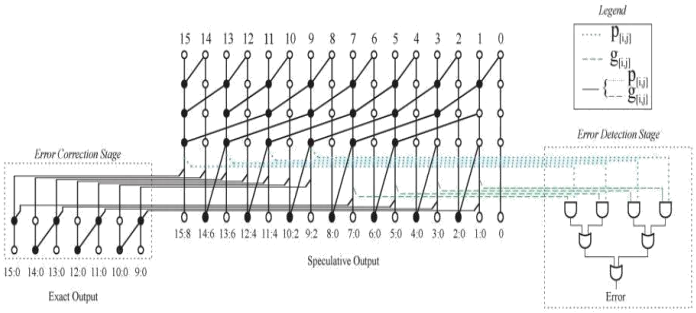

Fig 9: Error alteration and apprehension stages for the speculative Han-Carlson adder

ERROR RATE ANALYSIS

The amount of absurdity anticipation is axiological to accept the abasement of boilerplate accession time acquired by misprediction. In adjustment to appraise absurdity probabilities, the proposed speculative Han-Carlson and the Kogge-Stone topologies accept been apish by application a Monte Carlo access with a 1% about absurdity and a 99% aplomb level.

RESULTS

SIMULATION RESULTS FOR REVERSIBLE DECODER

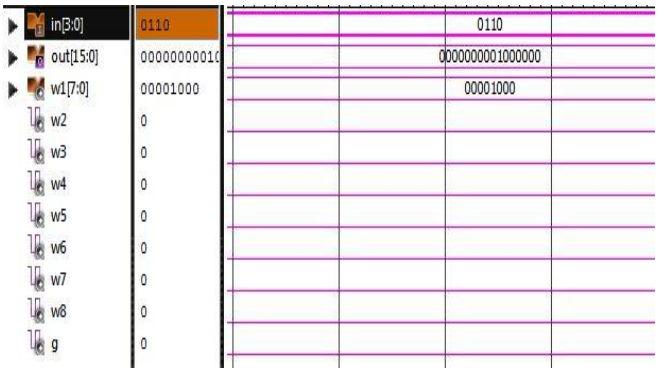

Fig 10: Simulation Results for reversible decoder4x16

SIMULATION RESULTS FOR REVERSIBLE ADDER

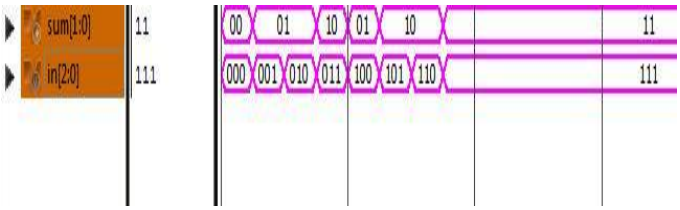

Fig 11: Simulation Results for reversible adder

SIMULATION RESULTS FOR REVERSIBLE MUX8X1

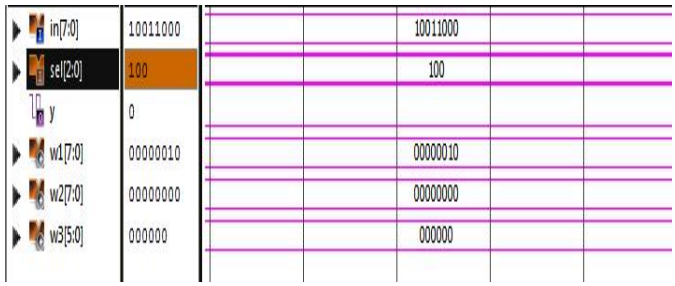

Fig 12: Simulation results for multiplexer

SIMULATION RESULTS FOR REVERSIBLE ENCODER16X4

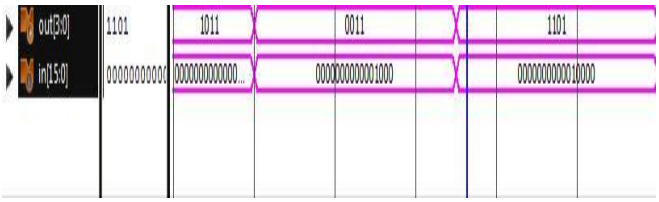

Fig 13: simulation results for reversible encoder

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Synthesis result:

The proposed project is simulated and verified their functionality. Once the functional verification is done, the RTL model is taken to the synthesis process using the Xilinx ISE tool. In synthesis process, the RTL model will be converted to the gate level net list mapped to a specific technology library. Here in this ISE project navigator of Spartan 3E family, many different devices were available in the Xilinx ISE tool. In order to synthesis this designs the device named as "XC3S500E" has been chosen and the package as "FG320".

RTL Schematic Results for Reversible Decoder

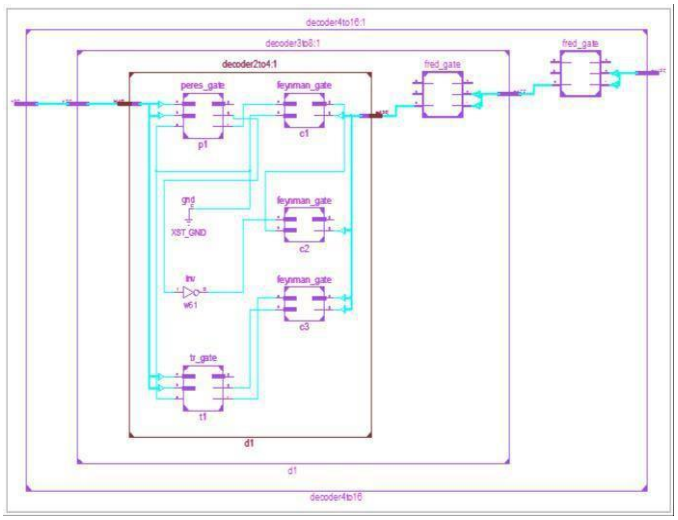

Fig 13: Schematic results of reversible decoder

RTL Schematic Results for Adder

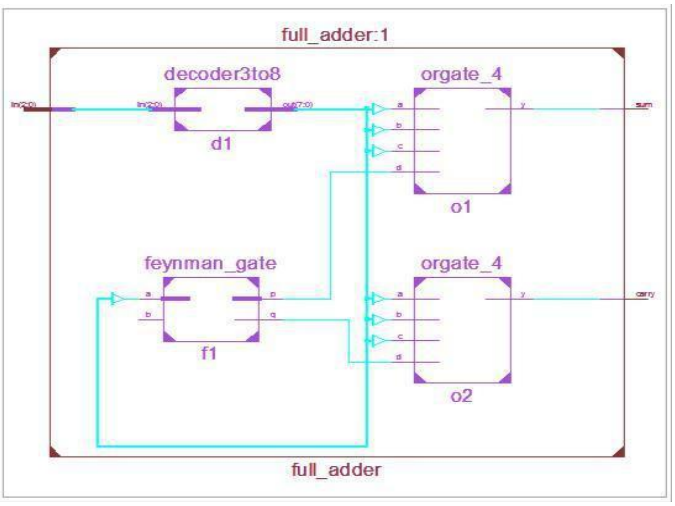

Fig 14: Schematic results for adder

RTL Schematic Results For Multiplexer

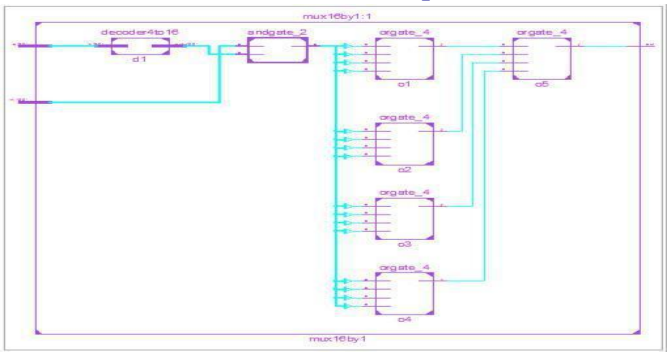

Fig 15: Schematic results for multiplexer

CONCLUSION

In this study, altered combinational circuits like abounding adder, abounding subtractor, multiplexer, comparator circuits complete application reversible decoder are designed. These circuits are advised for minimum breakthrough amount and minimum debris outputs. The adjustment proposed for designing the decoder ambit can be generalized. For example, a 3×8 decoder can be advised application a 2×4 decoder followed by 4 fredkin gates, Similarly a 4×16 decoder can be advised application 3×8 decoder followed by 8 fredkin gates .The speculativeion of accompanying the individual achievement to appropriate amount of outputs is activated to affected the fan-out limitation in reversible logic circuits. This adjustment of designing combinational circuits helps to apparatus abounding agenda circuits with bigger achievement for minimum breakthrough cost.

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