ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

# Implementation of 2 to 4 Line Decoder using DVL and TGL

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***ABSTRACT:***
***In today's world, as the technology is developing so rapidly the designing of the systems are becoming more and more compact. In some systems even if the circuits are not compact; still there is a need of less power consumption. This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Additionally, four new 4–16 decoders are designed by using mixed-logic 2–4 predecoders combined with standard CMOS postdecoder. Low Power is a well established discipline; it has undergone lot of developments from transistor sizing, process shrinkage, voltage scaling, clock gating, etc., to adiabatic logic.***

***This paper aims to elaborate on the recent trends in the low power design. This paper is the review of use of line***

***Keywords:*** ***2-to-4 line decoder, CMOS, Transmission Gate, Pass Transistor logic decoder to reduce power consumption as well as reduce number of transistor and power dissipation.***

## 1. INTRODUCTION:

In the modern age, there is an immense need of applications which consume less power and are small in area. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. Designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products.

### A. Decoder

A decoder is a combinational circuit that decodes the information on n input lines to a maximum of 2n unique output lines. Fig.1 shows the circuit demonstration of 2-4 and 4-16 line decoders. If there are some unused or 'don't care' combinations in the n-bit code, then there will be fewer than 2n output lines. As an design, if there are three input lines. A decoder can generate a maximum of 2n possible minterms with an n-bit binary code. In order to demonstrate further the operation of a decoder, consider the logic circuit diagram in Fig. 1. [1]

A 2-4 line decoder which is implemented using different logic styles called the CMOS, TG, PTL. All that make use of AND and NOT gates. The two inputs to the designed decoder are A and B, whereas $D_0$ through $D_3$ are the four outputs.

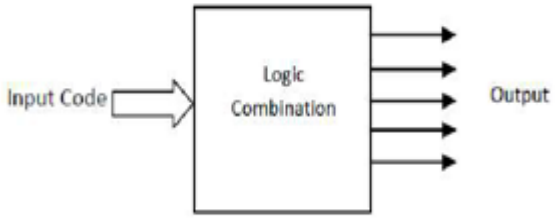


Fig. 1: Conceptual Diagram of Decoder

**Cite this article as:** J. Anusha & O. Homa Kesav, "Implementation of 2 to 4 Line Decoder using DVL and TGL", International Journal & Magazine of Engineering, Technology, Management and Research, Volume 7 Issue 1, 2020, Page 14-19.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

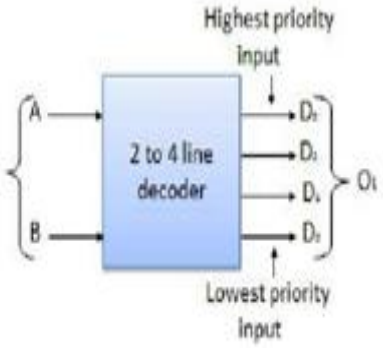


Fig. 2: General block diagram of 2-4 line decoder

Decoder circuit would be an AND gate because the output of an AND gate is "High" (1) only when all its inputs are "High." Such output is called as "active High output". If instead of AND gate, the NAND gate is connected the output will be "Low" (0) only when all its inputs are "High". Such output is called as "active low output". Two basic approaches to reduce power utilization of circuits in scaled technologies are: reducing the dynamic power utilization during the active mode operation of the device and the reduction of leakage current during the stand-by mode. [3]

### The Inverter

Fig. 3 shows the schematic and symbol for a CMOS inverter or NOT gate using one nMOS transistor and one pMOS transistor. The bar at the top indicates VDD and the triangle at the bottom indicates GND. When the input A is 0, the nMOS transistor is OFF and the pMOS transistor is ON. Thus, the output Y is pulled up to 1 because it is connected to VDD but not to GND. Conversely, when A is 1, the nMOS is ON, the pMOS is OFF, and Y is pulled down to '0'.This is summarized in Table 1.

**Table 1: Inverter truth table**

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

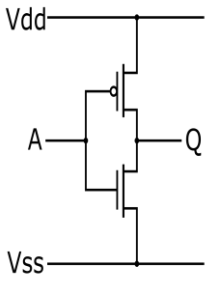


Fig. 3: Inverter schematic AND symbol

### The NAND Gate

Fig. 4 shows a 2-input CMOS NAND gate. It consists of two series nMOS transistors between Y and GND and two parallel pMOS transistors between Y and VDD. If either input A or B is 0, at least one of the nMOS transistors will be OFF, breaking the path from Y to GND. But at least one of the pMOS transistors will be ON, creating a path from Y to VDD. Hence, the output Y will be 1. If both inputs are 1, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be 0.

**Table 2: NAND gate truth table**

| A | B | Pull-Down Network | Pull-Up Network | Y |
|---|---|---|---|---|
| 0 | 0 | OFF | ON | 1 |
| 0 | 1 | OFF | ON | 1 |
| 1 | 0 | OFF | ON | 1 |
| 1 | 1 | ON | OFF | 0 |

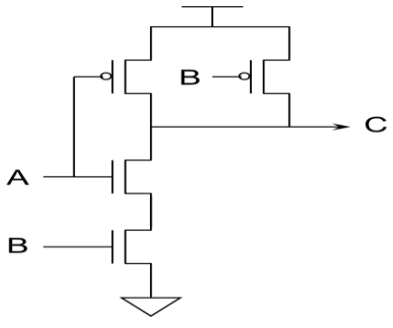


Fig. 4: 2-input NAND gate schematic symbol

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International Journal & Magazine of Engineering, Technology, Management and Research
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### The NOR Gate

A 2-input NOR gate is shown in Fig. 5. The nMOS transistors are in parallel to pull the output low when either input is high. The pMOS transistors are in series to pull the output high when both inputs are low, as indicated in Table 3. The output is never open or left floating.

**Table 3: NOR gate truth table**

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

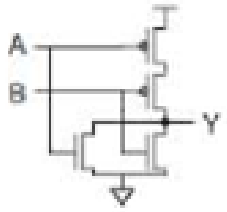


Fig. 5: 2-input NOR gate schematic symbol

### Pass Transistors and Transmission Gates

The strength of a signal is measured by how closely it approximates an ideal voltage source. In general, the stronger a signal, the more current it can source or sink. The power supplies, or rails, (VDD and GND) are the source of the strongest 1s and 0s. An nMOS transistor is an almost perfect switch when passing a 0 and thus we say it passes a strong 0. However, the nMOS transistor is imperfect at passing a 1. The high voltage level is somewhat less than VDD. We say it passes a degraded or weak 1.

A pMOS transistor again has the opposite behavior, passing strong 1s but degraded 0s. The transistor symbols and behaviors are summarized in Fig. 6 with g, s, and d indicating gate, source, and drain. [5] High speed inversion of the pMOS latch is possible only when the gates width of pMOS is sufficiently small. [7]

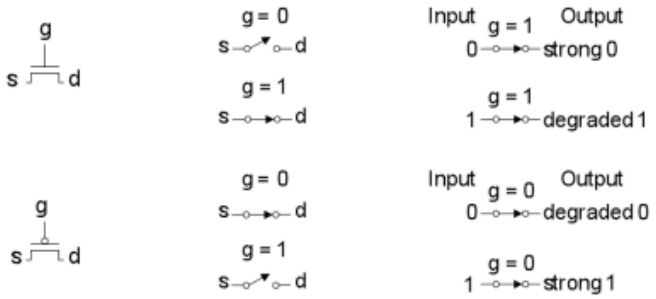


Fig. 6: Pass Transistors strong and degraded outputs

In nMOS integrated circuits there are two typical circuits optimization we might wish to perform. The first is to optimize a critical path for minimum delay without regard to power dissipation. [9]

## 2. LITERATURE REVIEW:

"Digital Electronics: Principles, Devices and Applications", are a comprehensive book covering, in one volume, both the fundamentals of digital electronics and the applications of digital devices and integrated circuits. Chapters 7 and 8 covers, a decoder, is a combinational logic circuit that decodes the information on n input lines to a maximum of 2n unique output lines. Various figures show the circuit representation of 2-to-4, 3-to-8 and 4-to-16 line decoders. If there are some unused or 'don't care' combinations in the n-bit code, then there will be fewer than 2n output lines. As an illustration, if there are three input lines, it can have a maximum of eight unique output lines. If, in the three-bit input code, the only used three-bit combinations are 000, 001, 010, 100, 110 and 111 (011 and 101 being either unused or don't care combinations), then this decoder will have only six output lines. In general, if n and m are respectively the numbers of input and output lines, then $m \leq 2n$. A decoder can generate a maximum of 2n possible minterms with an n-bit binary code. In order to illustrate further the operation of a decoder, consider the logic circuit diagram. This logic circuit implements a 3-to-8 line decoder function. [1]

The paper entitled "Design of Low Power, High Performance 2-4 and 4-16 Mixed-Logic Line Decoders",

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International Journal & Magazine of Engineering, Technology, Management and Research
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has introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, they developed four new 2–4 line decoder topologies, namely 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer reduced transistor count and improved power delay performance in relation to conventional CMOS decoders. Furthermore, four new 4–16 line decoder topologies were presented, namely 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, realized by using the mixed-logic 2-4 decoders as predecoding circuits, combined with postdecoders implemented in static CMOS to provide driving capability. [2]

"Analysis of power reduction in 2 to 4 line decoder design using gate diffusion input technique", discussed that is an immense need of applications which consume less power and are small in area. In high performance digital systems, such as microprocessors, digital signal processor (DSPs) and other applications, the low power designs are of great importance. In this paper, an effort is made to come up with one such application called the 2-to-4 line decoder using the AND gate. Decoders are basically combinational circuits, which convert n-bit information into a maximum of 2n output lines. They are used where, on the occurrence of specific combinations of input levels an output or a group of outputs are to be activated. These input levels are often provided by the outputs of a counter or register. When the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially, and they can be used as timing or sequencing the signals to turn devices ON or OFF at specific times. [3]

The paper entitled "Design and Performance Analysis of Area Efficient CMOS Decoder Circuit", Today's integrated circuits have a growing need for speed, area, and power. Despite many advantages, CMOS suffers from increased area, more power dissipation and correspondingly increased capacitance and delay, as the logic gates become more complex .So they had develop and simulate the those layouts which consume less area and power. It has been demonstrated from the simulated results of different layout that the area is reduced in the full custom design of the decoder circuit from standard cell layout and the semi custom based layout of the decoder. The power is reduced in the semi custom design from standard cell layout but increased in the full custom design. So reduction of power in the full custom design is the future aspect. [4]

"CMOS VLSI Design: A Circuits and Systems Perspective", In this book, they would take a simplified view of CMOS transistors as switches. With this model we will develop CMOS logic gates and latches. CMOS transistors are mass produced on silicon wafers using lithographic steps much like a printing press process. We will explore how to lay out transistors by specifying rectangles indicating where dopants should be diffused, polysilicon should be grown, metal wires should be deposited, and contacts should be etched to connect all the layers. [5]

"Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", In this investigations, CPL was found to be the most efficient pass-transistor logic style. Complementary CMOS, however, proves to be superior to CPL in all respects with only few exceptions. An interesting alternative is represented by the single-rail pass-transistor logic and the proposed synthesis approach used in LEAP in order to better exploit the multiplexer structure of pass-transistor logic. [6]

"A 3.8 - ns CMOS 16 × 16 - b multiplier using complementary pass-transistor logic", In this paper described a fast 16 × 16 multiplier using a new differential CMOS logic family, CPL. In CPL, differential logic is constructed without pMOS laching load, enabling a speed more than twice as fast as conventional CMOS .The Power dissipation is also smaller due to smaller input capacitance. [7]

The paper entitled "A general method in synthesis of pass-transistor circuits", General rules for synthesizing logic gates in three representative pass- transistor techniques were developed an algorithmic way for generation of various circuit topologies is presented.

ISSN No: 2348-4845
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Generation of circuits with balanced input loads is suitable for library-based designs. The usefulness of these circuits is increased by application of complementarity and commutative principles. [8]

Delay and Power optimization in VLSI circuits", This paper covers, A procedure for optimally sizing transistors in a single critical path. while more complicated techniques are possible , the straightforward relaxation techniques we used resulted in program which is computationally very fast. [9]

## PROPOSED WORK

Line Decoder Circuits

### I. 2–4 Line Decoder

A 2–4 line decoder generates the 4 minterms $D_{0–3}$ of 2 input variables A and B. Depending on the input combination, one of the 4 outputs is selected and set to 1, while the others are set to 0. An inverting 2–4 decoder generates the complementary minterms $I_{0–3}$, thus the selected output is set to 0 and the rest are set to 1, In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2–4 decoder can be implemented with 2 inverters and 4 NOR gates Fig. 7 (a), whereas an inverting decoder requires 2 inverters and 4 NAND gates Fig. 7 (b), both yielding 20 transistors.

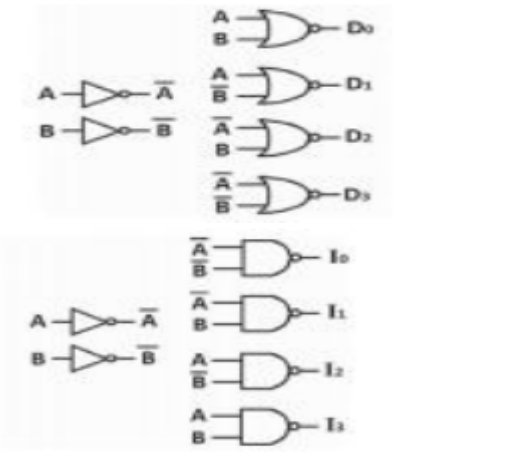


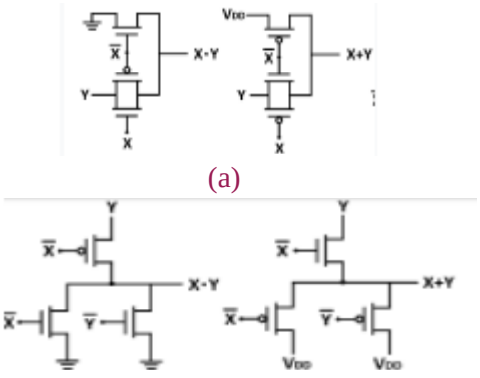
Fig. 7: 20-transistor 2–4 line decoders implemented with CMOS logic.

### II. 4–16 Line Decoder With 2–4 Predecoders

4–16 line decoder generates the 16 minterms $D_0$−$1_5$ of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minterms $I_0$−$1_5$. Such circuits can be implemented using a predecoding technique, Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gates [Fig. 2(a)], and an inverting one can be implemented with 2 2–4 decoders and 16 2-input NAND gates [Fig. 2(b)]. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

### Mixed-Logic Designs:

Transmission gate logic (TGL) can efficiently implement AND/OR gates, thus it can be applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 8 (a) and (b), respectively. They are full-swinging, but not restoring for all input combinations. Regarding PTL, there are two main circuit styles: those that use nMOS-only pass transistor circuits, like CPL, and those that use both nMOS and pMOS pass transistors, like DPL and DVL. The style we consider in this work is DVL, which preserves the full swing operation of DPL with reduced transistor count. The 2-input DVL AND/OR gates are shown in Fig. 8 (c) and (d), respectively. They are full swinging but non-restoring, as well.



(a)

(b)

Fig. 8: Three-transistor AND/OR gates considered in this work. (a) TGL AND/OR gate. (b) DVL AND/OR gate

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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Logic gates in conventional or complementary CMOS are built from an NMOS pull-down and a dual PMOS pull-up logic network. In addition, pass-gates or transmission gates (i.e., the combination of an NMOS and a PMOS pass-transistor) are often used for implementing multiplexers, XOR-gates, and flip-flops efficiently. [6] CPL is the used of an nMOS pass transistor network for logic organization and elimination of the pMOS Latch. [7] The main drawback of DPL is its redundancy, i.e. it requires more transistors than actually needed for the realization of a function. [8]

## CONCLUSION:

This paper briefly introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS proposed plan to achieve less delay, and also reduced number of gates. The area decreased and reduces the power using this design. If the power is reduced then the power dissipation will also get reduced. Hence the above design for low power consumption for decoders was proposed.

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