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A VLSI Implementation of Low Power Encoder using DVL, DPL and TGL

J. Anusha
Department of Electronics & Communication Engineering,
Annamacharya Institute of Technology & Sciences,
Kadapa, Andhra Pradesh 516003, India.

O. Homa Kesav
Department of Electronics & Communication Engineering,
Annamacharya Institute of Technology & Sciences,
Kadapa, Andhra Pradesh 516003, India.

ABSTRACT

This document introduces a switch logic-design technique for line-encoders, including with transmission-gate-logic, pass-transistor-logic and standard complementary metal-oxide semi-conductor (CMOS).Targeting on reducing the transistor count t, power utilization All proposed encoders have full-voltage level capability and decreased transistor count considered with their standard CMOS methodology. Finally, a different types of simulation at 32 nm gives the present method gives a effective performance in power and delay.

Key Words - Encoder, Switch-Logic, PTL, and TG

I. INTRDOUCTION

The convention CMOS is preferred most popularly in logic gates of integrated digital circuits. These consists of complementary N-type (ENMOS) and P-type (EPMOS) as pull down and pull up respectively. This network is more effectively designed for resistance, noise and well as for device variation. However, CMOS logic is effective for scaling of voltages and sizing of transistor and thus performs better generation of small voltages and also the small transistor sizes. The input lines are linked to transistor gates only, which reduces the complicated design and even provides last level of logic synthesis and design[13]

The year 1990 leads to the development of Pass-Transistor-Logic (PTL), when different styles preferred to run, which provides a reliable alternative to CMOS logic and improves speed, power delay and also the area. The vital differ is that the lines which are considered as inputs are given to either the gates and Source or Drain dif-fusions of transistors. The simple-single MOS .i.e., NMOS or PMOS transistor is called as a Pass transistor, and the parallel combination of NMOS & PMOS transistors connected in parallel is given as Transmission gate.[13]Line encoders are fundamental circuits famously preferred in primary circuits of memory elements (e.g. SRAM). This brief gives a mixed logic methodology for this development, opting for efficient performance related too single style design.

This part is described as follows: firstly gives a glance of the examined encoder circuits, designed with convention CMOS logic, secondly consists of new mixed logic designs. After that it details the comparative simulation study among the designed and conventional encoders, with a discussion of the designed results. Finally, terminates with the glance and final conclusions of the work designed. [12]

II. LINE ENCODERS

In digital studies, the concept is reported by binary codes. The 2^n bits of coded data can be represented up to n-different elements of binary code. An encoder is like a combinational circuit that translates coded data of 2^n-bit of binary coded data that has unused combination which generates the NxM min-terms of 2^n input variables.

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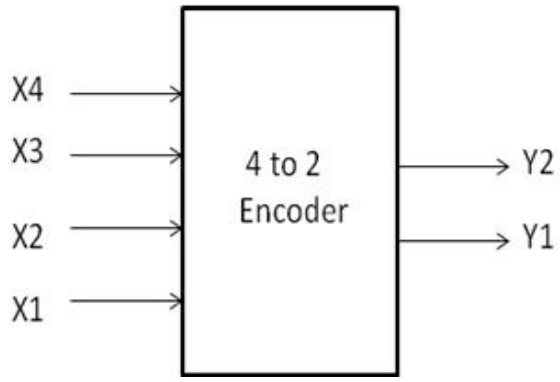


Fig :1 General 4-2 encoder block

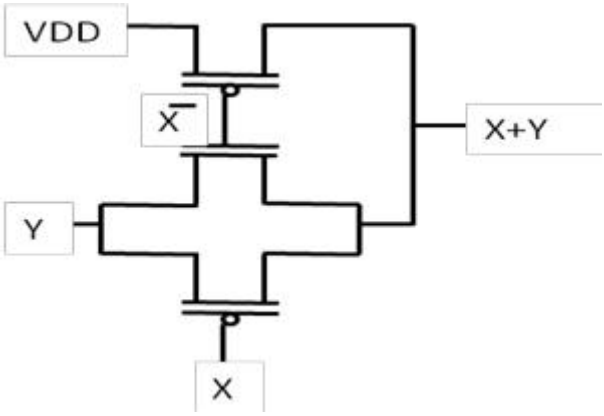
TABLE1: Truth-table of 4-2 encoder

X4	X3	X2	X1	Y2	Y1
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

TABLE2: Truth-table of inverting 4-2 encoder

I3	I2	I1	I0	Y2	Y1
1	1	1	0	0	0
1	1	0	1	0	1
1	0	1	1	1	0
0	1	1	1	1	1

III. SWITCH LOGIC DESIGN



Implementing a 4-2 line encoder with any one of TGL or DVL gates gives 16-transistors (12-t for AND/OR gates and 4-t for inverters). (12)

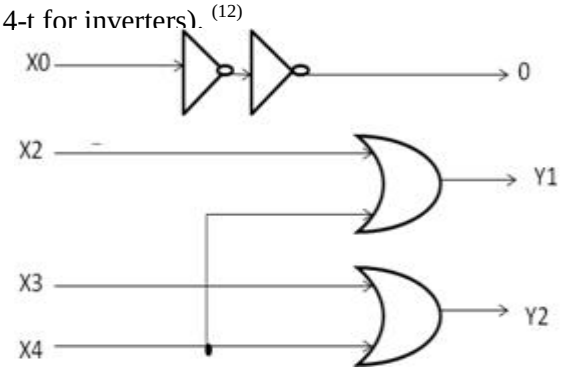


Fig 2: 20-Transistors 4-2 line encoders

In modern approach for reducing transistor count switch logic is used. This of two types i.e. Pass Transistor logic (PTL) and Transmission gate logic (TGL). Regarding PTL it is considered to be of two types as CPL in which only NMOS transistors are used whereas in DPL and DVL both PMOS and NMOS transistors are used. Here while considering DVL, this logic reduces transistor count of DPL.

The figures 3 and 4 show the switch logic operation f the Double Pass Transistor Logic and Dual Variable Logic.

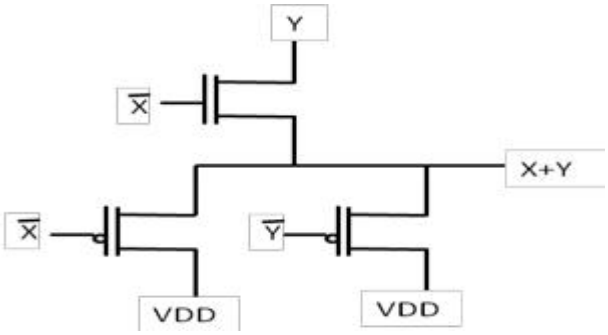


Fig 5: TG OR logic

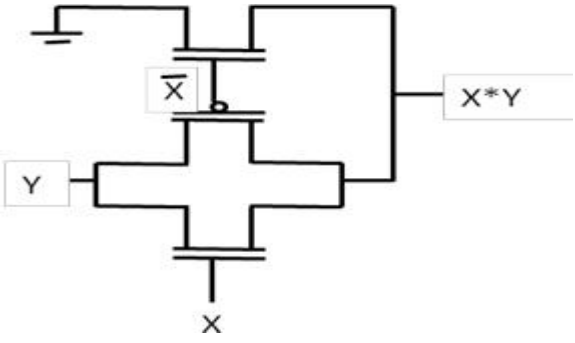


Fig 6: TG AND logic

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The encoder is designed by using these above logics .i.e. DPL, DVL, TG logics. Here 12 T are required by using DPL logic in order to obtain 4-2 encoder circuit with the help of two inverters for X3 and X4 input variables.

The fig. 5,6 Shows the 4-2 encoder with DPL.

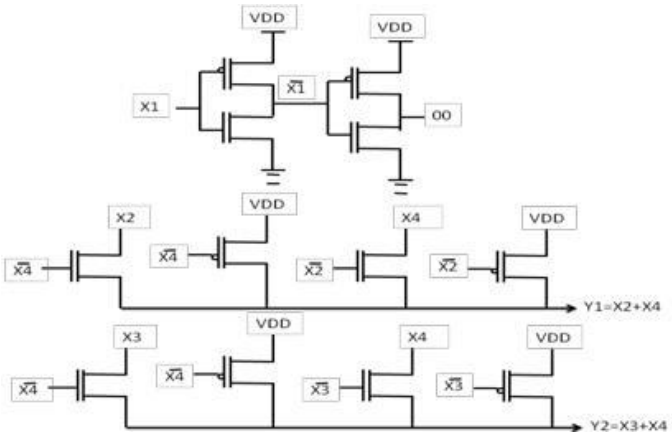


Fig 3:DVL OR logic

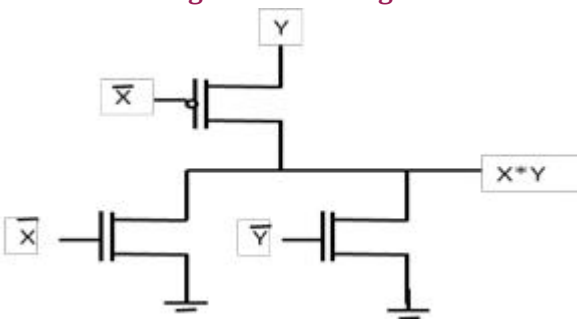


Fig 7: 4-2 Encoder using DPL

This figure shows the 4-2 encoder design with DVL by reducing the transistor count of DPL, with the use of 2 inverters for X2, X3 and X4 input signals.

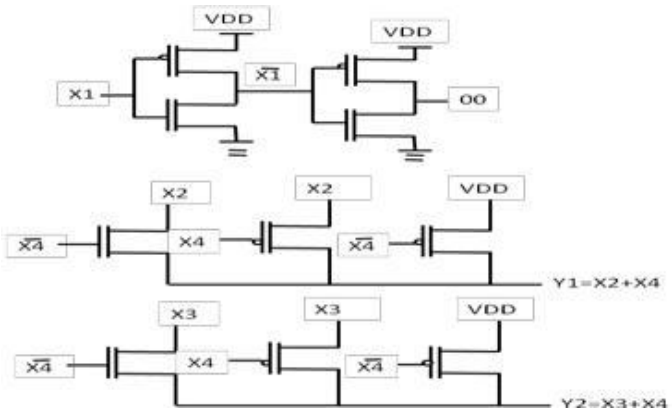


Fig 4 :DVL AND logic

The another type classified is Transmission Gate logic(TGL) in which both NMOS and PMOS transistors are considered in parallel to acquire full swing voltage capability as a output compared with other logic.

This TG logic also reduces the transistor count hence by reducing the area of the chip, also by power can also be reduced. Thereby an efficient full swing output voltage is obtained by using this logic.

Figure discuss about the TG logic in which the transistor count is reduced by reducing the fro to one inverter for X2 or X3 input terminals.

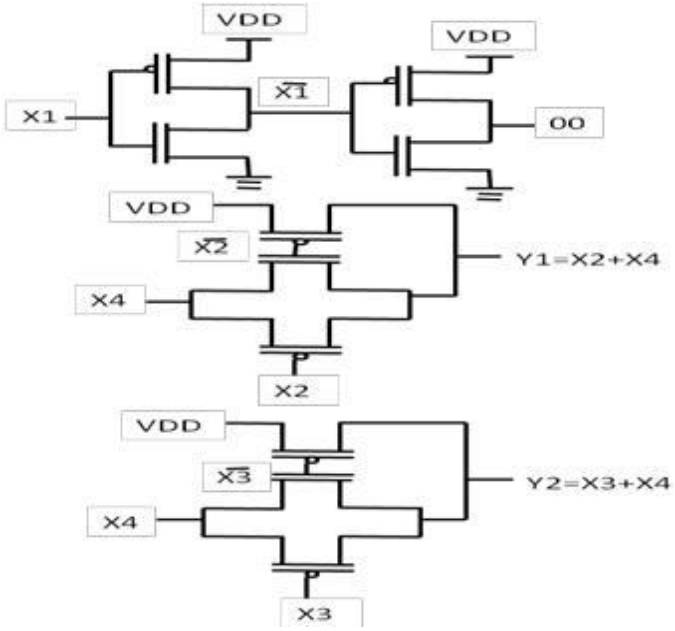
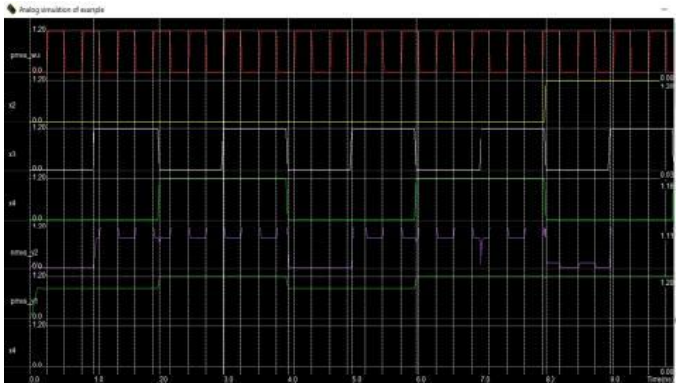


Fig 9: 4-2 Encoder using TG logic

IV. SIMULATION



DPL

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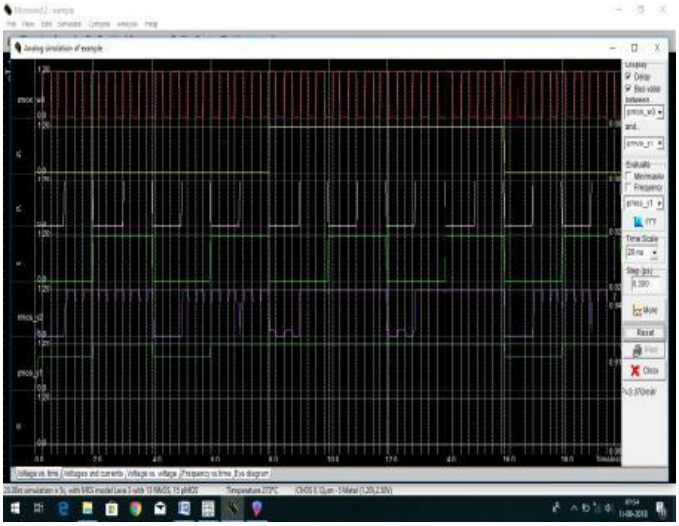
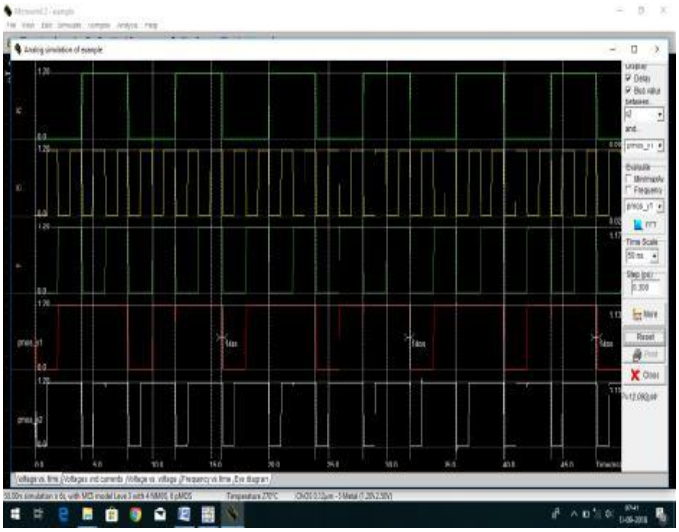


DVL



TGL

Fig 10: Simulation results of encoder

This circuits are represented using a 32 nm technology design to obtain better power appliances (PTM LP),[11]. For fair and unbiased comparison we use unit-size transistors exclusively ($L_n = L_p = 32$ nm, $W_n = W_p = 64$ nm) for all encoders[12]

A. Result Discussion

In simulation process different parameters like power, PDP and delay are examined by comparatively,. Each of the present de-signs will be compare to its standard counterpart[13]

TABLE3: Comparison Table of 4-2 Encoder:

Logic considered	Area(in terms of transistor count)	Power	Output Capability
DPL	14 T with 3 inverters	26.28µw	Full swing
DVL	12 T with 3 inverters	22.653µw	Full swing
TGL	10 T with 2 inverters	12.938µw	Full swing

V. CONCLUSION

By comparing conventional and switch logic from the results of 32nm technology switch logic implementation provides effective performance for count of a transistor and power-utilization.[12]

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