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An efficient diagnosis method to identify the Segmentation and number of faulty power switches in a design.

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Abstract: ***The speed test of power switches are used to reduce the leakage power electronic circuit design system this technique which shows the accurate power switching technique .our proposed system provides design test pattern solutions for efficient design testing power switches in the presence of power ,current, voltage, frequency, fast Fourier variations .which provides the power switches divided into segments this process provided the any fault or errors are detected so this system provides more accuracy results are provided. The proposed method we are using micro wind tool and DSCH tool, are 45 nm, technology are provided same simulation result compare other 90nm technology.***

Key words :ATPG generation , launch of capture , scanned enable , launch shifting operation , de4sign for test , sleep transistors , leakage power management , micro wind tool , DSCH , CMOS technology.

INTRODUCTION

The 45 nm micro wind CMOS technology used in a low-power design technique to reduce leakage power. It has gained popularity in sub-100-nmCMOS designs, the overall power consumption is controlled by leakage current It utilize s power switches(also called sleep transistors) to power-down the logic bSegment1ks during the idle mode to reduce leakage power consumption Power switches are implemented as header switches or footer switches. This paper analyzes the a design detail, but the results are equally applicable to footer power switches as well as. Power switches are usually implement in either “fine-grain” or“ coarse-grain” design styles. A fine- grain style in corporate a power switch within each standard logic cell with a control signal to switch on/off the power supply of the cell. In the coarse grain design style, a number of power switches are combined to feed a bSegment1k of logic. When comparing design style simplifies the i9n corporation of power gaining through MICROWIND ,DSCH tool .due to the voltage ,current, frequency , power variation s . in cross gain technique more useful compare fain grain tool operation and it takes less time.

Power switches are implemented in two power modes operations, which provides a tradeoff between leakage power saving mode and wake-up time. These process include complete power-off mode higher leakage power saving and intermediate power off mode lower wake-up time) Design-for-test (DFT) solutions for power switches with intermediate power-off mode have been recently proposed Therefore, this paper focuses on power switches with a complete power o ff mode. Recent research has reported a number of DFT solutions to test power switches when considering the two possible type of faults: stuck-open and stuck-short struck open mode operation is going on based on physically method in this method drain and source modes or off state leading to fault transistor behavior in this test transistor method two test vectors are generated one is output transistor logic either high or low .and the second vector transistor which provides pull up or pull down network system operations. Stuck-short faults produce a conducting path between

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V dd and ground and may be detected by a test technique called IDDQ testing which monitors the current flow during a steady-state condition .The first DFT solution was reported in [9], and was used to test power switches in both fine-grain and coarse-grain designs. However, it was highlighted in [10] that this DFT solution suffers from long discharge time when the power switches are turned off. This leads to long test time due to the necessity of applying a slower test cSegment1k and may lead to false test(false-fail or false-pass). This problem was addressed in through an effective DFT solution, which added a low-leakage(high *V*th) discharge transistor segment to the DFT. This is because the discharge transistor is switched off during normal operation of the design, therefore high performance and leaky(low *V* th or standard *V*th) transistors are unnecessary. This is why a high *V* th (low performance and less leaky) n MOS transistor is used as a discharge transistor. It is designed such that Ion is maximum and I off is minimum to ensure low leakage through virtual rail DFT during normal operation of the design.

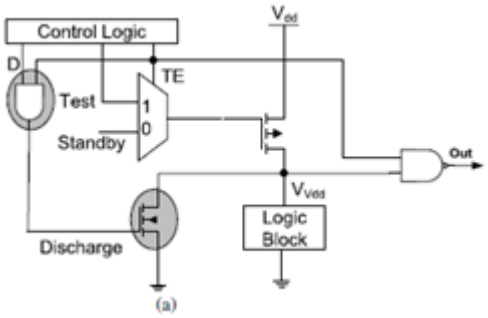

Fig1. fine grain circuit.

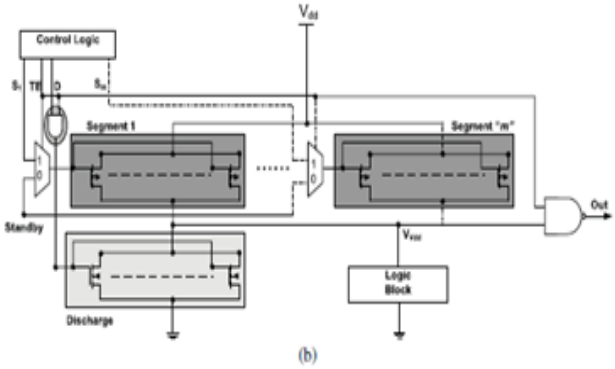

Fig2.cross grain circuit

Here we are designing the delay test for power switches by simulating delay at the outputs of specific unit of the circuit design. The circuit delay increase with a large number of faulty stuck-open power switches

III. DIAGNOSIS ALGORITHM

Proposed system

In this proposed system divided into segments using their corresponding frequency single error segment is detectable finding fault power switches are identified using three modules for test frequency for design. The algorithm (Fig. 1) takes as input the net list, number of segments "*m*," and test frequencies and returns diagnosis information consisting of the Segment1ation and number of faulty power switches per segment in a design. The algorithm is activates one segment (S*i* = 0, *i* ∈ [1,*m*]) during each test cycle, reaming all others segments are switched off. Diagnosis is carried out through capturing the signal at the output of NAND gate [signal "OUT" in Fig. 1(b)]. The algorithm steps to test each segment are shown in lines where starting from the first segment (*i* = 1), the highest test frequency (*f*1) is applied first and the response is observed at "OUT." In case OUT _= 0, the segment is identified as faulty, and lower test frequencies are then used to determine the number of faulty power switches for segment *i* . Once the number (range) of faulty power switches is identified, this information is stored on stack.

A. Launch of capture:

To restore scanned load state (the bit shifted) of the interface(functional) register upon the launch and capture operations ,one scanned test register is inserted for each interface register .Throughout the shift operations, the shadow register scanned the test content of the interface register, and during the capture window, the shadow register is not cSegment1ked, ensuring that the copied value in the last shift cycle is retained. Upon every launch and capture operation that the interface register gets involved in, its load state is restored by copying the content of the shadow register back into the interface register. Fig. 3 provides the DfT

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support for the load state restore mechanism. Effectively, a multiplexer and a shadow flip-flops inserted for the interface register, doubling the size of the interface scan cell. The newly inserted logic falls on the test paths only, incurring to timing penalty whatsoever. The restore signal can be easily generated on-chip as shown in the same figure. The total cost is *N*int MUX es and *N*int + 2 flip-flops for *N* int interface registers.

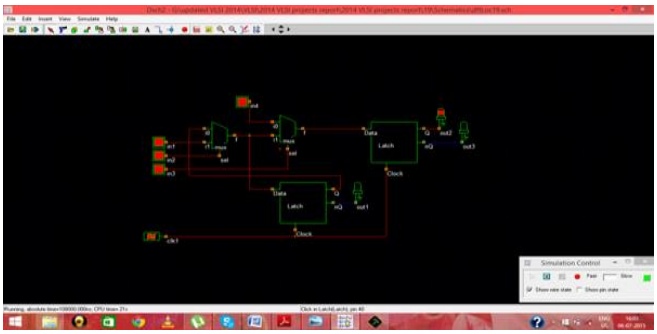

Fig 3 shows segment1 schematic diagram.

B. Implementation for launch of shifting operation:

The test of SEGMENT2 scheme launches transitions via a shift operation, a set of test patterns circuits are valid as the final scan cell performances in the chain perfectly matches that during automated test pattern generation. Therefore, SEGMENT2 pattern generation should be done subsequent to scan stitching in conventional SEGMENT2. The only additional constraint imposed on scan stitching by the proposed partitioning scheme is that the interface registers of each region should be placed in consecutive positions on the scan chain and that they must be stitched in a bidirectional manner. Such a special stitching and the associated DfT support are required only for the interface registers in order to enable a proper rewind operation; minimization of the number of interface registers helps to minimize the area of cost and minimum power ,less current ,low frequency . Finally, restoring the value of the right most bit of a group of interface registers subsequent to the launch operation necessitates an extra flip-flop, which holds the value of the rightmost interface bit upon operation restores the value of the rightmost interface register from the value in this extra flip-flop.

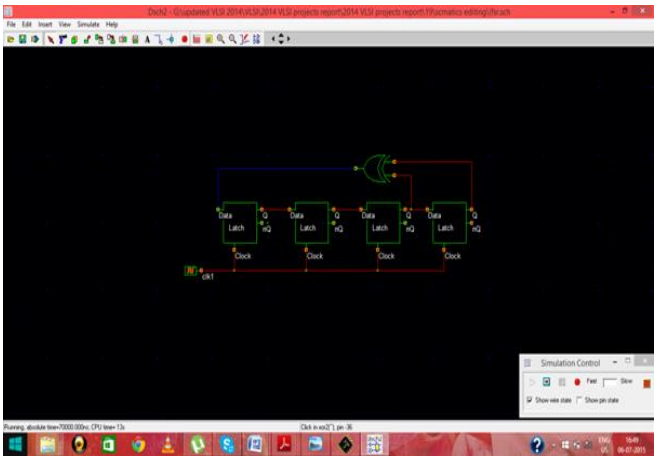

Fig 4.linear feedback register schematic circuit

In this shifting operation we are using linear feed back shift operation for shifting the test pattern generation bits . Bidirectional operation of the interface registers in a certain region needs one extra multiplexer for each interface register this multiplexer can be inserted on the scan path of the scanned multiplier input path imposing no impact on the functional timing of the design whatsoever. The proposed scanned architecture that supports design partitioning into two regions is provided .and it requires less area and less power consumption ,the area of chip design is very less compare to other techniques.

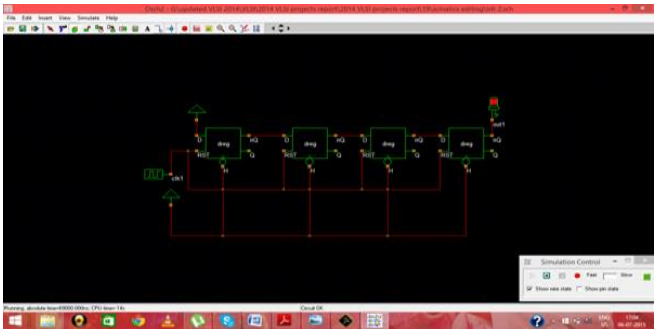

Fig 5 Segment2 operation

***C.* Design and implementation for combination of launch of capture and launch of shift:**

As the SEGMENT2 and SEGMENT1 testing may uniquely detect the faults in a mutually exclusive manner, a mixed operation test pattern generates or covers the high fault error detection compare to other schematic techniques operation . In this section, the

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final output result provides low power testing and delay operation is performed based on combination of segment1 and segment 2operation. The SEGMENT2/SEGMENT1 signal, which denotes the type of test for the current pattern being applied and can be peak launch power reduction; the maximum reduction in peak launch power as well as in peak capture power and the required area cost are presented the results when a certain level of peak launch power reduction is targeted and attained; columns 6–11 present the 10%, respectively.

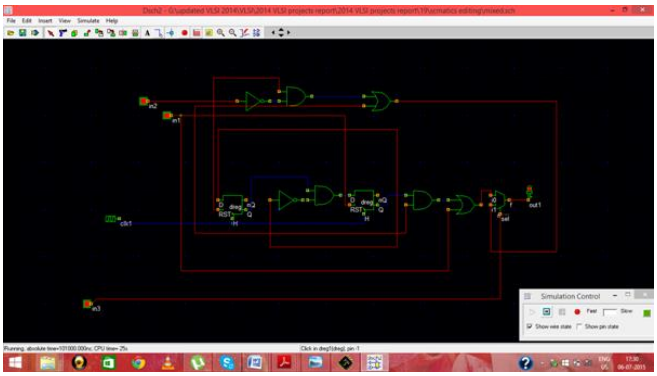

Fig6 Proposed mixed operation technique for power optimization technique

In this schematic diagram which shows combination of both segments operation .in this technique we reduced more power and less time , and caluculate the power, voltage, current ,frequency values compare to other tools. we reduce the minimum 40-60%of power.

IV SIMULATION RESULTS :

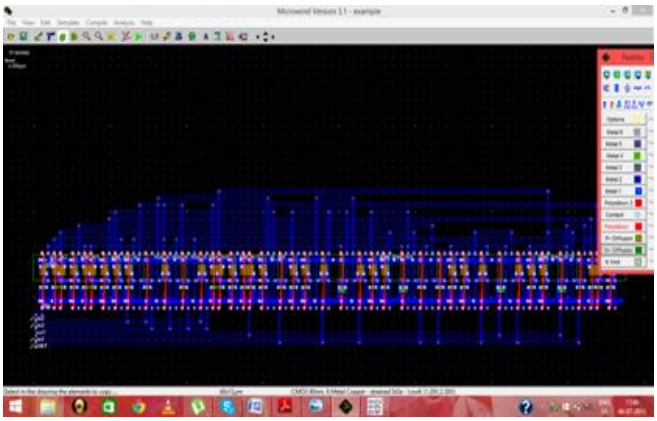

Fig 7.layout diagram for power optimization delay testing

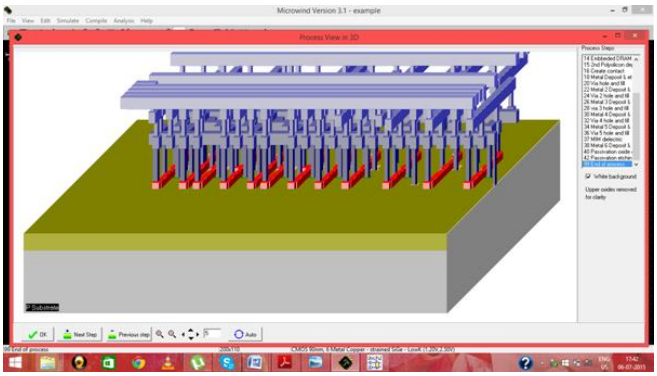

Fig 8.3D design for power optimization for delay testing

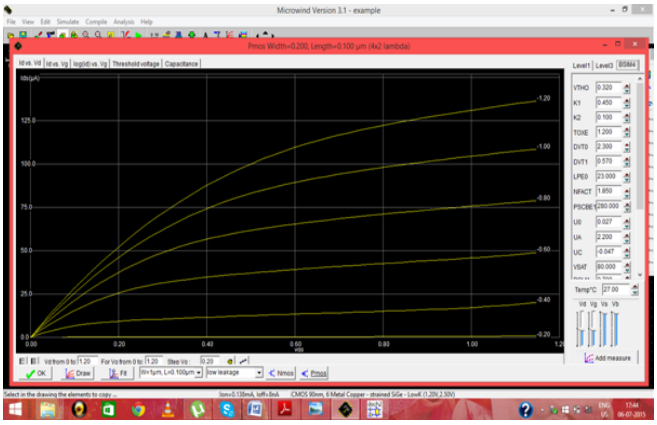

Fig 9.cmos characteristics simulation

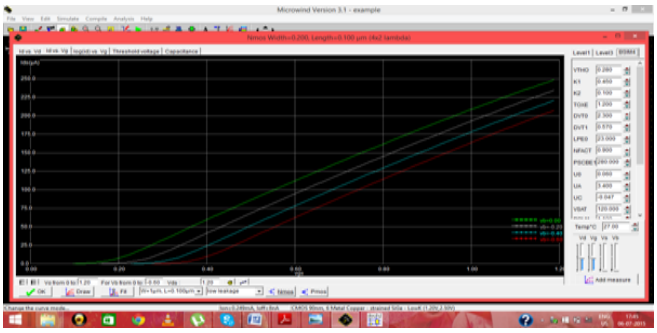

Fig 10.drain current vs gate voltage simulation result

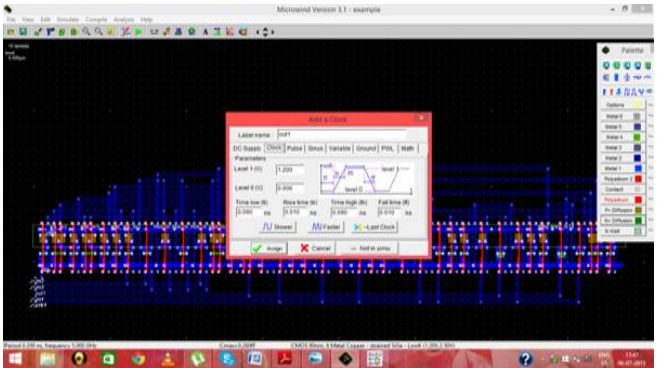

Fig 11. fall time ,rise time ,time high signal simulation result

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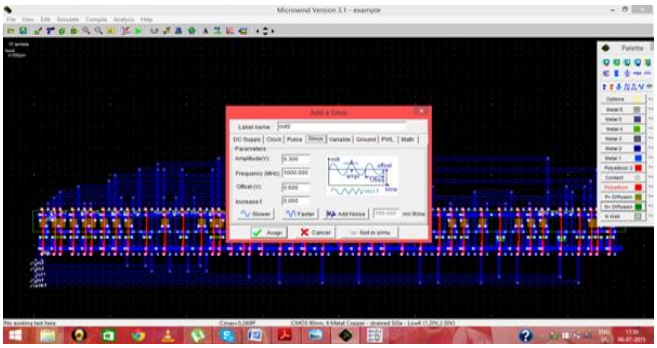

Fig 12.output shows the testing signal amplitude ,peak value variations

ANALOG SIMULATION OUTPUTS

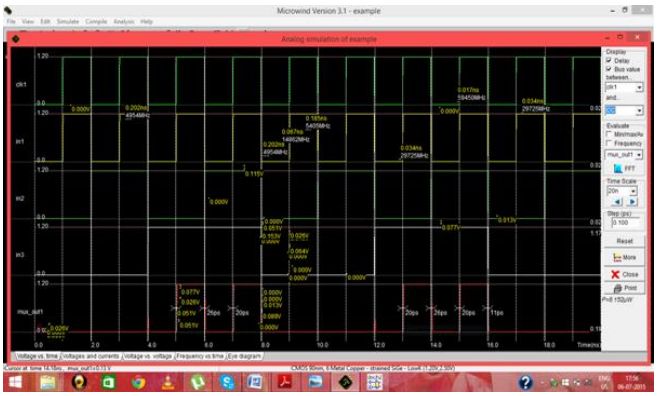

FIG 13. voltage vs time simulation

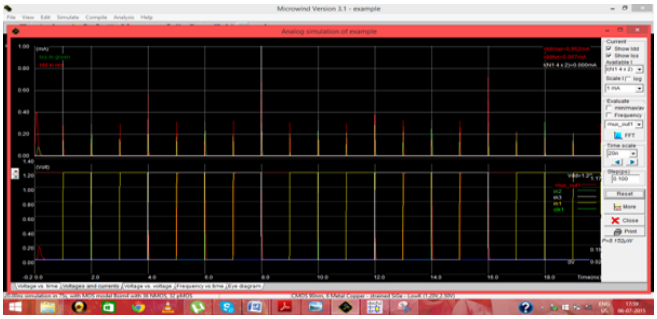

Fig 14. current vs voltage simulation out put wave forms.

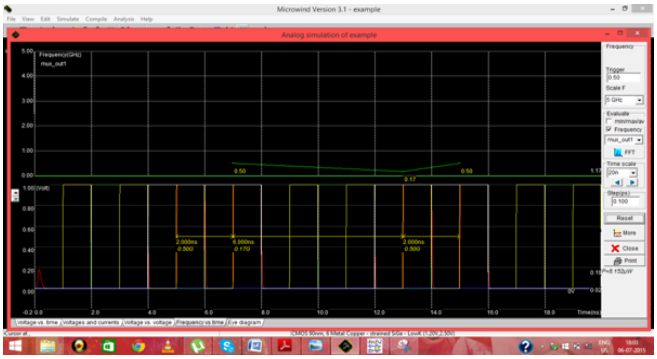

Fig 15. frequency vs time simulation output

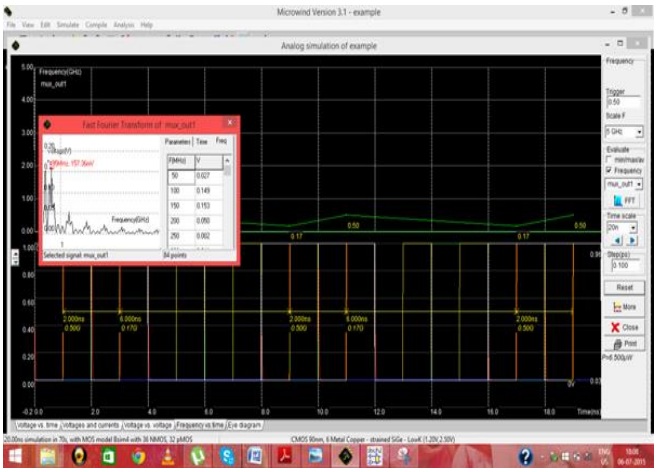

Fig 16 . analog simulation time delay vs frequency FFT operations

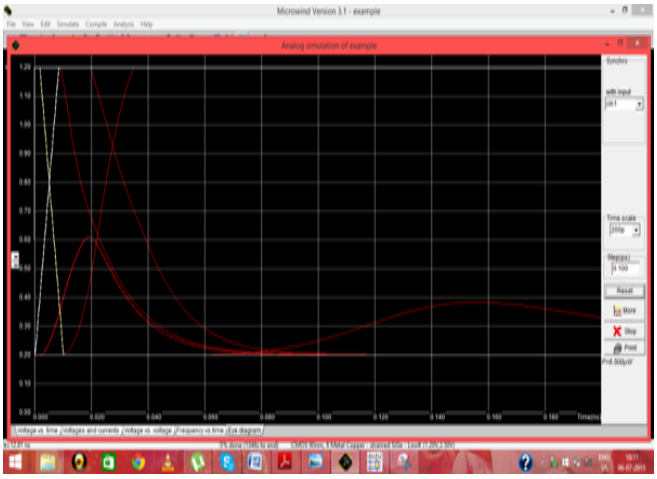

Fig 17 .visual effect of delay testing operation.

V CONCLUSION

We demonstrated an efficient diagnosis method to identify the Segmentation and number of faulty power switches in a design. It utilizes an efficient DFT solution for testing power switches. The proposed method divided power switches into segments and uses the transition delay test to achieve very high diagnosis accuracy. The diagnosis method was validated through MICROWIND,DSCH operation .we observe in this simulation we take 1.20 v voltage ,0.962m A and 0.51 MHZ frequency are used and it takes less power 0.144w compare to other techniques, here the testing pattern provides 100% accuracy compare to techniques.

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