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Lessening of power loss in voltage/current source inverter by using Space Vector Pulse Width Modulation (SVPWM) Technique.

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Abstract- ***The main objective of this paper is a space vector pulse width amplitude modulation (SVPWAM) method for a buck–boost voltage/current source inverter. For a voltage source inverter, the switching loss is reduced by 87%, compared to a conventional sinusoidal pulse width modulation (SPWM) method. For a current source inverter, the switching loss is reduced by 60%. In both cases, the power density is increased by a factor of 2 to 3. In addition, it is also verified that the output harmonic distortions of SVPWAM is lower than SPWM, by only using one-third switching frequency of the latter one. As a result, it is feasible to use SVPWAM to make the buck–boost inverter suitable for applications that require high efficiency, high power density, high temperature, and low cost. Such applications include electric vehicle motor drive or engine starter/alternator.***

Index terms- ***SVPWM, Switching power loss, VSI,CSI, Buck-boost***

Introduction- Varies types of modulation method have been proposed previously such as optimized pulse-width-modulation, improved Space-Vector-PWM control for different optimization targets and applications, and discontinuous PWM (DPWM). Different switching sequence arrangement can also affect the harmonics, power loss and voltage/current ripples. DPWM has been widely used to reduce the switching frequency, by selecting only one zero vector in one sector. It results in 50% switching frequency reduction. However, if an equal output THD is required, DPWM can not reduce switching loss than SPWM. Moreover, it will worsen the device heat transfer because the temperature variation. A double 120 flattop modulation method has been proposed in and to reduce the period of PWM switching to only 1/3 of the whole fundamental period. However, these papers didn't compare the spectrum of this method with others, which is not fair. In addition, the method is only specified to a fixed topology, which cannot be applied widely. This paper proposes a novel generalized space vector pulse width amplitude modulation (SVPWAM) method for the buck/boost voltage source inverter (VSI) and current source inverter (CSI). By eliminating the conventional zero vector in the space vector modulation, two-third and one-third switching frequency reduction can be achieved in VSI and CSI, respectively. If a unity power factor is assumed, an 87% switching loss reduction can be implemented in VSI, and a 74% reduction can be implemented in CSI. A 1-kW boost-converter inverter system has been developed and tested based on the SVPWAM method. A 90% power loss reduction compared to SPWM has been observed. The two stage efficiency reaches 96.7% at the full power rating. The power volume density of the prototype is 2.3 kW/L. The total weight of the system is 1.51 lb. Therefore, ahigh-efficiency, high-power density, high-temperature, and low cost 1-kW inverter is achieved by using an SVPWAM method

SVPWAM FORVSI

A. Principle of SVPWAM Control in VSI

The principle of an SVPWAM control is to eliminate the zero vector in each sector. The modulation principle of SVPWAM is shown in Fig. 2. In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the

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adjacent two sectors. For example, in sector VI and I, phase leg A has no switching at all. The dc-link voltage thus is directly generated from the output line-to-line voltage. In sector I, no zero vector is selected. Therefore,S1and S2keep constant ON, andS3and S6are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltageVacat this time. Consequently, the dc-link voltage should present a6ωvaried feature to maintain a desired output voltage.

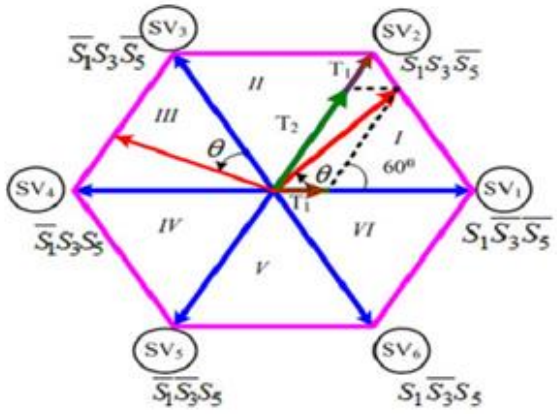

Fig. 2. SVPWAM for VSI.

B. Inverter Switching Loss Reduction for VSI

For unity power factor case, the inverter switching loss is reduced by 86% because the voltage phase for PWM switching is within [−60◦,60◦], at which the current is in the zero-crossingregion.

In VSI, the device voltage stress is equal to dc-link voltage VDC, and the current stress is equal to output current ia. Thus the switching loss for each switch is

$$P_{\mathrm{SW\_I}} = \frac{1}{2\pi}\left[\int_{-\pi/6}^{\pi/6} E_{\mathrm{SR}} \frac{|I_m \sin(\omega t)| \cdot V_{\mathrm{DC}}}{V_{\mathrm{ref}} I_{\mathrm{ref}}} \cdot f_{\mathrm{sw}}\, d\omega t + \int_{5\pi/6}^{7\pi/6} E_{\mathrm{SR}} \frac{|I_m \sin(\omega t)| \cdot V_{\mathrm{DC}}}{V_{\mathrm{ref}} I_{\mathrm{ref}}} \cdot f_{\mathrm{sw}}\, d\omega t\right] = \frac{2-\sqrt{3}}{\pi} \cdot \frac{I_m V_{\mathrm{DC}}}{V_{\mathrm{ref}} I_{\mathrm{ref}}} E_{\mathrm{SR}} \cdot f_{\mathrm{sw}},$$

(1)

Where ESR,Vref,Iref are the references.

In result, the switching loss of SVPWAM over SPWM is f=13.4%. However, when the power factor decreases, the switching loss reduction amount decreases because the switching current increases as Fig. 3 shows. As indicated, the worst case happens when power factor is equal to zero, where the switching loss reduction still reaches 50%. In conclusion, SVPWAM can bring the switching loss down by 50–87%

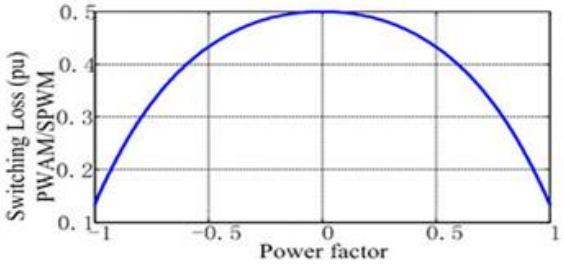

Fig. 3. (SVPWAM power loss/SPWM power loss) versus power factor in VSI.

SVPWAM FOR CSI

A. Principle of SVPWAM in CSI

The principle of SVPWAM in CSI is also to eliminate the zero vectors. As shown in Fig. 4, for each sector, only two switches are doing PWM switching, since only one switch in upper phase legs and one switch in lower phase legs are conducting together at any moment. Thus, for each switch, it only needs to do PWM switching in two sectors, which is one-third of the switching period. Compared to SVPWM with single zero vector selected in each sector, this method brings down the switching frequency by one-third. Similarly, the dc-link current in this case is a6ωvaried current. It is the maximum envelope of six output currents: Ia,Ib,Ic,−Ia,−Ib,−Ic, as shown in Fig. 8. For example, in sector I,S1 always keeps ON, so the dc-link current is equal to Ia. The difference between dc-link current in CSI and dc-link voltage in VSI is dc-link current in CSI is overlapped with the phase

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current, but dc-link voltage in VSI is overlapped with the line voltage, not the phase voltage.

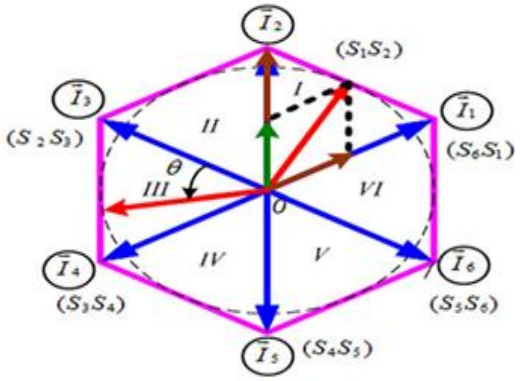

Fig.4. Conventional CSI and its corresponding SVPWAM diagram

B. Inverter Switching Loss Reduction for CSI

In CSI, the current stress on the switch is equal to the dc link current, and the voltage stress is equal to output line-to-line voltage, as shown the shadow area in Fig. 5Thus, the switching loss for a single switch is determined by

$$P_{\mathrm{SW\_CSI}} = \frac{2-\sqrt{3}}{\pi}\frac{\overline{i_{\mathrm{dc}}}\cdot V_{\mathrm{l-lpeak}}}{V_{\mathrm{ref}} I_{\mathrm{ref}}} E_{\mathrm{SR}} f_{\mathrm{sw}}.$$

(2)

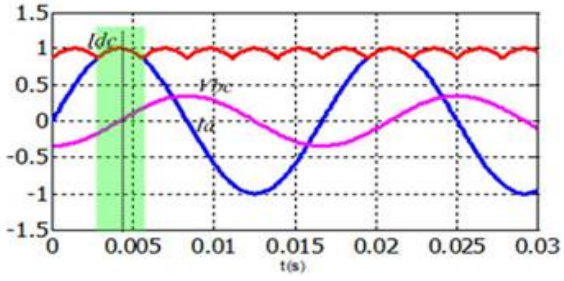

Fig. 5. Switching voltage and current when pf=1.

When compared to discontinuous SVPWM, if the half switching frequency is utilized, then the switching loss of it becomes half of the result in . The corresponding switching loss ratio between SVPWAM and discontinuous SVPWM is shown in Fig.6

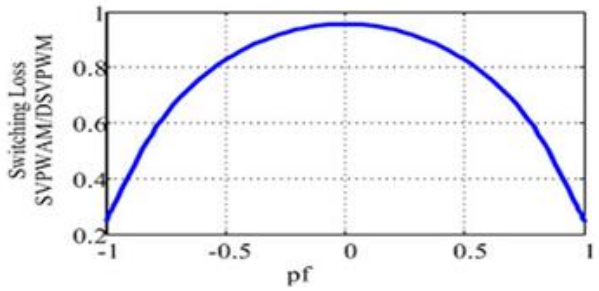

Fig.6. CSI switching loss ratio between SVPWAM and discontinuous SVPWM versus power factor

Topologies for SVPWM

Basically, the topologies that can utilize SVPWAM have two stages: dc–dc conversion which converts a dc voltage or current into a6ωvaried dc-link voltage or current; VSI or CSI for which SVPWAM is applied. One typical example of this structure is the boost converter inverter discussed previously. However, the same function can also be implemented in a single stage, such as Z/quasi-Z/trans-Z source inverter [37]. The front stage can also be integrated with inverter to form a single stage. Take current-fed quasi-Z-source inverter as an example. Instead of controlling the dc-link current Ipn to have a constant average value, the open zero state duty cycle Dop will be regulated instantaneously to control Ipm to have a 6ω fluctuate average value, resulting in a pulse type 6ωwaveform at the real dc-link current Ipn, sinceI1is related to the input dc current Iin by a transfer function

$$I_1 = \frac{1-D_{\mathrm{op}}}{1-2D_{\mathrm{op}}} I_{\mathrm{in}}$$

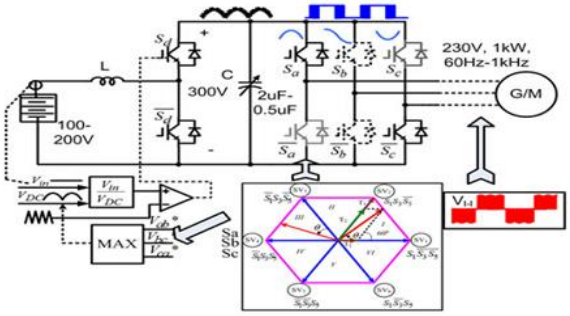

Fig. 7. SVPWAM-based boost-converter-inverter motor drive system.

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PRINCIPLE OF OPERATION

The circuit schematic and control system for a 1-kW boost converter inverter motor drive system is shown in Fig.7 . A 6ωdc-link voltage is generated from a constant dc voltage by a boost converter, using open-loop control. Inverter then could be modulated by a SVPWAM method. The specifications for the system are input voltage is 100–200 V; the average dc-link voltage is 300 V; output line-to-line voltage rms is 230 V; and frequency is from 60 Hz to 1 kHz.

In SVPWAM control of boost mode, dc-link voltage varies with the output voltage, in which the modulation index is always kept maximum. So, when dc-link voltage is above the battery voltage, dc-link voltage level varies with the output voltage. The voltage utilization increased and the total power stress on the devices has been reduced

SIMULATION DIAGRAM AND RESULTS

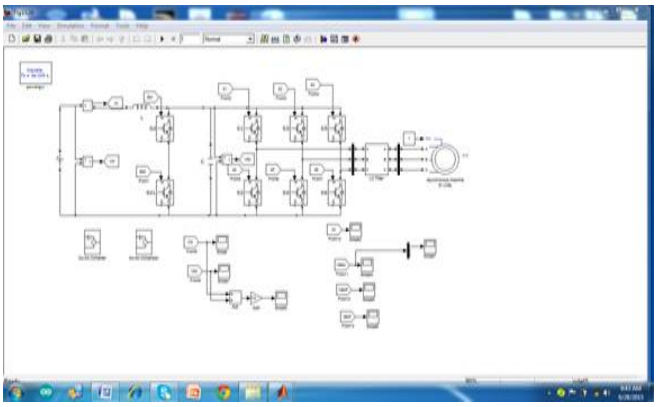

Figure8 : SVPWAM-based boost-converter-inverter motor drive system (Vin=20V)

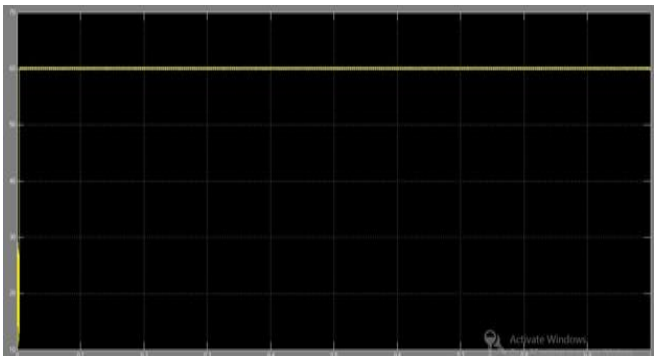

Figure 9 :Vdc avg=60V

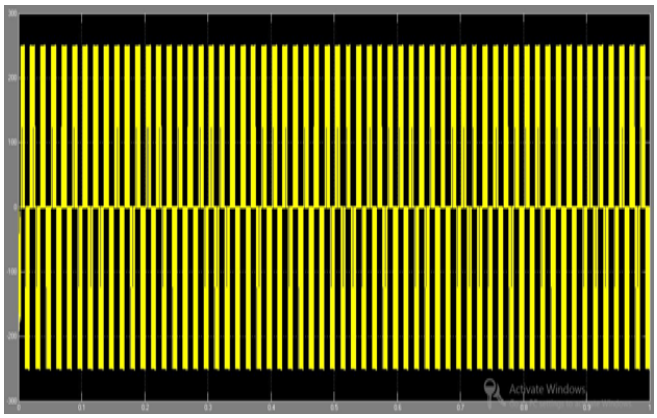

Figure 10: Vab before filter

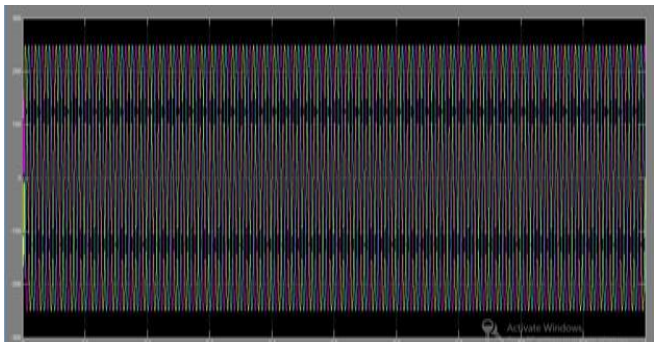

Figure 11: Vab after filter

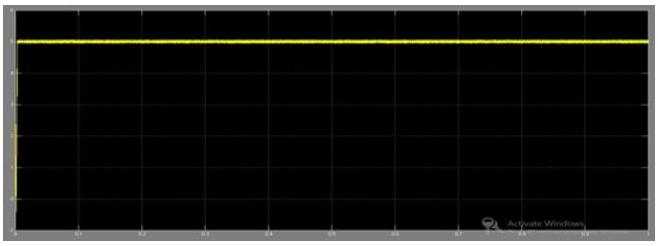

Figure 12: Iin

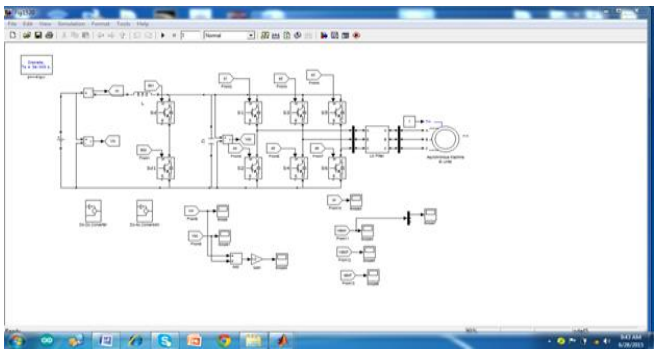

Figure 13 : SVPWAM-based boost-converter-inverter motor drive system (Vin=100V)

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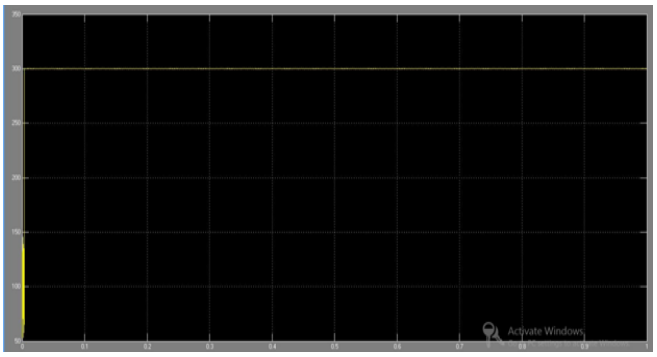

Figure 14:Vdc avg=300V

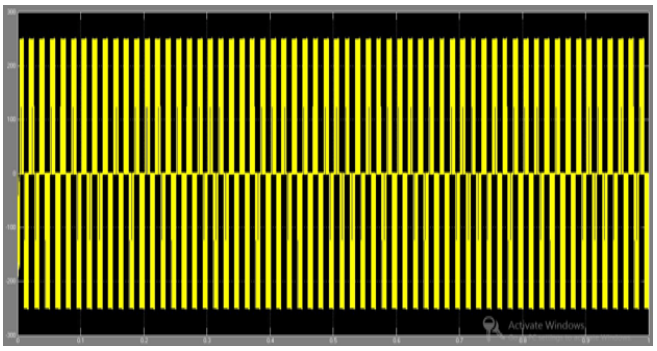

Figure 15 : Vab before filter

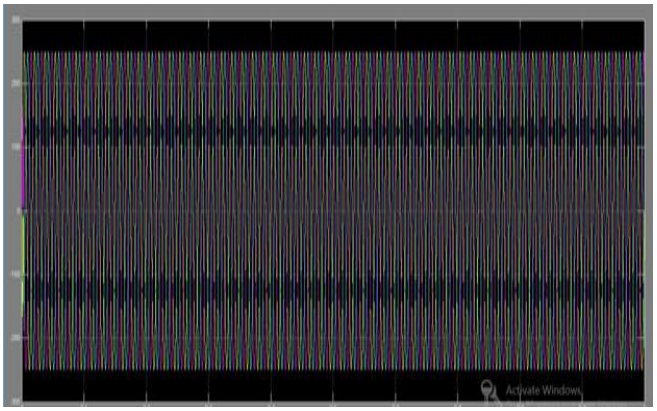

Figure 16: Vab after filter

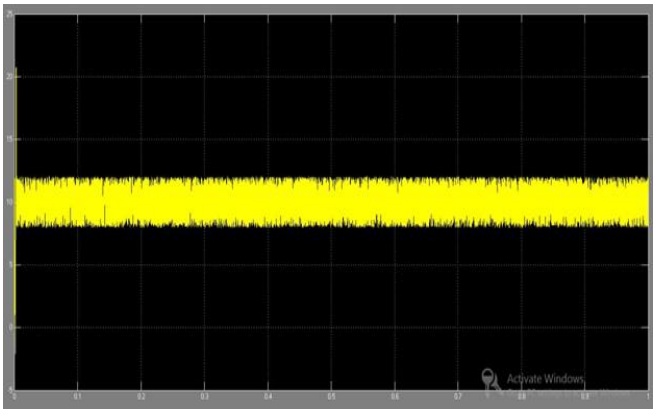

Figure: Iin

CONCLUSION

The SVPWAM control method preserves the following advantages compared to traditional SPWM and SVPWM method.

1) The switching power loss is reduced by 90% compared with the conventional SPWM inverter system.

2) The power density is increased by a factor of 2 because of reduced dc capacitor (from 40 to 6 μF) and small heat sink is needed.

3) The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress. A high-efficiency, high-power density, high-temperature, and low-cost 1-kW inverter engine drive system has been developed and tested. The effectiveness of the proposed method in reduction of power losses has been validated by the experimental results that were obtained from the laboratory scale prototype.

REFERENCES

[1] D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for highpower applications," *IEEE Trans. Ind. Appl.*, vol. 25, no. 4, pp. 634–643, Jul./Aug. 1989.

[2] W.McMurray, "Resonant snubbers with auxiliary switches," *IEEE Trans. Ind. Appl.*, vol. 29, no. 2, pp. 355–362, Mar./Apr. 1993.

[3] J.-S. Lai, R. W. Young, Sr., G. W. Ott, Jr., J. W. McKeever, and F. Z. Peng, "A delta-configured auxiliary resonant snubber inverter," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 518–525, May/Jun. 1996.

[4] J. S. Kim and S. K. Sul, "New control scheme for ac-dc-ac converter without dc link electrolytic capacitor," in *Proc. 24th Annu. IEEE Power Electron. Spec. Conf.*, Jun. 1993, pp. 300–306.

[5] K. Rigbers, S. Thomas, U. Boke, and R. W. De Doncker, "Behavior and loss modeling of a three-phase resonant pole inverter operating with 120°A double flattop modulation," in *Proc. 41st IAS Annu.*

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International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Meeting IEEE Ind. Appl. Conf., Oct. 8–12, 2006, vol. 4, pp. 1694–1701.

[6] J. Shen, K Rigbers, C. P. Dick, and R. W. De Doncker, "A dynamic boost converter input stage for a double 120◦ flattop modulation based threephase inverter," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Oct. 5–9, 2008, pp. 1–7.

[7] H. Fujita, "A three-phase voltage-source solar power conditioner using a single-phase PWM control method," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 3748–3754.

[8] H. Haga, K. Nishiya, S. Kondo, and K. Ohishi, "High power factor control of electrolytic capacitor less current-fed single-phase to three-phase power converter," in *Proc. Int. Power Electron. Conf.*, Jun. 21–24, 2010, pp. 443– 448.

[9] X.Chen and M. Kazerani, "Space vectormodulation control of an ac-dc-ac converter with a front-end diode rectifier and reduced dc-link capacitor," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1470–1478, Sep. 2006.

[10] M. Hinkkanen and J. Luomi, "Induction motor drives equipped with diode rectifier and small dc-link capacitance," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 312–320, Jan. 2008.