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Design and Comparative Analysis of Different Latch-Type Sense Amplifiers

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Abstract: ***The difference of input voltage sense amplifier (SA)exceeds the offset voltage (VOS), the SA correctly detects The output voltage of large signal. However, when the input voltage of certain region, thesense amplifier can fail it shows the difference of input voltage sense. If it is sufficiently large,this input voltage region is modified or provide the sensing dead zone of thesensing amplifier.The problem is sensing dead zones differ depending on SAs and the inputvoltages to the SA differ depending on the memory devices, verifying the sensing dead zone is most important. In this project, we find thesensing dead zones of the most usual latch-type sensing amplifiers, voltage- andcurrent-latched SAs. In feature, most important type of sensing amplifier technique isproposed for different type of SA input voltages in terms of sensing delay, powerreduction , and PDP techniques are , using a 90-nm micro wind and DSCH operations.***

Keywords: ***Latch-type, mismatch, offset voltage, sense amplifier (SA), sensing dead zone, micro wind tool, DSCH, technologies.***

IINTRODUCTION

In memory devices sensing amplifier is one of the most peripheral circuit although many types sensing amplifier developed,the most popular type of sensing amplifier is latch type sensing amplifier because it provides high speed and low power consumption. And it provides two type of sensing amplifier and is voltage latch sensing amplifier with n-MOS foot switch amplifier, based p-MOS access transistors and second thing current sensing latch amplifier using n-MOS foot switch voltage latch sensing amplifier which sense the voltage difference between bit line voltage and bit line bar voltage and amplifiers provides rail to rail output voltages and same as the current latch sensing amplifier provides bit line voltages and the voltage latch sensing provides high speed and low power consumption compare to current latch sensing amplifier, less area because current latch sensing amplifier having less transistors,here output nodes having serve as a input nodes and sense amplifier enable signal it controlled carefully. But current latch sensing amplifier can't do output serve nodes act has a input node because having to separate output node and input node operations.

$$Y_{SA} = P\left[\Delta V_{BL} > V_{OS}\right] = \Phi\left(\frac{\Delta V_{BL} - \mu_{OS}}{\sigma_{OS}}\right)$$

The above equation it shows the general Gaussian distribution function of cumulative distributive function of the standard normal distribution function whereYsa is yield function,μos is mean of vos and σOS is standard deviation function of Vos and Ysa depends only bit line voltage,Ysa is significantly reduced input voltage and the bit line voltage is large at the input voltage sensing becomes dead zone. And deferent types of memory sensing devices like SRAM, DRAM ,MRAM, PRAM .here SRAM provides input voltage near vdd but D RAM provides half of the VDD.

II. SENSING DEAD ZONES OF LATCH-TYPE SENSING AMPLIFIER

Simulation TECHNIQUE and Variability

Simulation technique we are using 45nm CMOS technology and verifying the power reduction of bit line voltage and current latch value of bit line current.

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BL is assumed to be larger than *V*BLB by *ΔV*BL. The sensing amplifier input voltage is defined as *V*BL in this brief. DSCH ,micro wind simulations were performed to analyze the sensing dead zones of an sensing amplifier. There are many sources of random and systematic variability that can induce transistor mismatch. As the process technology is scaled down, the effects of random variation increase.

The standard deviation mathematical expression is

$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{W \times L}}$$

$$A_{VT} = \frac{\sqrt[4]{4q^3 \varepsilon_{Si} \Phi_F N}}{2} \cdot \frac{T_{OX}}{\varepsilon_{OX}}$$

Here *A*VT is expressed constant value depends on process techniques ,*F* is the Fermi potential, *T*OX is the thickness of the gate oxide, *N* is the doping concentration of the substrate *ε*OX are the permittivity of silicon and the gate oxide, respectively. The simulation methodology for performing sensing dead zone analysis is as follows. With a fixed value of *V*BL, the correct sensing operation occurs when *ΔV*BL is larger than *V*OS. Then, *Y*SA can be estimated as

$$Y_{SA} = \frac{\text{number of correct sensing operations}}{\text{total MC simulation trials}}$$

Modified *CLSAs and VLSAs*

The range of bit line divided into six regions based on standard deviation equation technique .the voltage difference between the output nodes when latching PMOS turned on increases and very accuracy decision. same as the standard deviation decreases the bit line also decreases when the bit line is less than the threshold voltage . at the time input transistors are off state .here no sensinsing operation is performed .the problem is transistors can not be convert input voltage into current. by using this statement voltage to current conversation technique .at the time sensing dead zone becomes low compare to threshold voltage .

III. Proposed system

VLSAs with Double Switches:

In this proposed system invalid switches are removed by adding new header switches or footswitches respectively, by providing complimentary sensing enable signals .

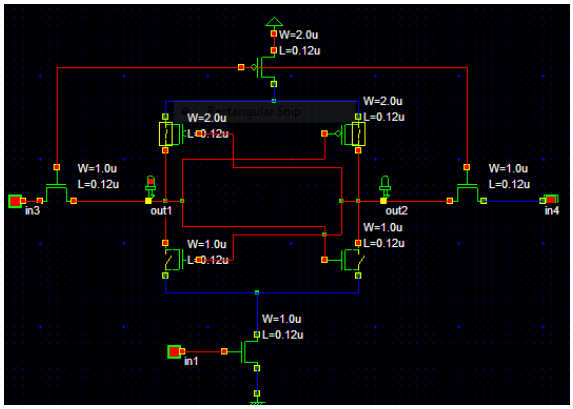

Fig 1 .showsDouble switch schemes. (a) DSPA-VLSA.

The additional switch prevents the weak latching transistors (MP1 and MP2 in DSPA-VLSA, orMN1 and MN2 in DSNA-VLSA) from being turned on during an idle period; thus, the invalid current paths are prevented , leading to a wide sensible *V*BL region. In the DSPA-VLSA, if the SAEB is activated earlier than SAE, both MP1 and MP2 are turned on when *V*BL is lower than*V*DD−|*V*THP|, leading to invalid current paths, similar to those found in FSPA-VLSA. Thus, the SAE must be activated earlier than the SAEB. Similarly, the SAEB must be activated earlier than the SAE in the DSNA-VLSA.

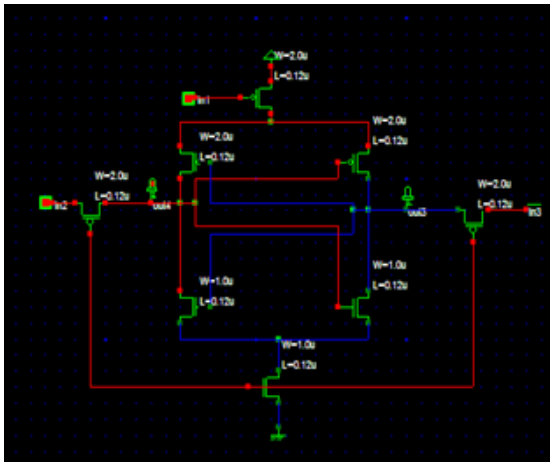

Fig 2.DSNA VLSA.

Sequence of circuit is implemented by using an inverter between SAE (SAEB)and SAEB (SAE).

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Because of the additional switch, the sensing amplifier scheme dead zones of double switch schemes become narrow compared to those of single switch schemes; however, the sensing dead zones never disappear because of the voltage transmitting problems introduced by the access transistors. Because the p MOS access transistors in the DSPA-VLSA cannot perfectly transfer the *V*BL when it is lower than| *V*THP|, the sensing dead zone is below |*V*THP|. Similarly, because MOS access transistors in DSNA-VLSA cannot perfectly transfer the *V*BL higher than *V*DD − *V*THN, the sensing dead zone is above *V*DD − *V*THN.

VLSAs With Double Switches and Transmission Gate Access Transistors

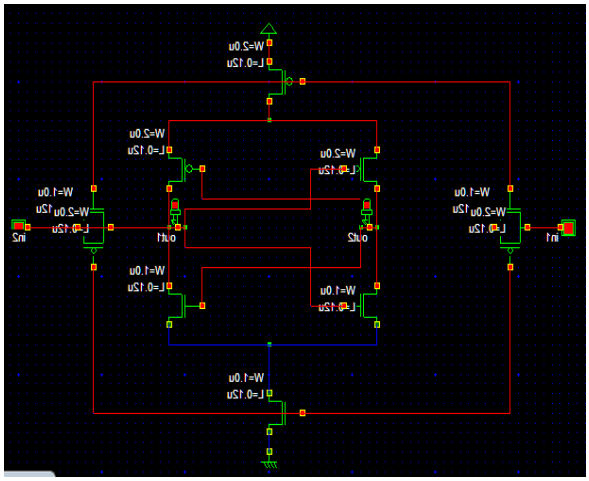

Fig 3 VLSAs With Double Switches and Transmission Gate Access Transistors

The double switching sensing amplifier reduced the size of sensing dead zone , its access transistors induce the sensing dead zone. Using transmission gates the access transistors, as shown in Fig. 3, one can completely remove the sensing dead zone. The solid lineindicates that the VLSA with double switches and transmission gate access transistors (DSTA-VLSA) has no sensing dead zone. Because of the effect of both latching n MOS and latching pMOStransistors theσOS of the DSTA-VLSA is almost flat over all *V*BL regions. In this brief information ,it is assumed that *V*BL is greater than *V*BLB by ΔVBL. Thus, in the case of no process variation, *I*MP1 is larger than *I*MP2, and *I*MN1 is smaller than *I*MN2.

However, when the process variation is applied only to a latching n MOS pair, *V*OSN, which is the offset voltage caused by the latching n MOS pair, is not zero. When the *V*OSN Is positive, *I*MN1 increases. This can cause sensing failure when *I*MN1 is larger than *I*MN2 because of the large *V*OSN. As *V*BL decreases below *V*THN, the discharging current through the latching n MOSs decreases and charging current through the latching p MOSs increases, leading to a decrease in the effect of *V*OSN.

Similarly, when the process variation is applied only to a latching p MOS pair, *V*OSP, which is the offset voltage caused by the latching p MOS pair, is not zero. A s*V*BL increases beyond *V*DD − *V*THP, the charging current through the latching p MOSs decreases and the discharging current through the latching n MOSs increases, leading to a decrease in the effect of *V*OSP. When the process variation is applied to both the latching MOS and p MOS pairs, *V*OS is the sum of *V*OSN and *V*OSP.

IV. SIMULATION RESULT

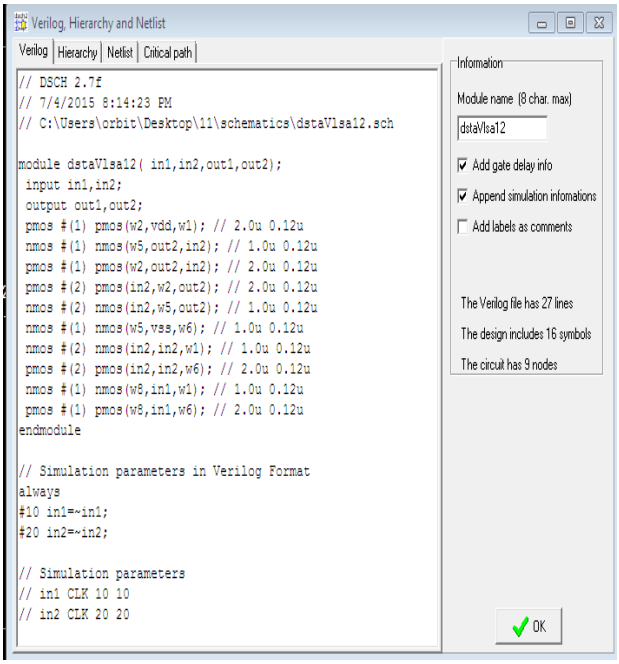

Fig 4.Generate verilog code

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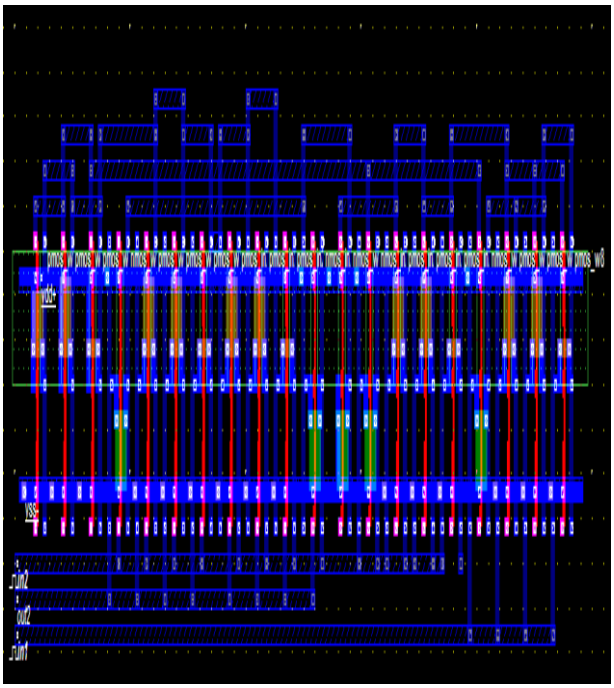

Fig 5 .layout based voltage latch sensing amplifier DSTA

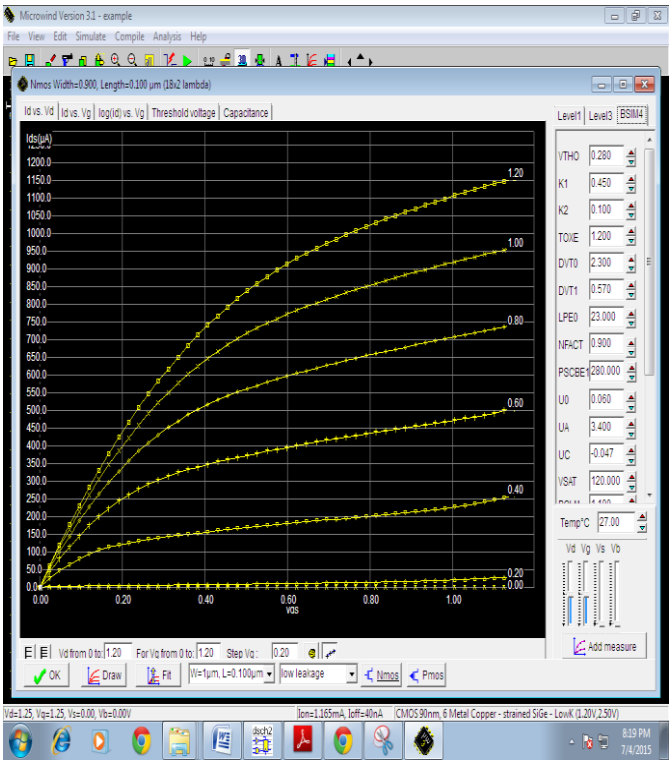

Fig 7.MOS characters of 45 nm technology

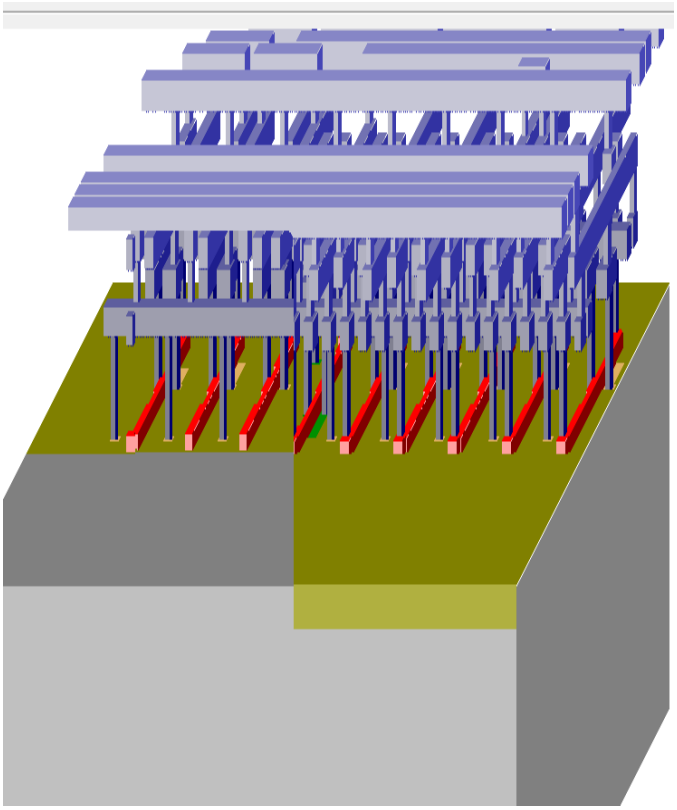

Fig 6 .3D design lay out diagram for VLSA-DSTA

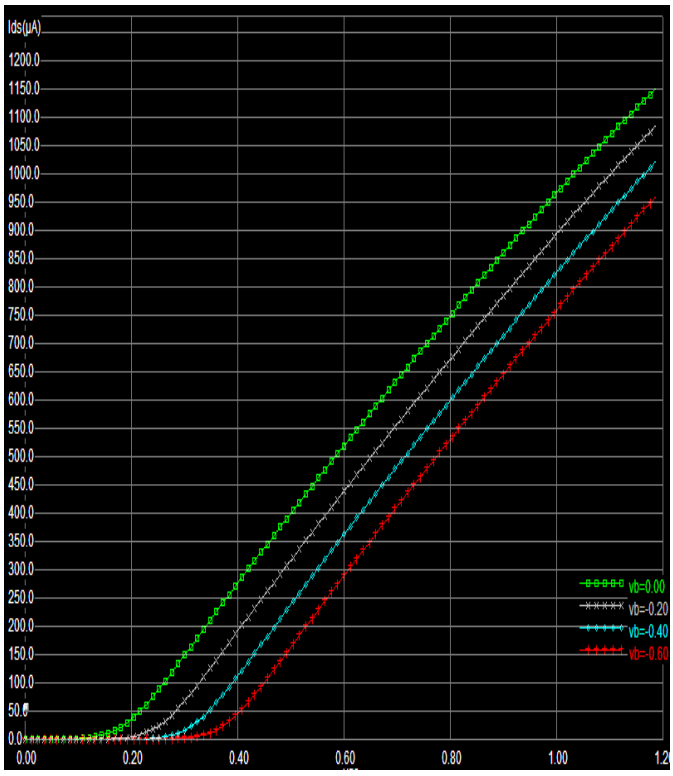

Fig 8.gate current vs gate voltage simulation verification.

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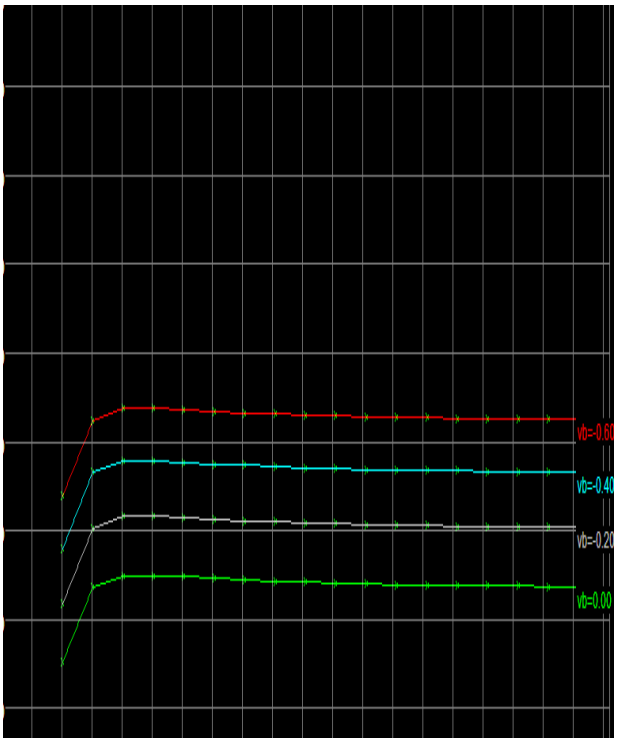

Fig 9. Threshold voltage simulation result

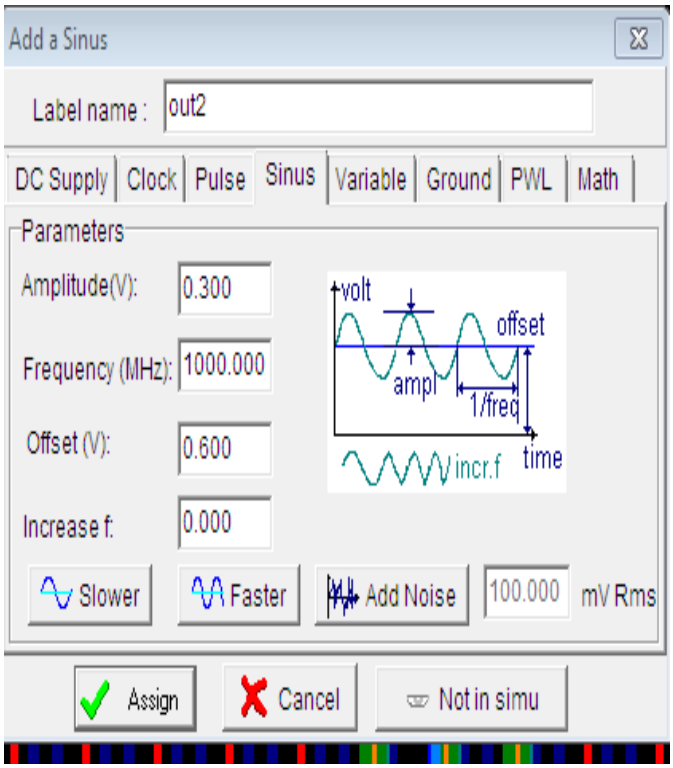

Fig 11. Amplitude verification of 45 nm technology

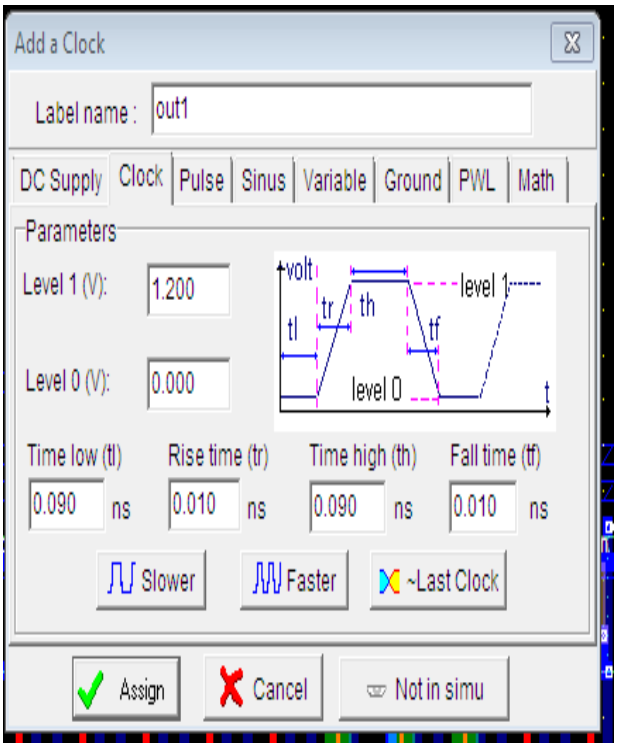

Fig 10 shows fall time and rise time

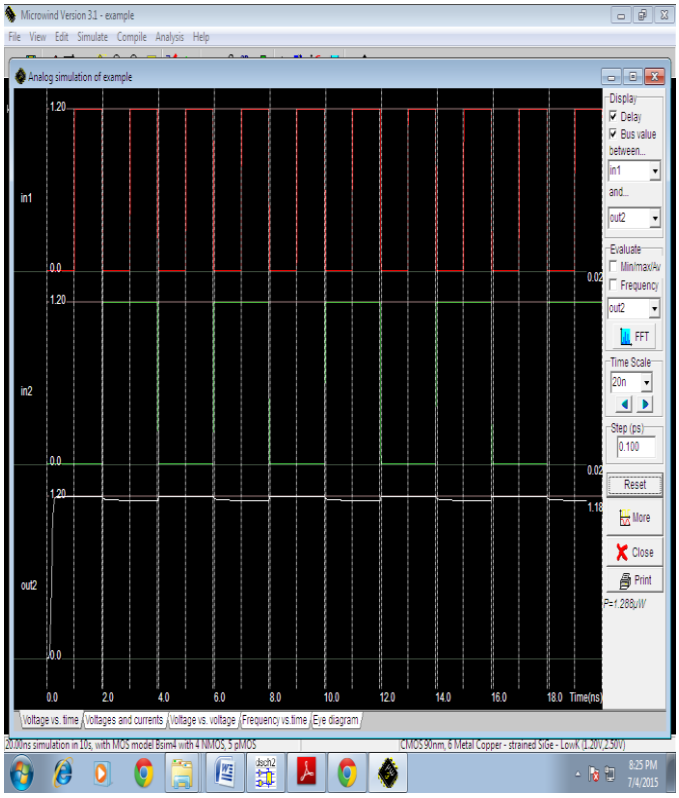

Fig 12.Voltage vs time simulation

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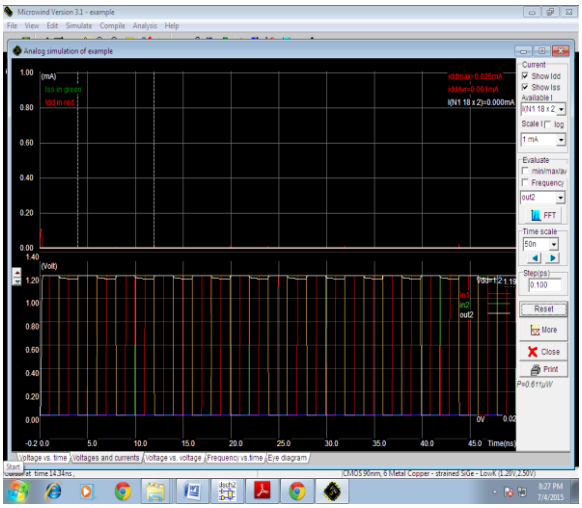

Fig 13. Voltage vs current simulation

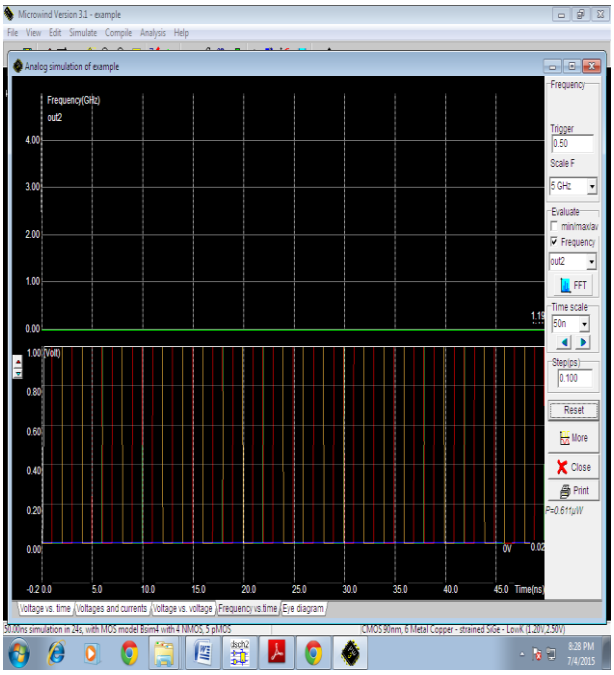

Fig 14 .frequency vs time simulation.

V. CONCLUSION

The input voltage region in which an SA cannot correctly detect the input voltage difference is called the sensing dead zone. Because each SA scheme has its own respective sensing dead zone, detailed knowledge of this zone is important for designing a high-yield memory. In this brief, we analyzed the sensing dead zones of the most popular latch-type SAs and proposed a suitable SA scheme according to the input voltage region .in this micro wind tool we find the minimum power delay ,and 40 MHZ frequency,5.88m V,0.024m A current values are observed. we verifying the less power compared to other technology in this project we find 0.114w power are calculated

VI. REFERENCES

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