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A Capacitor less LDO Regulator using Push–Pull Composite Power Transistor with A Sub-1 V Transient An Enhanced Output

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Abstract:
A yield capacitor less low-dropout (OCL-LDO) controller with a push–pull composite force transistor is introduced in this paper. Utilizing the proposed composite transistor, the non predominant parasitic posts can be pushed to higher frequencies, prompting great security. Moreover, the large number rate restriction at the door of the force transistor is enhanced incredibly by the proposed push–pull structure. Actualized and manufactured in UMC 65-nm CMOS innovation, the LDO controller involves just an dynamic region of 0.0096 mm2 . The exploratory results have demonstrated that the controller has the capacity work at VIN = 0.75 V and convey a most extreme burden current of 50 mA with a dropout voltage of under 250 mV. It expends a quiet current of 16.2 µA and has the capacity settle inside of 1.

I.INTRODUCTION

LOW-DROPOUT (LDO) controller is an imperative building block in present day VLSI circuit outlines. Contrasted and exchanging sort of controllers, LDO controller is frequently utilized to give a controlled and stable supply voltage to those commotion touchy simple/RF pieces, particularly under on-chip applications environment.

Routine LDO controller obliges an extensive off-chip capacitor in the scope of µF to guarantee strength. In this way, yield capacitor less LDO controller (OCLLDO) is favored for on-chip applications. Low-control utilization is a standout amongst the most discriminating parameters, particularly for compact electronic circuits . To diminish the force utilization, the working supply voltage must be lessened while tending to calm mindful outline. It is on the grounds that this is a standout amongst the best approaches to drag out the battery life of a convenient . Along these lines, it has an interest of a ultralow voltage LDO controller which can give a 0.5 V supply line to those coordinated circuits. Ultralow voltage outline forces a few difficulties for LDO controllers as far as soundness, headroom, and slew-rate issues

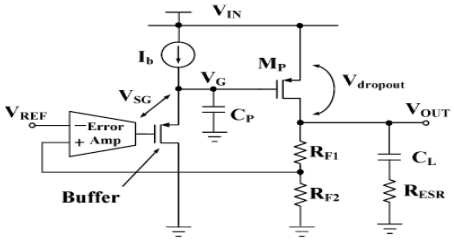

Fig. 1. Structure of the buffer based LDO regulator

As shown in Fig. 1, the buffer based LDO regulators require an additional *V*SG to ensure the operation. Under sub-1 V environment, the buffer based LDO regulator is difficult to fulfill the headroom budget. In addition, the parasitic capacitor *CP* associated at the gate of power transistor *MP* is greatly affected by the input supply *V*IN and the dropout voltage *V* dropout*(*max*)* = *(V*IN–*V*OUT*)* of regulator design. Consider a pMOS power transistor operates in saturation region, the required aspect ratio is given as

$$\frac{W}{L}=\frac{2I_{LOAD(\max)}}{\mu C_{OX}V_{dropout}\left(V_{IN}-V_G-V_{THP}-\frac{V_{dropout}}{2}\right)}\ldots\ldots\ldots(1)$$

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where μ, *C*ox, and VTHP are the mobility, gate capacitance per unit, and threshold voltage of power transistor, respectively. *VG* is defined as the power transistor's driver output voltage. *I* LOAD*(*max*)* is the maximum load current. To save silicon area the power transistor working in linear region can be adopted but at the expense of loop gain of the LDO regulator as the design tradeoff. The required aspect ratio becomes

$$\frac{W}{L} = \frac{I_{LOAD(\max)}}{\mu C_{OX} V_{dropout}\left(V_{IN} - V_G - V_{THP} - \frac{V_{dropout}}{2}\right)} \quad \ldots\ldots\ldots (2)$$

As can be observed in (1) and (2), the size of power transistor depends on multiple parameters. They are operating region, *I*LOAD*(*max*)*, *V*dropout, and *V*IN. In either approach, when both low voltage and/or low dropout are required, the size of the power transistor needs to be increased to compensate the reduction in the headroom, thus leading to the increase of *CP*. As a result, the parasitic capacitances increase significantly, causing the stability, and slew-rate problems.

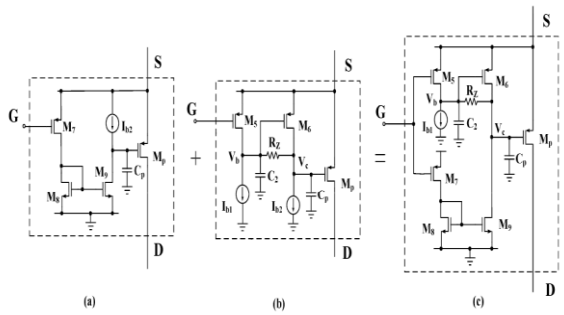

Fig. 2. (a) Conventional noninverting stage + power transistor. (b) Class-A composite power transistor [20]. (c) Proposed push–pull composite power

LDO regulators that can operate at sub-1 V supply voltage have been demonstrated. the body-bias technique is employed to reduce the threshold voltage *V*TH of the transistors. However, in nanometer CMOS technology devices, the body-bias threshold reduction for low-voltage operation is not effective due to small value of body factor. In addition, the design only supports a very limited output capacitor value. No output capacitor *CL* is reported. It may have difficulty for use in higher on-chip capacitive load *CL* that lies in the range of few tens of pF. The *Q*-reduction technique is introduced to permit the low-voltage stable LDO operation. Due to the fact that the output nodes of each stage are loaded with the compensation capacitors, the slew-rate of the LDO regulator is greatly affected. Although a LDO regulator with ultralow-quiescent current of 103 nA is reported by employing a digital error amplifier (EA), the large voltage dip of 300 mV and setting time of 400 μs might not meet the speed requirements in the ultralow-voltage applications. demonstrates a gain-enhanced flipped voltage follower-based LDO regulator that consumes only 8 μA. However, it draws a minimum *I*LOAD of 3 mA to ensure stability for *CL* of 50 pF. Hence, it is not suitable for lowload current applications. Push–pull technique is demonstrated to improve the slew-rate problem. However, they need the minimum *I*LOAD requirement to maintain stability. an assisted push–pull output stage is proposed to enhance the transient response without requiring any compensation capacitor. However, the transient enhancement circuit is a complicated structure which also requires additional biasing voltage. In addition, it suffers from stability problem when *I*LOAD is less than 100 μA. A sub-1 V OCL-LDO regulator with a push–pull composite power transistor is presented. By using the proposed push– pull composite power transistor, without any minimum *I*LOAD requirement, the stability is enhanced because the non dominant parasitic poles can be pushed to higher frequencies. In addition, the slew-rate limitation at the gate of the power transistor is improved greatly by the proposed push–pull structure without increasing the static biasing current. It permits the use of simple frequency compensation scheme with small compensation capacitor.

II.EXISTING SYSTEM:

A. The composite transistors:

Because the complementary-symmetry circuits of Sziklai offer many advantages to the designer of an extremely precise linear power amplifier, it is desirable to develop techniques to circumvent the problems that arise due to the lack of suitable power transistors.

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Figure 1 shows the basic complementary-symmetry circuit of Sziklai in which the common emitter configuration is used in the output stage (17). This circuit may be modified as shown in Figure 2 so that the driver-output stage combination forms a direct-coupled group with no inherent d-c unbalance, quiescent voltage levels at the ground potential, and push-pull operation without the need for an output transformer. Impedances connected in boxes 1 and 2 can be used to provide a very versatile local feedback. The use of this circuit is limited by the non-availability of suitable transistors in the output stage. The purpose of this chapter is to describe the development of complementary-symmetry composite transistors which have characteristics much more suitable to use in this circuit than any available single transistor.

B.The N-p-n Composite Transistor:

A p-n-p transistor in the common-collector configuration when driven by a current source behaves very much like an n-p-n transistor in the common-emitter configuration when driven by-a current source. Thus the two transistors shown in Figure 3a

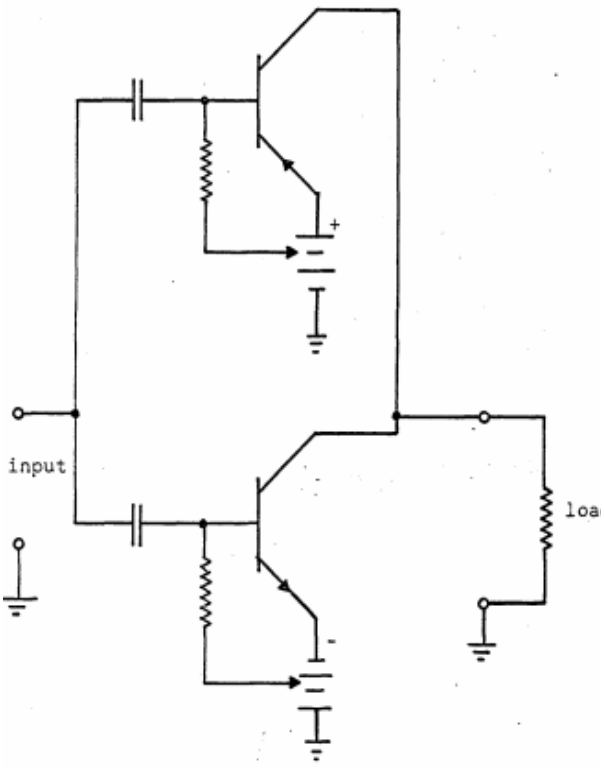

Figure 1. The basic complementary-symmetry circuit

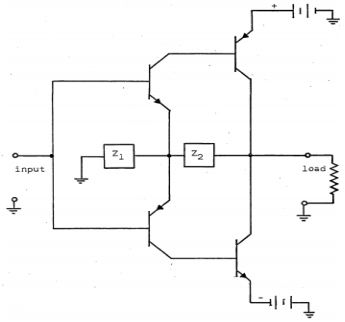

Figure 2. A modified form of complementary-symmetry circuit

behave somewhat like a single n-p-n power transistor. This composite transistor has the advantage that the power is largely dissipated by the p-n-p power transistor and a much smaller and readily-available n-p-n unit can be used in the driver stage. It has the disadvantage that the current gain and cutoff frequency are first order functions of the current gains and cutoff frequencies of the individual transistors. Any attempt to match such a composite transistor to an enantiomorphic counterpart would at best be a very tedious process and as a practical matter would probably be impossible. The addition of two impedances as shown in Figure 3b provides local series feedback and results in a composite n-p-n transistor whose characteristics are almost independent of the characteristics of the individual transistors as will be shown by the following analysis. If the bias levels are ignored for the present, the composite transistor of Figure 3b may be represented for small-signal purposes by the set of two-port networks shown in Figure 4a. Note.' the addition of a current-s our ce input and a load to complete the circuit as it will appear in the final form. In the analysis, a two-port network will be represented by a matrix using the standard notation as given by Shea (16). The subscript will indicate the particular element of a matrix and the superscript will indicate the matrix to which it belongs. i \z Thus b^2 will be the first-row, second-column element of the B matrix for the fourth two-port network. The hybrid-tt model of the transistor will be

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used as the standard model for all of the following analysis (15). This model represents the transistor quite satisfactorily for small-signal analysis below the a-cutoff frequency and its parameters are readily interpreted as physical quantities.

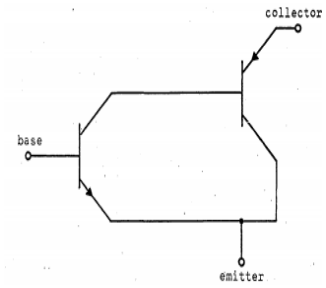


Figure 3a. One possible composite n-p-n transistor

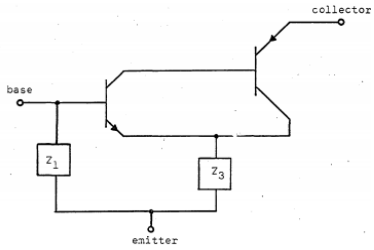


Figure 3b. The final form of the composite n-p-n transistor

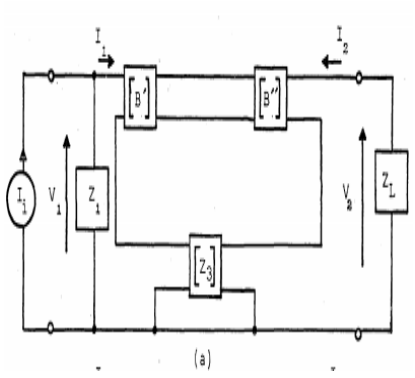


Figure 4. Sequence of two-port networks used in the analysis of the n-p-n composite transistor

c.Linear regulators

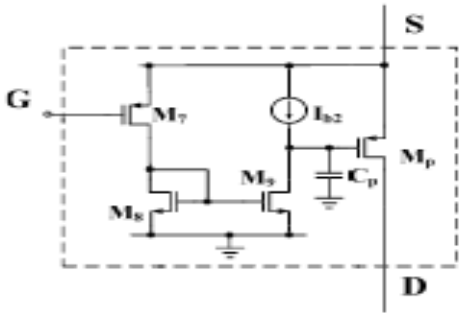
There are two types of linear regulators: standard linear regulators and low dropout linear regulators (LDOs). The difference between the two is in the pass element and the amount of headroom, or dropout voltage, required to maintain a regulated output voltage. The dropout voltage is the minimum voltage required across the regulator to maintain regulation. A 3.3 V regulator that has 1 V of dropout requires the input voltage to be at least 4.3 V. The input voltage minus the voltage drop across the pass element equals the output voltage. This brings up the question, "What is the minimum voltage drop across the pass element?" The answer to this question depends upon several factors.

III.PROPOSED SYSTEM

PROPOSED PUSH–PULL COMPOSITE POWER TRANSISTOR

A. Class-A Composite Power Transistor:

Under ultralow-voltage operating environment, to have enough loop gain, LDO regulators with multistage structure are often adopted. To maximize the voltage swing, output stage with only two transistors [shown in Fig. 2(a)] are allowed to serve as a power transistor driver. By adopting this structure, the LDO regulator is potentially unstable because of the multiple high-impedance nodes in the control loop. To solve this problem, a complex frequency compensation technique [5] is required. To avoid the need of complex frequency compensation, a Class-A composite power transistor is proposed in [20] and [21].



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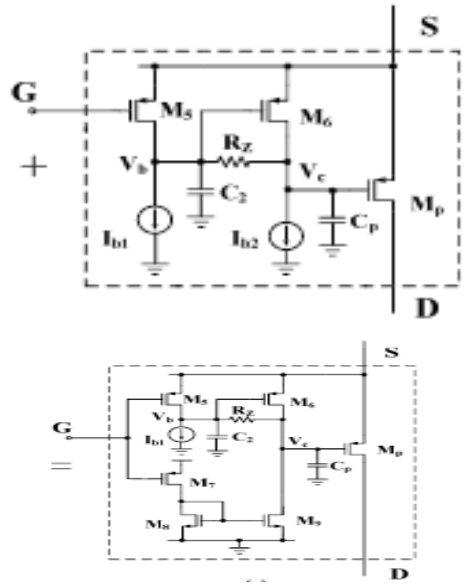

Fig. 2. (a) Conventional noninverting stage + power transistor. (b) Class-A composite power transistor [20]. (c) Proposed push–pull composite power

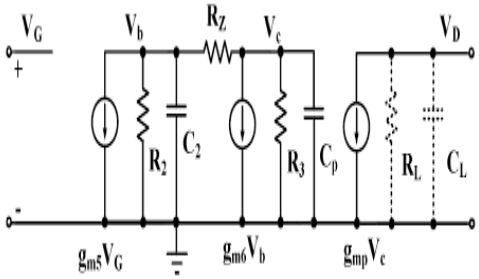

Fig. 3. Small-signal model of the Class-A composite power transistor

which has an open-loop structure, is shown in Fig. 2(b). The smallsignal model of the composite power transistor is shown in Fig. 3, with *RL* and *CL* representing the effective resistive and capacitive load, respectively. This loading effect will be included in the analysis when the composite transistor forms the circuit in the subsequent LDO circuit topology.

By applying the nodal analysis to the small-signal model that excludes the loading effect, the frequency-dependent transconductance *G*mp*(*Class-A*)* of the composite power transistor which is defined as the ratio of output current *g*mp*Vc* to input voltage *VG* can be approximated as

$$G_{mp(class-A)} = \frac{g_{m5}R_Z}{\left(1+\frac{C_p(R_2+R_Z)}{g_{m6}R_2}S\right)\left(1+\frac{C_2R_ZR_2}{R_2+R_Z}S\right)}g_{mp} \ldots\ldots (3)$$

where *g*mi is the transconductance for the respective devices, *Ci* and *Ri* are the respective lumped parasitic capacitance and resistance at the output of each stage. As can be seen from (3), the transconductance consists of two poles. In general, the parasitic capacitor *C*2 is small. Therefore, the second pole can be ignored. Due to the shunt feedback resistor *RZ*, the output impedance of the Class-A driver approximately equals to (*R*2 + *RZ*)/*R*2*gm*6. If *R*2 _ *RZ* , the output impedance ≈1/*gm*6. This low impedance will be helpful in the context of stability of the LDO regulator. In advanced nanometer CMOS technology, the value of *RZ* could be close to *R*2 such that the output impedance is ∼2/*gm*6. In short, the Class-A driver can be viewed as a buffer stage with gain of *gm*5*RZ* . Therefore, it offers the advantage of higher stability over other designs. Furthermore, the transconductance and bandwidth of the composite power transistor can be adjusted independently. However, the main drawback of this Class- A composite power transistor is that the sinking capability at node *Vc* is limited by the bias current *Ib*2. To turn-on the LDO regulator fast, the charges at node *Vc* has to be discharged quickly. However, the parasitic capacitor *Cp* is relatively large in ultralow-voltage LDO regulator. This is due to large power transistor dedicated to low-supply operation. Thus, for a limited bias current *Ib*2, the turn-on speed of the power transistor *MP* is greatly affected. This turns out that the OCL-LDO regulator will exhibit a large undershoot. This may not be acceptable, especially in the ultralow-voltage environment.

To solve the sinking capability problem in the Class-A composite power transistor, a modified push–pull composite power transistor is shown in Fig. 2(c). The proposed circuit technique is to combine the conventional noninverting stage and Class-A driver together. As a result, the sourcing and sinking capability is not limited by the biasing current.

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B. Push–Pull Composite Power Transistor:

The operation of the push–pull composite power transistor in Fig. 2(c) is explained in the following. The static bias current source *Ib*2 is replaced by a signal-dependent current source formed by transistors *M*7 −*M*9. Consequently, the bias current of transistor *M*6 and *M*9 depends on the voltage level at the gate of the composite power transistor. With the signal dependent current source, the sinking capability at node *Vc* is no longer limited by the static current source *Ib*2. The proposed low-voltage push–pull structure will provide extra transient current which is much larger than the static bias current at node *Vc* during transient event.

$$G_{mp(push-pull)} = \frac{\left(g_{m5}R_Z + \frac{g_{m7}}{g_{m6}}\right)\left(1 + \frac{g_{m7}C_2}{g_{m5}g_{m6}}S\right)}{\left(1 + \frac{C_p(R_2+R_Z)}{g_{m6}R_2}S\right)\left(1 + \frac{C_2R_ZR_2}{R_2+R_Z}S\right)} \times g_{mp}$$

……. (4)

From (4), it can be seen that the transconductance of the push–pull composite power transistor is larger than that of

the Class-A counterpart due to the signal-dependent current source. In addition, the signal-dependent current source also introduces a left-hand-plane zero. However, it is a function of parasitic capacitance and can be located at high-frequency easily. Furthermore, the parasitic pole is also located at high frequency. Similar to the Class-A version, the transconductance and bandwidth are independent of each other.

IV.PROPOSED LDO REGULATOR:

The schematic of the proposed LDO regulator with push–pull composite power transistor is show in Fig. 4. The EA is composed by five transistors *M*1–*M*4 and *Mb*1 with *M*1 = *M*2 and *M*3 = *M*4. The transistors *M*1 and *M*2 form a differential pair whereas the transistors *M*3 and *M*4 form a current mirror. The transistor *Mb*1 serves as the current source of EA. The push–pull composite power transistor is formed by a low-voltage embedded gain stage (*M*5–*M*9) and a power transistor (*MP*). *Cm* is the Miller compensation capacitor whereas *Cp* is the lumped parasitic capacitance at the gate of *MP*. The feedback resistive divider network is realized by resistors *R*F1 and *R*F2. The on-chip capacitance and load current are represented by *CL* and *RL* , respectively. The push–pull stage can be viewed as a buffer stage in the LDO regulator in [1] and [3]. With the proposed push–pull composite power transistor, the high-impedance node at the output of the EA and the parasitic capacitance node at the gate of the conventional power transistor are decoupled. It benefits the LDO regulator to have a high-stability performance as revealed by the analysis.

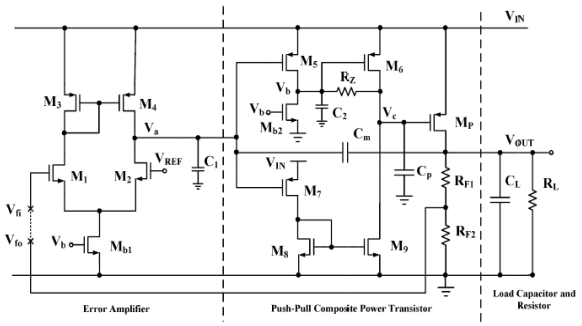

Fig. 4. Schematic of the proposed LDO regulator.

A. Stability Analysis:

The simplified small-signal model of the proposed LDO regulator is shown in Fig. 5. The stability is investigated using the loop-gain transfer function of the regulation loop. The transfer function is obtained as follows:

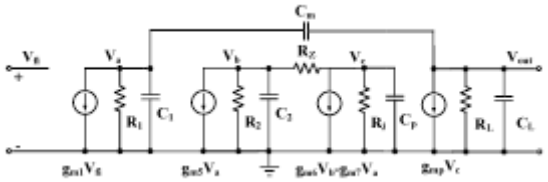

Fig. 5. Small-signal model of the proposed LDO regulator.

$$A_v = \frac{-g_{m1}g_{mp}A_ER_1R_L\left[1+\left(\frac{g_{m7}R_ZC_2}{g_{m6}A_E}-\frac{C_m}{g_{mp}A_E}\right)S\right]}{\left(g_{mp}A_ER_1R_LS\right)\left(1+\frac{\frac{g_{mp}g_{m7}R_ZC_2}{g_{m6}}}{g_{m6}A_k}+\frac{C_pC_L(R_2+R_Z)}{g_{mp}g_{m6}A_ER_2}\right)}$$

(5)

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where $AE = gm5RZ + gm7/gm6$ is the gain of the push–pull stage. The derivation is based on the following ssumptions:

1) $gm1R1 >> 1$, $gm5R2 >> 1$, and $gm6R3 >> 1$ and

2) $CL >> Cm >> C1$. From the transfer function, it can be observed that

there are one dominant pole, a pair of complex poles and one zero. The dc gain and dominant pole $p-3dB$ are obtained as

$$A_{DC} = g_{m1} g_{mp} A_E R_1 R_L \text{.....(6)}$$

$$P=3db=\frac{1}{C_m g_{mp} A_E R_1 R_L} \text{.....(7)}$$

Since the load current varies greatly, the stability of the LDO regulator will be discussed at different loading onditions. There are two cases to be considered.

1) Low to Moderate Load Current:

Under this case, the transistor *MP* is working in subthreshold region. The transconductance *g*mp is small. Therefore, $Cm/gmpAE >> gm7RZC2/gm6AE$, $CL >> gm7gmpRZC2/gm6$ and the transfer function can be simplified as

$$A_v = \frac{-g_{m1} g_{mp} A_E R_1 R_L \left(1 + \frac{C_m}{g_{m6} A_E} S\right)}{\left(1 + C_m g_{mp} A_E R_1 R_L S\right)\left(1 + \frac{C_1}{g_{m6} A_k} + \frac{C_p C_L (R_2 + R_Z)}{g_{mp} g_{m6} A_E R_2}\right)}$$

(8)

Both the dc gain and dominant pole remain the same. Stability of this condition is determined by the location of the

RHP zero and the nondominant complex poles. Of particular interest, the location of the RHP zero is shifted to higher frequencies by a factor of *AE* . The location of the nondominant complex poles can be approximately modeled as

$$\left| P_{2,3} = \sqrt{\frac{g_{mp} g_{m6} A_E R_6}{C_p C_L (R_2 + R_Z)}} \right|$$

(9)

As shown in (9), the nondominant complex poles are a function of *g*mp which is proportional to the square root of

*I*LOAD. This implies that the nondominant complex poles are shifted to higher frequencies when *I*LOAD increases. Therefore, the worst case stability happens at no load condition. The stability condition can be achieved by adjusting the compensation capacitor *Cm* and locating the nondominant complex poles beyond the unity gain frequency (UGF) which is about 1 MHz in this design.

2) Moderate to High-Load Current:

Under this case, the transistor *MP* is working in saturation region. The transconductance *g*mp is large. Therefore, $g_{m7}R_ZC_2/g_{m6}A_E >> C_m/g_{mp} A_E$, $gm7gmpR_ZC_2/g_{m6} \_ CL$ and the transfer

$$\frac{-g_{m1} g_{mp} A_E R_1 R_L \left(1 + \frac{g_{m7} R_Z C_2}{g_{m6} A_E} S\right)}{\left(1 + C_m g_{mp} A_E R_1 R_L S\right)\left(1 + \frac{g_{m7} R_Z C_2}{g_{m6} A_k} + \frac{C_p C_L (R_2 + R_Z)}{g_{mp} g_{m6} A_E R_2}\right)}$$

function can be simplified to

The RHP zero is replaced by a high-frequency LHP zero. It can be noticed that the location of the nondominant complex poles still can be modeled by (9). Due to the large *g*mp, the nondominant poles are shifted to even higher frequencies. Therefore, the stability is ensured. Table II summaries the calculated poles and zero location.

By adopting the third-order Butterworth response, the dimension condition of the Miller compensation capacitor *Cm*

can be found by

$$C_m = \frac{2\sqrt{2} g_{m1}}{P_{2,3}} = 2 g_{m1} \sqrt{\frac{2 C_p C_L (R_2 + R_Z)}{g_{m6} g_{mp} A_E R_2}}$$

(11)

To ensure the stability, the *Cm* needs to be found at maximum *CL* and minimum *g*mp conditions. From (11), the dimension condition of the *Cm* is proportional to the square root of the product of *Cp* and *CL* . This implies that the required compensation capacitor size

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is smaller when compared with that of the conventional Miller compensation scheme which is directly proportional to the size of *CL* . As a result, the silicon area can be reduced. Furthermore, the size of *Cm* can be further reduced by increasing *gm*6, *gm*5, or g_{mp} .

B.Large Signal Dynamic Behaviors

As shown in Fig. 9(a), when the *I*LOAD suddenly increases, *V*OUT drops rapidly and this drop is sensed and amplified by the EA. This undershoot will force the transistor *M*6 and *M*9 to be in off and on, respectively. As a result, the gate of *MP* is discharged by *IM*9. The power transistor is then turned on to supply the required *I*LOAD. Similarly, as showed in Fig. 9(b), when *I*LOAD suddenly decreases, *V*OUT rises rapidly. This will create an overshoot that appears at the gate of both transistors *M*5 and *M*7. This turns out that the transistors *M*6 and *M*9 are on and off, respectively. The transistor *M*6 injects current *IM*6 to charge the gate of *MP*, causing the power transistor to turn-off to decrease the *I*LOAD. Fig. 10 shows the simulated exemplary transient currents of transistor *M*6 and *M*9. As can be observed, when the

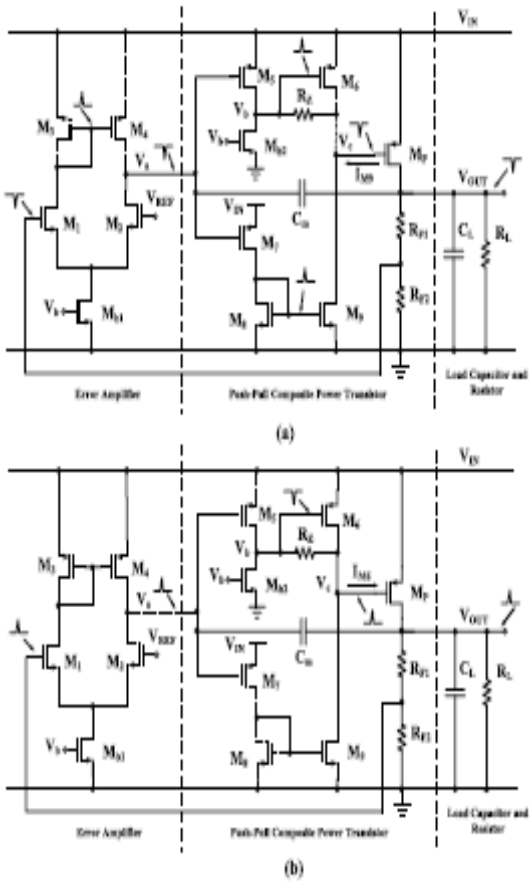
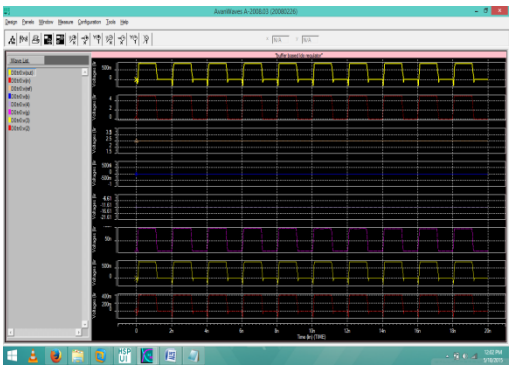


Fig. 9. Operation principle of the proposed LDO regulator (a) undershoot and (b) overshoot.

V. RESULTS:

Buffer based LDO Regulator (Existing Design)



here V(out) represents the output and V(in) represents the input.

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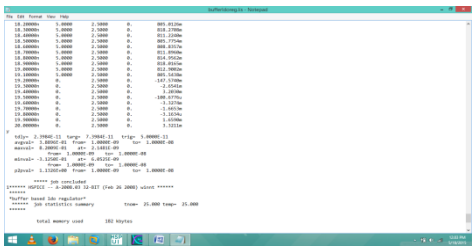
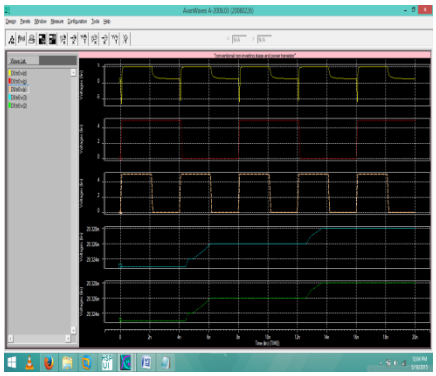
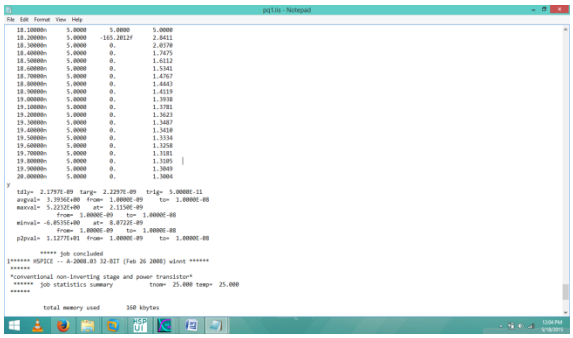


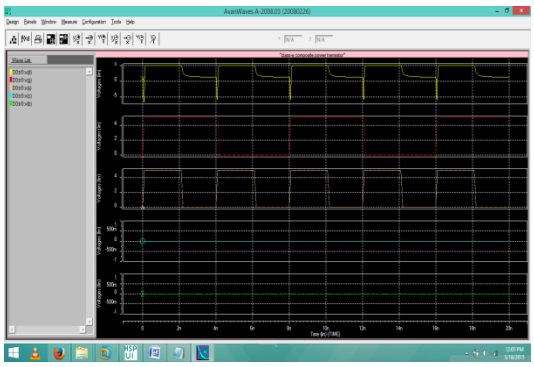
conventional non-inverting stage + power transistor



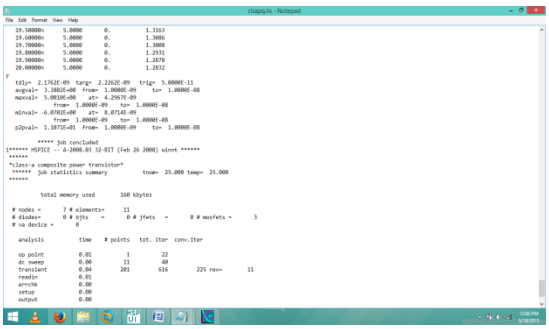
here v(g) is input and V(d) is output.



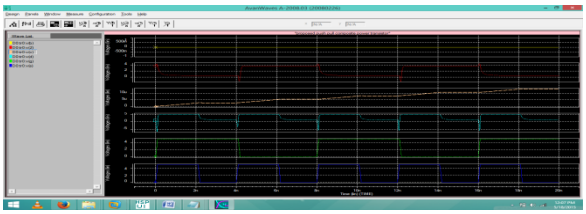
class-A composite power transistor



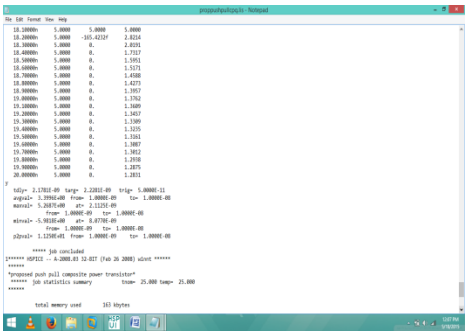
here v(g) is input and v(d) is output.



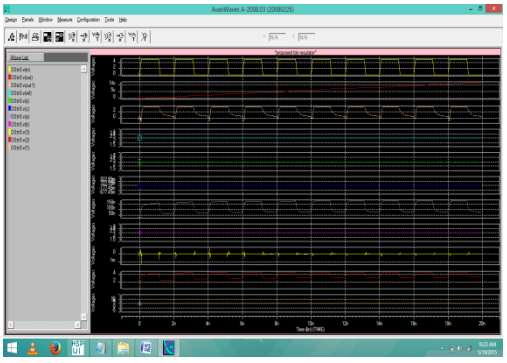
proposed push pull composite power transistor



here v(g) is input and v(d) is output.



Proposed LDO Regulator



Here v(in) is input and V(out1) is output. v(3) represents the transients in the regulated output.

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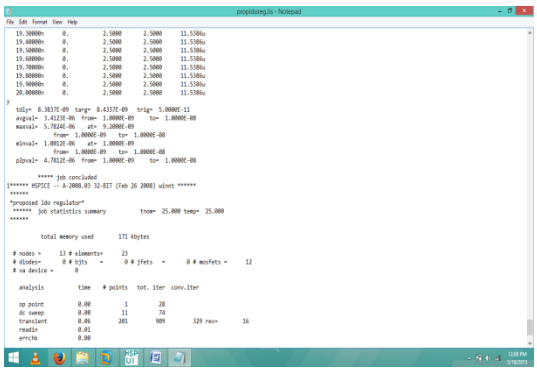
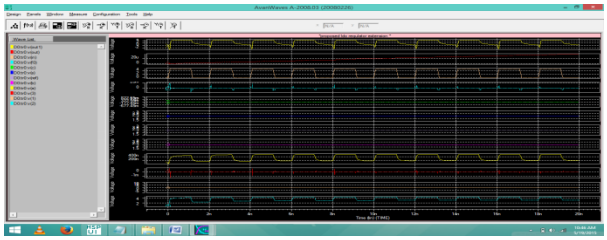
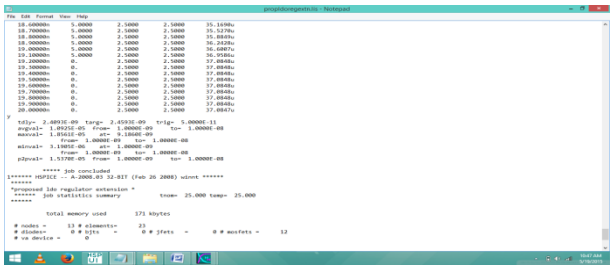


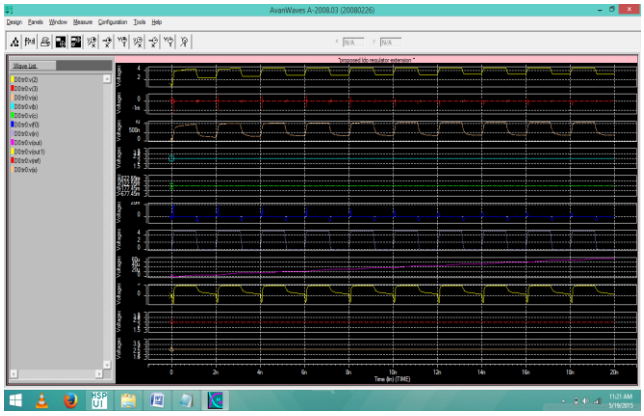
Project Extension – with proper sizing of transistors



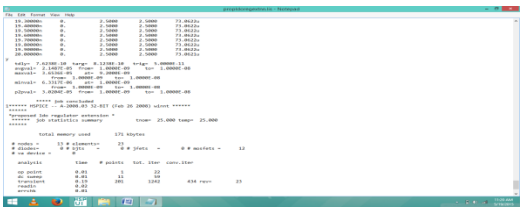
Here V(in) is input and V(out1) is output.



Project Extensionn – if area of pmos is not a constraint



Here v(in) is input and V(out) is output.



Hence the proposed LDO Regulator is best in terms of power delay Product. also further if proper sizing of transistors is maintained then the power delay product can be minimized

VI.CONCLUSION:

A transient-enhanced OCL-LDO controller with push–pull composite power transistor actualized in 65-nm CMOS innovation has been presented. With the proposed low voltage circuit building design, the LDO controller can work at sub-1 V supply. Moreover, the proposed push–pull structure enhances the heap transient reaction. Both undershoot and overshoot are enhanced significantly when contrasted and the partners. At last, with the composite power transistor, the non dominate are situated at higher frequencies. Therefore, the compensation capacitor can be made little. In perspective of silicon range, the littler compensation capacitor prompts a little territory LDO controller. This is extremely suitable for VLSI execution in which the silicon overhead of the proposed controller for completely on-chip applications is small.

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