ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Efficient Fixed- Point LMS Adaptive Filter Implementation on FPGA

G.Sirisha
M.Tech Student,
Department of ECE, Abdulkalam Institute of Technological Sciences, Kothagudem, Telangana, India.

M.Venkat Ratnam
Assistant Professor,
Department of ECE, Abdulkalam Institute of Technological Sciences, Kothagudem, Telangana, India.

G.Rajaiah
Professor & HoD,
Department of ECE, Abdulkalam Institute of Technological Sciences, Kothagudem, Telangana, India.

ABSTRACT:

This paper, we present an efficient architecture for the implementation of a delayed least mean square adaptive filter. For achieving lower adaptation-delay and area-delay-power efficient implementation, we use a novel partial product generator and propose a strategy for optimized balanced pipelining across the time-consuming combinational blocks of the structure. From synthesis results, we find that the proposed design offers nearly 17% less area-delay product (ADP) and nearly 14% less energy-delay product (EDP) than the best of the existing systolic structures, on average, for filter lengths N = 8, 16, and 32. We propose an efficient fixed-point implementation scheme of the proposed architecture, and derive the expression for steady-state error. We show that the steady-state mean squared error obtained from the analytical result matches with the simulation result. Moreover, we have proposed a bit-level pruning of the proposed architecture, which provides nearly 20% saving in ADP and 9% saving in EDP over the proposed structure before pruning without noticeable degradation of steady-state-error performance.

Index Terms— ***Adaptive filters, circuit optimization, fixed-point arithmetic, least mean square (LMS) algorithms.***

INTRODUCTION:

THE LEAST MEAN SQUARE (LMS) adaptive filter is the most popular and most widely used adaptive filter, not only because of its simplicity but also because of its satisfactory convergence performance [1], [2]. The direct-form LMS adaptive filter involves a long critical path due to an inner-product computation to obtain the filter output. The critical path is required to be reduced by pipelined implementation when it exceeds the desired sample period. Since the conventional LMS algorithm does not support pipelined implementation because of its recursive behavior, it is modified to a form called the delayed LMS (DLMS) algorithm [3]–[5], which allows pipelined implementation of the filter. A lot of work has been done to implement the DLMS algorithm in systolic architectures to increase the maximum usable frequency [3], [6], [7] but, they involve an adaptation delay of ~ N cycles for filter length N, which is quite high for largeorder filters. Since the convergence performance degrades considerably for a large adaptation delay, Visvanathan et al. [8] have proposed a modified systolic architecture to reduce the adaptation delay. A transpose-form LMS adaptive filter is suggested in [9], where the filter output at any instant depends

Existing System:

The weights of LMS adaptive filter during the nth iteration are updated according to the following equations [2].

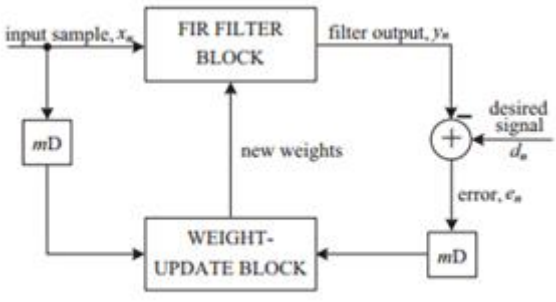

Fig. 1. Structure of the conventional delayed LMS adaptive filter.

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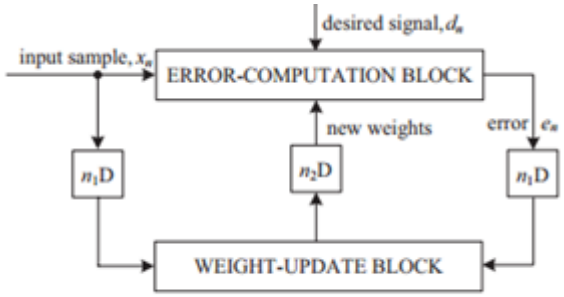
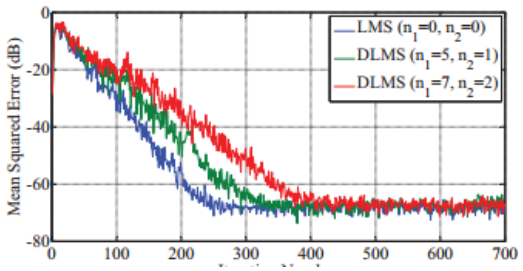


Fig. 2. Structure of the modified delayed LMS adaptive filter.

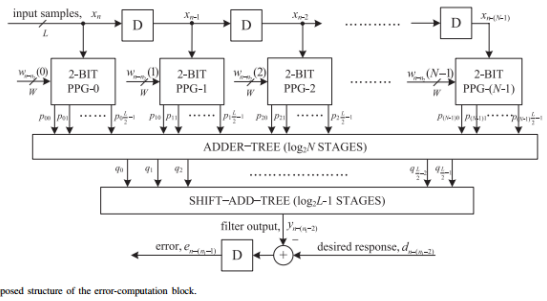
dn is the desired response, yn is the filter output, and en denotes the error computed during the nth iteration. μ is the step-size, and N is the number of weights used in the LMS adaptive filter. In the case of pipelined designs with m pipeline stages, the error en becomes available after m cycles, where m is called the "adaptation delay." The DLMS algorithm therefore uses the delayed error en−m, i.e., the error corresponding to (n − m)th iteration for updating the current weight instead of the recent-most error.



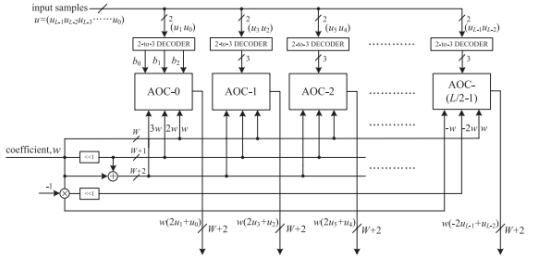
We notice that, during the weight update, the error with n1 delays is used, while the filtering unit uses the weights delayed by n2 cycles. The modified DLMS algorithm decouples computations of the error-computation block and the weight-update block and allows us to perform optimal pipelining by feedforward cut-set retiming of both these sections separately to minimize the number of pipeline stages and adaptation delay. The adaptive filters with different n1 and n2 are simulated for a system identification problem.

Proposed System:

As shown in Fig. 2, there are two main computing blocks in the adaptive filter architecture: 1) the error-computation.



Proposed structure of the error-computation block.



. 5. Proposed structure of PPG. AOC stands for AND/OR cell.

Fixed-Point Design Considerations For fixed-point implementation

The choice of word lengths and radix points for input samples, weights, and internal signals need to be decided. Fig. 9 shows the fixed-point representation of a binary number. Let (X, Xi) be a fixed-point representation of a binary number where X is the word length and Xi is the integer length. The word length and location of radix point of xn and wn in Fig. 4 need to be predetermined by the hardware designer taking the design constraints, such as desired accuracy and hardware complexity, into consideration. Assuming (L, Li) and (W, Wi), respectively, as the representations of input signals and filter weights, all other signals in Figs. 4 and 8 can be decided as shown in Table II. The signal pij , which is the output of PPG block (shown in Fig. 4), has at most three times the value of input coefficients. Thus, we can add two more bits to the word length and to the integer length of the coefficients to avoid overflow. The output of each stage in the adder tree in Fig. 7 is one bit more than the size of input signals, so that the fixed-point representation of the output of the adder tree with log2 N stages becomes (W + log2 N + 2, Wi + log2 N + 2). Accordingly, the output of the shift–add tree would be of the form (W +L+log2 N, Wi +Li+ log2 N), assuming that no truncation of any least significant bits

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International Journal & Magazine of Engineering, Technology, Management and Research
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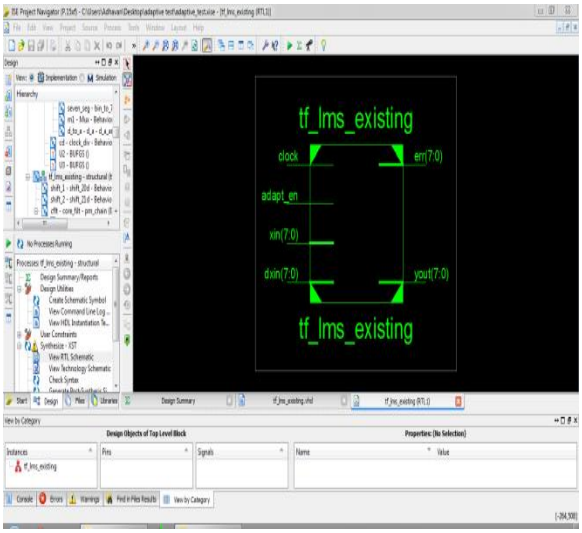
(LSB) is performed in the adder tree or the shift–add tree. However, the number of bits of the output of the shift–add tree is designed to have W bits. The most significant W bits need to be retained out of (W + L + log2 N) bits, which results in the fixed-point representation (W, Wi + Li +log2 N) for y, as shown in Table II. Let the representation of the desired signal d be the same as y, even though its quantization is usually given as the input. For this purpose, the specific scaling/sign extension and truncation/zero padding are required. Since the LMS algorithm performs learning so that y has the same sign as d, the error signal e can also be set to have the same representation as y without overflow after the subtraction. It is shown in [4] that the convergence of an N-tap DLMS adaptive filter with n1 adaptation delay will be ensured if 0 <μ< 2 (σ2 x (N − 2) + 2n1 − 2)σ2 x (5) where σ2 x is the average power of input samples. Furthermore, if the value of μ is defined as (power of 2) 2−n, where n ≤ Wi +Li +log2 N, the multiplication with μ is equivalent to the change of location of the radix point. Since the multiplication with μ does not need any arithmetic operation, it does not introduce any truncation error. If we need to use a smaller step size, i.e., n > Wi + Li +log2 N, some of the LSBs of en need to be truncated. If we assume that n = Li + log2 N, i.e., μ = 2−(Li+log2 N), as in Table II, the representation of μen should be (W, Wi) without any truncation. The weight increment term s (shown in Fig. 8), which is equivalent to μen xn, is required to have fixed-point representation (W + L, Wi + Li). However, only Wi MSBs in the computation of the shift–add tree of the weight-update circuit are to be retained, while the rest of the more significant bits of MSBs need to be discarded. This is in accordance with the assumptions that, as the weights converge toward the optimal value, the weight increment terms become smaller, and the MSB end of error term contains more number of zeros. Also, in our design, L − Li LSBs of weight increment terms are truncated so that the terms have the same fixed-point representation as the weight values. We also assume that no overflow occurs during the addition for the weight update. Otherwise, the word length of the weights should be increased at every iteration, which is not desirable. The assumption is valid since the weight increment terms are small when the weights are converged. Also when overflow occurs during the training period, the weight updating is not appropriate and will lead to additional iterations to reach convergence. Accordingly, the updated weight can be computed in truncated form (W, Wi) and fed into the errorcomputation block.

Computer Simulation of the Proposed DLMS Filter

The proposed fixed-point DLMS adaptive filter is used for system identification used in Section II. μ is set to 0.5, 0.25, and 0.125 for filter lengths 8, 16, and 32, respectively, such that the multiplication with μ does not require any additional circuits. For the fixed-point simulation, the word length and For the fixed-point simulation, the word length and radix point of the input and coefficient are set to L = 16, Li = 2, W = 16, Wi = 0, and the Gaussian random input xn of zero mean and unit variance is scaled down to fit in with the representation of (16, 2). The fixed-point data type of all the other signals are obtained from Table II. Each learning curve is averaged over 50 runs to obtain a clean curve. The proposed design was coded in C++ using SystemC fixed-point library for different orders of the band-pass filter, that is, N = 8, N = 16.

Existing circuit



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International Journal & Magazine of Engineering, Technology, Management and Research
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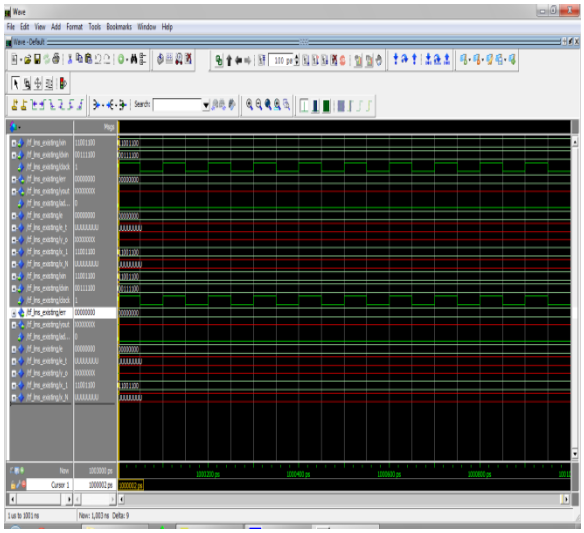
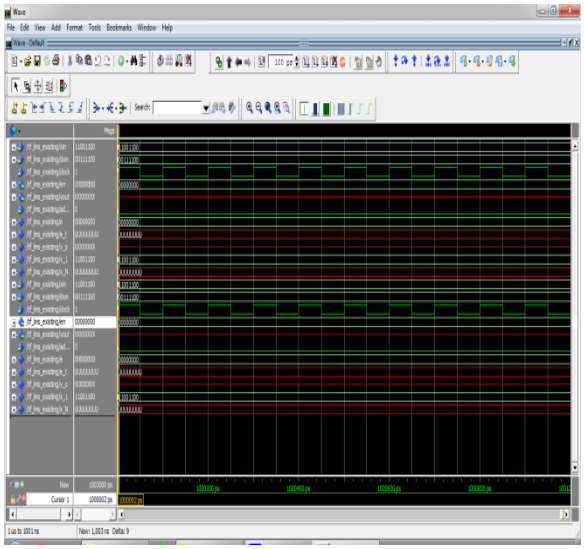
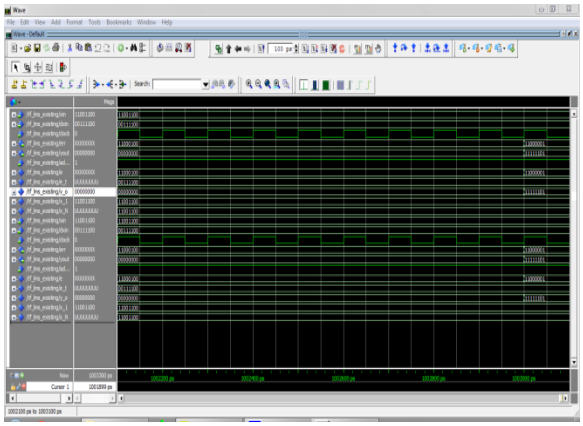
EXISTING DESIGN RESULT:

X in=10001100, din=10010010,adapt enable=0



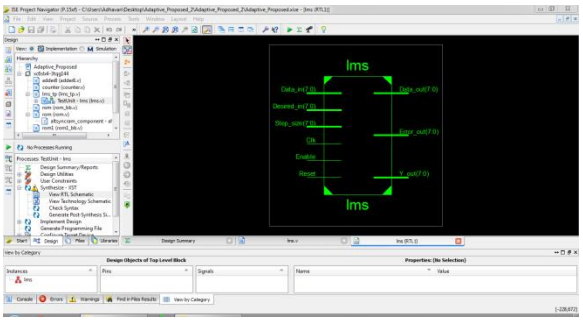


X in=10001100, din=10010010,adapt enable=1



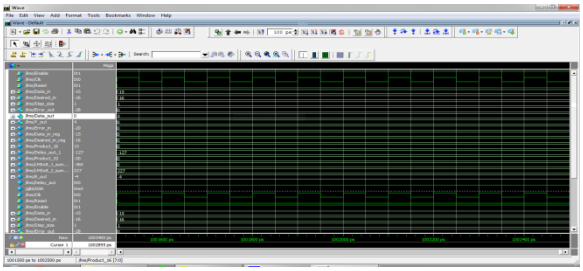
PROPOSED DESIGN RESULTS:

Proposed circuit:

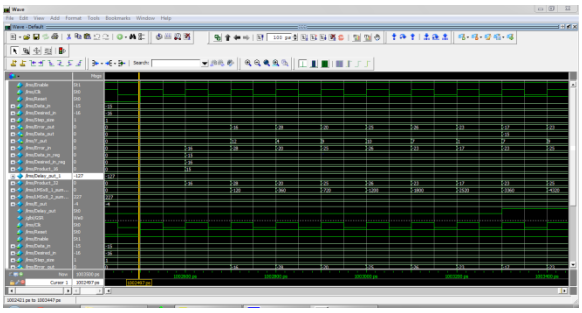


Proposed result

X in=10001100, din=10010010,adapt enable=0



X in=10001100, din=10010010,adapt enable=1



CONCLUSION

We proposed an area–delay-power efficient low adaptationdelay architecture for fixed-point implementation of LMS adaptive filter. We used a novel PPG for efficient implementation of general multiplications and inner-product computation by common subexpression sharing. Besides, we have proposed an efficient addition scheme for inner-product computation to reduce the adaptation delay significantly in order to achieve faster convergence

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performance and to reduce the critical path to support high input-sampling rates. Aside from this, we proposed a strategy for optimized balanced pipelining across the time-consuming blocks of the structure to reduce the adaptation delay and power consumption, as well. The proposed structure involved significantly less adaptation delay and provided significant saving of ADP and EDP compared to the existing structures. We proposed a fixed-point implementation of the proposed architecture, and derived the expression for steady-state error. We found that the steady-state MSE obtained from the analytical result matched well with the simulation result. We also discussed a pruning scheme that provides nearly 20% saving in the ADP and 9% saving in EDP over the proposed structure before pruning, without a noticeable degradation of steady-state error performance. The highest sampling rate that could be supported by the ASIC implementation of the proposed design ranged from about 870 to 1010 MHz for filter orders 8 to 32. When the adaptive filter is required to be operated at a lower sampling rate, one can use the proposed design with a clock slower than the maximum usable frequency and a lower operating voltage to reduce the power consumption further.

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Author(s) Details:

STUDENT

G Sirisha Received B.Tech Degree in E.C.E froms Anu Bose Institute of Technology k.s.p road paloncha in 2012.and Presently Studying M.Tech in Embedded Systems and VLSI. System Design at AKITS.

GUIDE

Venkata Rathnam M has received his B.Tech degree in Electronics and Communication Engineering from JNTU,Hyderabad in 2008 and M.Tech degree in Electronics and Communication Engineering with specialization of Systems and Signal Processing from JNTU Hyderabad in 2012. He worked as Teaching Faculty at Lemonpro Technology,Hyderabad From 2008 to2010. Presently working as Assistant Professor at Abdulkalam Institute of Technological Sciences, Kothagudem. Telangana.

HOD

G.Rajaiah ASSC. Professor. Received his B.tech Degree in Electronics and Instrumentation Engineering from Kakatiya Universit in 1997 and M.Tech in Instrumentation and Control System Design from JNTU Kakinad in 2005.Presently working as a Proffesor and HOD in Abdul Kalam Institute of Technological Sciences. He has contributed more than 20 reviewed publications in Journals.