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Design and Implementation of Low Power Dynamic Thermometer Encoder For Flash ADC

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Abstract:

In the design of a low power Flash ADC, a major challenge lies in designing a high speed thermometer code to binary code encoder. In this paper, design of a low power thermometer encoder deploying a new logic design style to convert the thermometer code to binary code with fewer transistors through the use of pseudo-dynamic CMOS logic circuits is presented for gray code , gray code to binary code encoder and for thermometer encoder the dynamic CMOS logic style is used . With this encoder a much higher conversion rate is achieved when compared to traditional encoders. The proposed dynamic thermometer encoder which operates sampling frequency can go up to 10GHz with an average power dissipation consumes 23.667µW (for 4-bit) and 55.673µW (for 5-bit) from 1.2V voltage source. To demonstrate performance, the encoder is implemented in a 5 bit Flash ADC designed in CMOS 120nm technology by using MICROWIND tool. The results clearly show that it outperforms commonly used encoders in terms of low power, speed and cost.

Keywords:

Analog to digital converter, Flash ADC, Gray code, Gray code to Binary code and Thermometer encoder, Pseudo Dynamic CMOS logic, Dynamic CMOS logic style, Microwind tool, Post-layout.

I. INTRODUCTION:

The flash ADC is known for its fastest speed compared to other ADC architectures. Therefore, it is used for high-speed and very large bandwidth applications such as radar processing, digital oscilloscopes, high-density disk drives, and so on. The flash ADC is also known as the parallel ADC because of its parallel architecture. Figure 1 illustrates a typical flash ADC block diagram. As shown in Fig. 1, this architecture needs 2n – 1 comparators for a n-bit ADC; for example, a set of 31 comparators is used for 5-bit Flash ADC. Each comparator has a reference voltage that is provided by an external reference source. These reference voltages are equally spaced by V LSB from the largest reference voltage to the smallest reference voltage V1. An analog input is

connected to all Comparators so that each comparator output is produced in one cycle. The digital out-put of the set of comparators is called the thermometer code and is being converted to gray code initially (for minimizing the bubble errors) and further changed into a binary code through the encoder [1]. However, the flash ADC needs a large number of comparators as the resolution increases. For instance, a 6-bit flash ADC needs 63 comparators, but 1023 comparators are needed for a 10-bit flash ADC.

This exponentially increasing number of comparators requires a large die size and a large amount of power consumption [3].The encoder is designed using Dynamic CMOS logic style for achieving highest sampling frequency of 10GS/s and low power dissipation. The design of the encoder with detailed description is presented in section II and III. The implementation of the encoder using pseudo NMOS and Dynamic CMOS logic styles is presented in this design of encoders.

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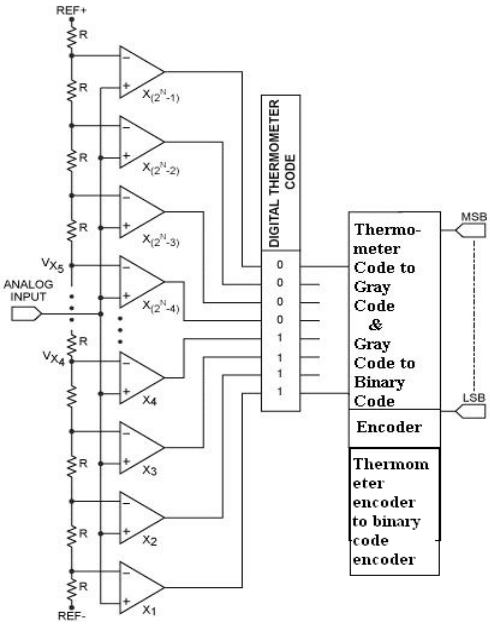

Fig. 1 Flash ADC Block Diagram

II. DESIGN OF GRAY CODE, GRAY CODE TO BINARY CODE ENCODER

Conversion of the thermometer code output to binary code is one of the bottlenecks in high speed flash ADC design [2]. For very fast input signals, small timing difference can cause bubbles in the output code. Depending on the number of successive zeroes, the bubbles are characterized as of first, second and higher orders. To reduce the effect of bubbles in encoders [5, 6]. The truth table corresponding to 5 bit gray code is presented in Table1. The relationship between thermometer code, gray code and binary code is given below

$$G4=I16$$
$$G3=I8.\overline{I24}$$
$$G2=I4.\overline{I12}+I20.\overline{I28}$$
$$G1=I2.\overline{I6}+I10.\overline{I14}+I18.\overline{I22}+I26.\overline{I30}$$
$$G0=I1.\overline{I3}+I5.\overline{I7}+I9.\overline{I11}+I13.\overline{I15}+I17.\overline{I19}+I21.\overline{I23}+I25.\overline{I27}+I29.\overline{I31}$$

$B4 = G4$
$B3 = G3 \text{ XOR } B4$
$B2 = G2 \text{ XOR } B3$
$B1 = G1 \text{ XOR } B2$
$B0 = G0 \text{ XOR } B1$

The equations for this encoder are derived from the truth table provided in Table 1.

G4	G3	G2	G1	G0	Thermometer Code
0	0	0	0	0	00000000000000000000000000000000
0	0	0	0	1	00000000000000000000000000000001
0	0	0	1	1	00000000000000000000000000000011
0	0	0	1	0	00000000000000000000000000000111
0	0	1	1	0	00000000000000000000000000001111
0	0	1	1	1	00000000000000000000000000011111
0	0	1	0	1	00000000000000000000000000111111
0	0	1	0	0	00000000000000000000000001111111
0	1	1	0	0	00000000000000000000000011111111
0	1	1	0	1	00000000000000000000000111111111
0	1	1	1	1	00000000000000000000001111111111
0	1	1	1	0	00000000000000000000011111111111
0	1	0	1	0	00000000000000000000111111111111
0	1	0	1	1	00000000000000000001111111111111
0	1	0	0	1	00000000000000000011111111111111
0	1	0	0	0	00000000000000000111111111111111
1	1	0	0	0	00000000000000001111111111111111
1	1	0	0	1	00000000000000011111111111111111
1	1	0	1	1	00000000000000111111111111111111
1	1	0	1	0	00000000000001111111111111111111
1	1	1	1	0	00000000000011111111111111111111
1	1	1	1	1	00000000001111111111111111111111
1	1	1	0	1	00000000011111111111111111111111
1	1	1	0	0	00000000111111111111111111111111
1	0	1	0	0	00000001111111111111111111111111
1	0	1	0	1	00000011111111111111111111111111
1	0	1	1	1	00000111111111111111111111111111
1	0	1	1	0	00001111111111111111111111111111
1	0	0	1	0	00011111111111111111111111111111
1	0	0	1	1	00111111111111111111111111111111
1	0	0	0	1	01111111111111111111111111111111
1	0	0	0	0	11111111111111111111111111111111

Table1. Gray Code Encoder Truth Table

There are different logic styles to implement the encoder de-sign. Generally the implementation will be done using static CMOS logic style. The advantage of static CMOS logic style is that it is having the lowest power consumption with a lower speed. So for achieving a low power with high speed, other logic styles are preferred. Here the design is implemented using logic style called pseudo NMOS logic [8].The pseudo NMOS logic circuit consists of a PMOS transistor with gate connected to ground, a bunch of NMOS transistors for the implementation of the logic style in the pull down network and an inverter. For the implementation of a specific logic circuit with N inputs, pseudo NMOS logic re-quires N+ 1 transistor instead of 2N transistors in comparison with static CMOS logic. Pseudo NMOS logic is an attempt to reduce the number of transistors with extra power dissipation

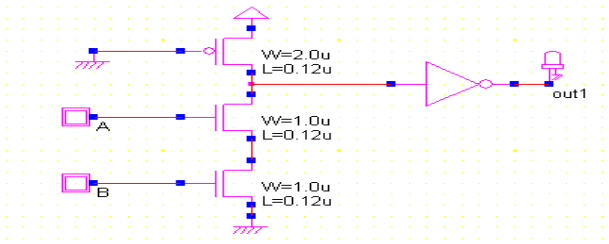

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Fig. 2 Schematic of two input AND Gate Using Pseudo NMOS Logic

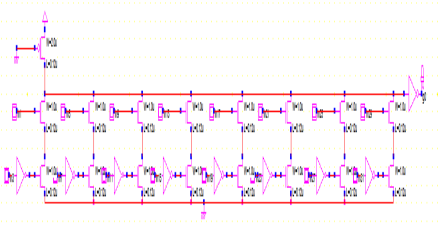
The basic structure of two inputs and gate using pseudo NMOS logic style is shown in Fig. 2. The PMOS transistor in the pull up network is connected to ground that will make the pull up network to be pulled on all the time. The output will be evaluated conditionally depending upon the value of the inputs in the pull down network. The inverter on the output transforms the inverted gate to non inverted gate. Since the voltage swing on the output and the overall functionality of the gate depend on the ratio of the NMOS and PMOS sizes, the transistor sizing is crucial in the implementation design.

The pseudo-dynamic CMOS circuit consists of a PMOS transistor, a bunch of NMOS transistors and an inverter. The PMOS transistor is used to pre-charge the output node and the NMOS logic is used to selectively discharge the output node. Unlike dynamic CMOS logic, there is no need for an NMOS evaluation transistor in series with NMOS logic block because the inputs to this circuit are the outputs of clocked comparators of Flash ADC, which latch the output till next rising edge of clock.

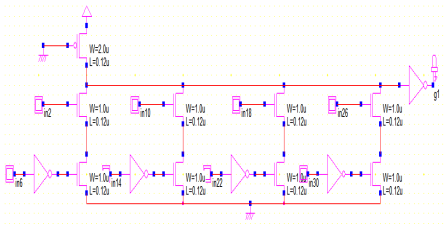
The disadvantage with pseudo NMOS logic is that it has static power consumption. (The power dissipation occurs when a direct current flows between VDD and ground. That is when both pull up and pull down networks are switched on simultaneously). The nominal high output voltage of (VOH) of pseudo NMOS logic is VDD (Assuming that the pull down network is switched off) and the nominal low output voltage (VOL) is not zero. This will results in reduced noise margins. For the implementation of the positive logics (e.g. AND, OR gate) a static CMOS inverter is added at the output side.

This will improve the noise margin of the circuit. In spite of static power dissipation, the pseudo NMOS logic consumes less amount of power because of the reduced number of transistors and the absence of other components (resistors) used for the implementation in comparison with current mode logic.The schematic of the gray code encoder for each bit is designed using the proposed logic is shown in Fig. 3. With the help of XOR gate, the gray code will be converted to bi-nary code.

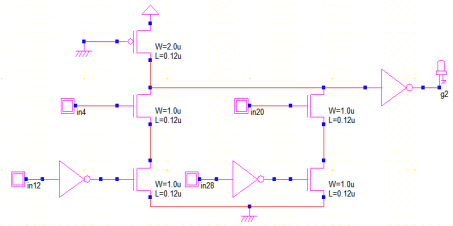
The schematic of the two input XOR gate is shown in Fig. 4. The XOR gate is implemented with a pseudo dynamic CMOS logic [7] to maintain the synchronization with the clock. Pseudo dynamic CMOS logic circuit consists of a PMOS transistor with gate connected to clock, a bunch of NMOS transistors for the implementation of the logic style in the pull down network and an inverter. The D flip flop is shown in fig. 5 and the conversion gray code to binary code we are using two input XOR gate and D flip flop. In the fig. 6 the gray code to binary code encoder is shown and the implementation this circuit takes more number of transistors with high power consumption at 10GHz.



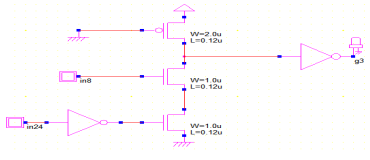
(a) Gray Code Bito Generation Circuit



(b) Gray Code Bit1 Generation Circuit



(c) Gray Code Bit2 Generation Circuit



(d) Gray Code Bit3 Generation Circuit

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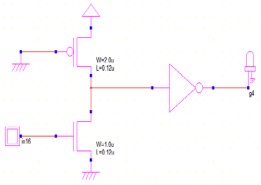

(e)Gray Code Bit4 Generation Circuit

Fig. 3 Schematic of Gray Code Encoder using Pseudo NMOS Logic

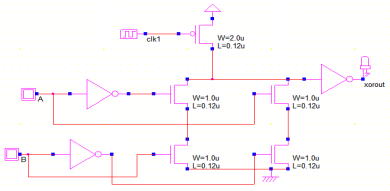

Fig. 4 Schematic of 2 Input XOR Gate using pseudo dynamic logic

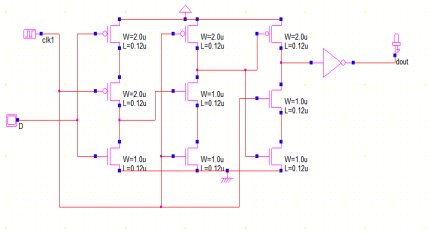

Fig. 5 Schematic of D Flip-Flop

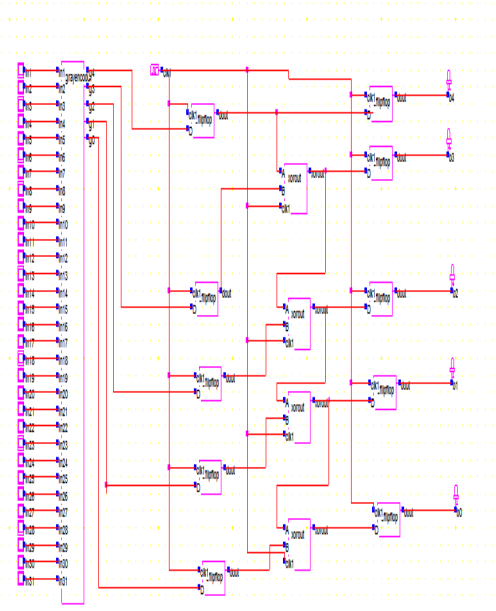

Fig. 6 Gray code to binary code encoder

III. THERMOMETER ENCODER FOR FLASH ADC:

In ADC, a series of resistors and comparators produce an output, which is a group of 1s followed by a group 0s for a particular analog voltage given as input. The outputs of the comparators are converted to binary code, using thermometer encoders. Digital thermometer encoders are of two types XOR thermometer encoder[3] and Wallace tree encoder [8]. In the XOR thermometer encoder [3], the thermometer code is first converted to Gray code, which is then converted to binary digital code. Gray code is an intermediate code, while converting thermometer code to binary digital code, which minimizes the effect of the metastability and bubble errors. XOR gates replace the AND/NAND gates due to the special format of the thermometer code itself, which improves the reliability of the encoder.The Wallace tree thermometer encoder [8] uses several full adders connected in parallel. Due to the tree structure, the numbers of transistors are reduced compared to the XOR encoder. Wallace tree method can correct higher order bubbles. The Wallace tree method is used in implementation of high speed multipliers in computer arithmetic units is the most efficient. It is used in the thermometer encoder in Flash ADCs where the number of"1's" is counted.

Bit 4 = I15

$$\text{Bit 3} = I7.\overline{I15} + I23$$

$$\text{Bit 2} = I3.\overline{I7} + I11.\overline{I15} + I19.\overline{I23} + I27$$

$$\text{Bit 1} = I1.\overline{I3} + I5.\overline{I7} + I9.\overline{I11} + I13.\overline{I15} + I17.\overline{I19} + I21.\overline{I23} + I25.\overline{I27} + I29$$

$$\text{Bit 0} = I0.\overline{I1} + I2.\overline{I3} + I4.\overline{I5} + I6.\overline{I7} + I8.\overline{I9} + I10.\overline{I11} + I12.\overline{I13} + I14.\overline{I15} + I16.\overline{I17} + I18.\overline{I19} + I20.\overline{I21} + I22.\overline{I23} + I24.\overline{I25} + I26.\overline{I27} + I28.\overline{I29} + I30$$

The truth table of a 4-bit Dynamic encoder is given below. From Table.2 Bit 3, Bit 2, Bit 1 and Bit 0 can be evaluated. The equations for 4-bit dynamic thermometer encoder are derived from its truth table.Dynamic thermometer encoders are designed using dynamic logic style for obtaining highest performance and lowest area. As the number of bits (resolution) of ADC increases, the maximum frequency of operation decreases. The dynamic CMOS circuit consists of single PMOS transistor and a bunch of NMOS transistors. In dynamic thermometer encoder, shown in Fig. 7, Fig. 8, Fig. 9, Fig. 10 and Fig. 11, the thermometer code is converted to binary output code without any intermediate stage. The number of transistors used is reduced to half when compared with CMOS logic, since PMOS network is replaced by a single PMOS transistor.

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The circuit operates in two phases - pre-charge and evaluation. During the pre-charge phase, when CLK = 0 output node is pre-charged to VDD by the pull-up PMOS transistor.The pull-down network is turned off during this time, independent of the logic implemented. During the evaluation phase.The truth table of a 4-bit Dynamic encoder is given

Bits 4 3 2 1 0	Thermometer code encoder
0 0 0 0 0	0000 0000 0000 0000 0000 0000 0000 000
0 0 0 0 1	0000 0000 0000 0000 0000 0000 0000 001
0 0 0 1 0	0000 0000 0000 0000 0000 0000 0000 011
0 0 0 1 1	0000 0000 0000 0000 0000 0000 0000 111
0 0 1 0 0	0000 0000 0000 0000 0000 0000 0001 111
0 0 1 0 1	0000 0000 0000 0000 0000 0000 0011 111
0 0 1 1 0	0000 0000 0000 0000 0000 0000 0111 111
0 0 1 1 1	0000 0000 0000 0000 0000 0000 1111 111
0 1 0 0 0	0000 0000 0000 0000 0000 0001 1111 111
0 1 0 0 1	0000 0000 0000 0000 0000 0011 1111 111
0 1 0 1 0	0000 0000 0000 0000 0000 0111 1111 111
0 1 0 1 1	0000 0000 0000 0000 0000 1111 1111 111
0 1 1 0 0	0000 0000 0000 0000 0001 1111 1111 111
0 1 1 0 1	0000 0000 0000 0000 0011 1111 1111 111
0 1 1 1 0	0000 0000 0000 0000 0111 1111 1111 111
0 1 1 1 1	0000 0000 0000 0000 1111 1111 1111 111
1 0 0 0 0	0000 0000 0000 0001 1111 1111 1111 111
1 0 0 0 1	0000 0000 0000 0011 1111 1111 1111 111
1 0 0 1 0	0000 0000 0000 0111 1111 1111 1111 111
1 0 0 1 1	0000 0000 0000 1111 1111 1111 1111 111
1 0 1 0 0	0000 0000 0001 1111 1111 1111 1111 111
1 0 1 0 1	0000 0000 0001 1111 1111 1111 1111 111
1 0 1 1 0	0000 0000 0011 1111 1111 1111 1111 111
1 0 1 1 1	0000 0000 0111 1111 1111 1111 1111 111
1 1 0 0 0	0000 0000 1111 1111 1111 1111 1111 111
1 1 0 0 1	0000 0001 1111 1111 1111 1111 1111 111
1 1 0 1 0	0000 0111 1111 1111 1111 1111 1111 111
1 1 1 0 0	0001 1111 1111 1111 1111 1111 1111 111
1 1 1 0 1	0011 1111 1111 1111 1111 1111 1111 111
1 1 1 1 0	0111 1111 1111 1111 1111 1111 1111 111
1 1 1 1 1	1111 1111 1111 1111 1111 1111 1111 111

Table2. Thermometer Code Encoder Truth Table

when CLK =1, the pre-charge PMOS transistor is turned off and the footed NMOS is turned on. The output is evaluated during this time depending upon the NMOS transistor conditions in the pull down network, which depend on the logic. The inverter in the output stage will invert the state and will give logic low or logic high value.The Total power dissipation in dynamic circuits are due to static power dissipation and dynamic power dissipation. The power dissipation occurring at the time of switching is called dynamic power dissipation, which contribute to the major part of the total power dissipation. Static power dissipation occurs when both pull up and pull down network are on. When both Pull Up and Pull down network are turned on, current flows from VDD to GND which dissipates a power in the circuit which leads to static power dissipation.

The static Power dissipation is reduced in dynamic circuits, due to the presence of footed NMOS. The final circuit is designed by using individual blocks of thermometer encoder is shown in the Fig. 13. This is final design of dynamic thermometer encoder for flash ADC.

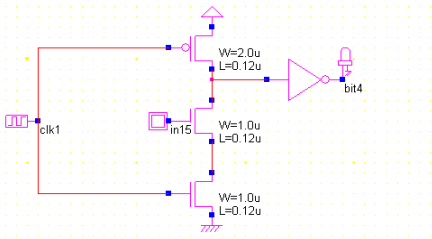

Fig.7. Bit4 of a 5-Bit Dynamic Thermometer Encoder

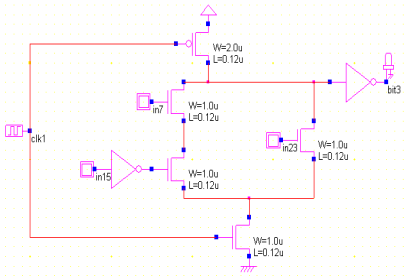

Fig.8. Bit3 of a 5-Bit Dynamic Thermometer Encoder

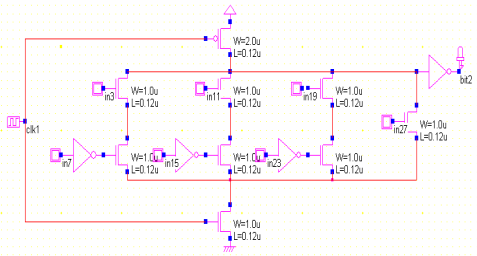

Fig.9. Bit2 of a 5-Bit Dynamic Thermometer Encoder

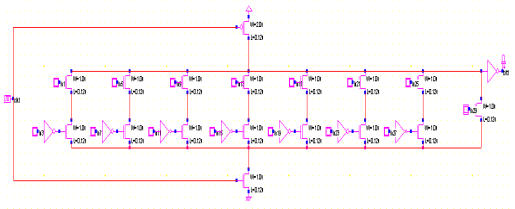

Fig.10. Bit1 of a 5-Bit Dynamic Thermometer Encoder

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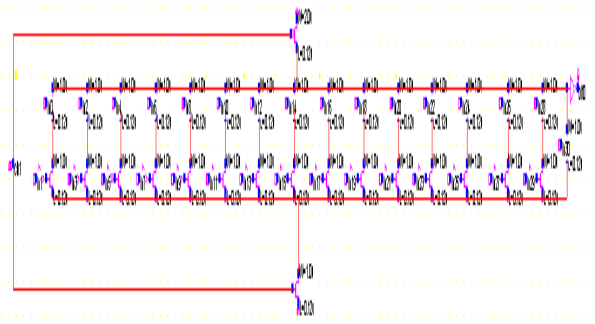

Fig.11. Bito of a 5-Bit Dynamic Thermometer Encoder

It was found that dynamic thermometer encoder has the highest performance, with respect to all parameters. It requires only one-third the number of transistors compared to Wallace tree encoder and one-fifth the number of transistors compared to XOR encoder. Hence the area is reduced drastically. Due to the presence of footed NMOS and lesser number of transistors, the static power is also reduced to 0.119nW.

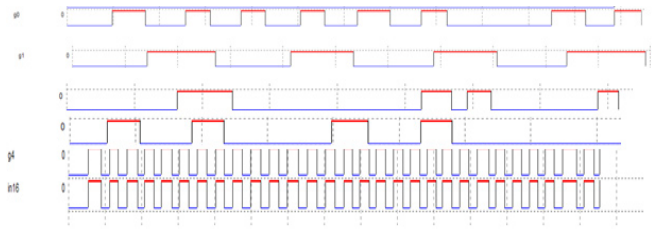

Fig.12 Wave forms of 5-bit gray code encoder for flash ADC.

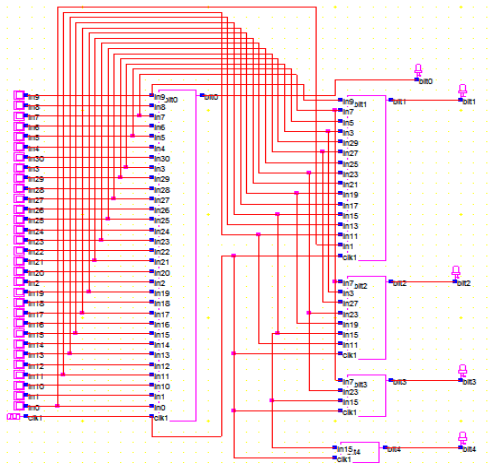

Fig.13. Schematic view of 5-bit dynamic thermometer encoder for flash ADC.

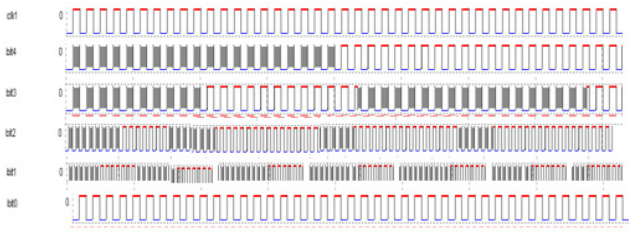

Fig.14. Output Waveform of a 5-Bit ADC

The output of the encoder is shown in the figures 12 and 14. There is also one Comparison table. The comparison is done with the reference paper In this paper author use the pseudo dynamic logic but the power dissipation is more as shown in table. So for the concern of the power consumption we choose the dynamic logic style and the result show that the power dissipation is less compared to the proposed thermometer encoder shown in table 3.

Table 3 Results Comparison table for gray code, gray to binary and dynamic Thermometer encoders for flash ADC.

Low power constraints	4-bit dynamic thermometer encoder (Mentor Graphics)	4-bit dynamic thermometer encoder (Microwind)	5-bit gray code encoder (Microwind)	5-bit gray code to binary code encoder (Microwind)	5-bit dynamic thermometer encoder (Microwind)
Resolution (bit)	4	4	5	5	5
Technology (nM)	180	120	120	120	120
Sampling frequency (GHz)	10	10	10	10	10
Supply voltage(V)	5	1.2	1.2	1.2	1.2
Power consumption	0.019 µW	22.345µW	0.164mW	2.262mW	55.673µW

IV. CONCLSION:

A high performance dynamic Flash ADC using new area-efficient dynamic thermometer encoder and low power open loop comparator is implemented and its performance is verified. It has been observed that the power dissipation and propagation delay is optimum for the new design. The number of transistors is reduced by 50%, which results in an area efficient implementation.

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Dynamic Flash ADC has been implemented, which is best suited for digital IC fabrication, since analog comparators are replaced with logic gates. Moreover technology scaling can be performed more easily for the design. Post-Layout simulations of RC extracted circuit, Design Rule Check (DRC) and Layout Versus Schematic (LVS) of a proposed dynamic thermometer encoder for Flash ADC's have also been performed.

V. REFERENCES:

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