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VHDL Implementation of High Performance Digital Up Converter Using Multi-DDS Technology For Radar Transmitters

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Abstract:
Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Radar is an object detection system which uses radio waves to determine the range, altitude, direction, or speed of objects. Digital Up-conversion is the core technology in digital radar transmitter. To achieve high sampling rate, we have to use high clock frequency hence a high hardware clock is required. In this paper we are using the Multi-DDS (10 DDS) technology which is based on parallel processing, a large bandwidth signal can be produced at conditions of a lower hardware clock. This output signal is used to generate the Radar signal with high sampling rate (50 MHz). Similarly Multi-DDS technology gives a high-efficient solution. With this by using lower hardware clock high sampling rate can be achieved. As this paper presents the results based on a system (i.e. Spatarn-3E FPGA) whose clock frequency is 50MHz.

Keywords: ***Digital Up-conversion, Multi-DDS algorithm, Parallel processing***

Introduction:

Digital radar transmitter is widely used in the field of radar signal processing due to the flexibility, small size and low development costs. The traditional radar signal transmitting process includes the generation of the base-band signal, modulated to the intermediate frequency, digital-to-analog conversion, modulated to a radio frequency and antenna transmits. The steps which involved in generation of the base-band signal, modulated to the intermediate frequency and digital-to-analog conversion are implemented by digital radar transmitter.

The demand for high performance and functionality of digital radar transmitter, especially the increasing requirements on resolution and real-time system in imaging radar, the large bandwidth base-band signals required. The multi-DDS technology for high performance digital conversion and High-efficient digital up-conversion processing which is based on multi-DDS technology.

Radar (acronym for Radio Detection and Ranging) is an object-detection system that uses radio waves to determine the range, altitude, direction, or speed of objects. It can be used to detect aircraft, ships, spacecraft, guided missiles, motor vehicles, weather formations, and terrain. The radar dish or antenna transmits pulses of radio waves or microwaves that bounce off any object in their path. The object returns a tiny part of the wave's energy to a dish or antenna that is usually located at the same site as the transmitter.

The direct digital synthesis (DDS) technology is a new type of frequency synthesizer technology which developed on the basis of the direct analog synthesizer (DAS) and direct digital waveform synthesis technology (DDWS). It draws advanced digital signal processing theory and methods into signal synthesis field. By this way, conversion speed can be guaranteed and synthesized signal accuracy also improved. DDS technology utilizes continuous phase transformation to generate signal with high frequency resolution, low

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phase noise and low spurious. Owing to these advantages, traditional digital up-conversion process typically uses the DDS technology to generate a required base-band signal.

Applications of DDS (Direct digital Synthesizer):

- Software-defined radios (SDR).
- Digital radios and modems.
- Digital down/up converters for cellular and PCS base stations.
- Waveform synthesis in digital phase locked loops.
- Generating injection frequencies for analog mixers.

Digital Up Conversion:

Digital up conversion by Multi dds is done by the adding the dds1 output to the next dds and next dds output to another dds likely to get the high sampling rate means digital up conversion occurred.

Digital up converter (DUC) translates the base band signal to a higher frequency band. This is done by first step up sampling the base band signal to the required sampling frequency and then mixing it with a high frequency carrier.

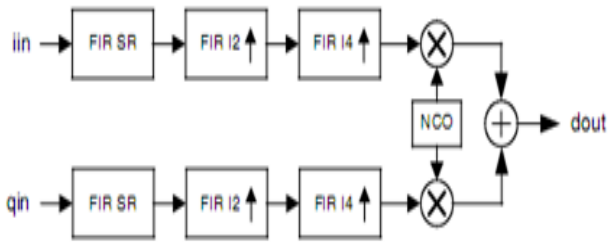

Fig 1: Functional Block Diagram of the DUC

Implementation Of Multi Dds:

Direct digital synthesizers (DDS), or numerically controlled oscillators (NCO), are important components in many digital communication systems. Quadrature synthesizers are used for constructing digital down and up converters, demodulators, and implementing various types of modulation schemes, including PSK (phase shift keying), FSK (frequency shift keying), and MSK(minimum shift keying). A common method for digitally generating a complex or real valued sinusoid employs a lookup table scheme. The lookup table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the lookup table to the desired output waveform. A simple user interface accepts system level parameters such as the desired output frequency and spurs suppression of the generated waveforms.

The LogiCORE™ IP DDS (Direct Digital Synthesizer) Compiler core sources sinusoidal waveforms for use in many applications. A DDS consists of a Phase Generator and a SIN/COS Lookup Table. These parts are available individually or combined via this core. Direct digital synthesis (DDS) is a method of producing an analog waveform—usually a sine wave—by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today's DDS devices are very compact and draw little power.

General Description:

Function generators have been around for a long while. Over time, these instruments have accumulated a long list of features. Starting with just a few knobs for setting the amplitude and frequency of a sinusoidal output, function generators now provide wider frequency ranges, calibrated output levels, a variety of waveforms, modulation modes, computer interfaces, and in some cases, arbitrary functions. The many features added to function generators have complicated their design and increased their cost. There is an opportunity for a radical re-design of the familiar function generator using direct digital synthesis (DDS).DDS provides remarkable frequency resolution and allows direct implementation of frequency, phase and amplitude modulation. These features which were

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'tacked-on' to function generators now are handled in a clean, fundamental way by DDS.

The ability to accurately produce and control waveforms of various frequencies and profiles has become a key requirement common to a number of industries. Whether providing agile sources of low-phase-noise variable-frequencies with good spurious performance for communications, or simply generating a frequency stimulus in industrial or biomedical test equipment applications, convenience, compactness, and low cost are important design considerations. Many possibilities for frequency generation are open to a designer, ranging from phase-locked-loop (PLL)-based techniques for very high-frequency synthesis, to dynamic programming of digital-to-analog converter (DAC) outputs to generate arbitrary waveforms at lower frequencies. But the DDS technique is rapidly gaining acceptance for solving frequency- (or waveform) generation requirements in both communications and industrial applications because single-chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy.

DDS devices like the AD9833 are programmed through a high speed serial peripheral- interface (SPI), and need only an external clock to generate simple sine waves. DDS devices are now available that can generate frequencies from less than 1 Hz up to 400 MHz (based on a 1-GHz clock). The benefits of their low power, low cost, and single small package, combined with their inherent excellent performance and the ability to digitally program (and re-program) the output waveform, make DDS devices an extremely attractive solution—preferable to less-flexible solutions comprising aggregations of discrete elements.

Applications currently using DDS-based waveform generation fall into two principal categories: Designers of communications systems requiring agile (i.e., immediately responding) frequency sources with excellent phase noise and low spurious performance often choose DDS for its combination of spectral performance and frequency-tuning resolution. Such applications include using a DDS for modulation, as a reference for a PLL to enhance overall frequency tunability, as a local oscillator (LO), or even for direct RF transmission.

Alternatively, many industrial and biomedical applications use a DDS as a programmable waveform generator. Because a DDS is digitally programmable, the phase and frequency of a waveform can be easily adjusted without the need to change the external components that would normally need to be changed when using traditional analog-programmed waveform generators. DDS permits simple adjustments of frequency in real time to locate resonant frequencies or compensate for temperature drift. Such applications include using a DDS in adjustable frequency sources to measure impedance (for example in an impedance-based sensor), to generate pulse-wave modulated signals for micro-actuation, or to examine attenuation in LANs or telephone cables.

Today's cost- competitive, high-performance, functionally integrated DDS ICs are becoming common in both communication systems and sensor applications. The advantages that make them attractive to design engineers include:

• Digitally controlled micro-hertz frequency-tuning and sub degree phase-tuning capability,
• Extremely fast hopping speed in tuning output frequency (or phase); phase - continuous frequency hops with no overshoot/undershoot or analog-related loop settling-time anomalies,
• The digital architecture of DDS eliminates the need for the manual tuning and tweaking related to component aging and temperature drift in analog synthesizer solutions, and
• The digital control interface of the DDS architecture facilitates an environment where systems can be remotely controlled and optimized with high resolution under processor control.

Core Architecture Overview:

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The core consists of two main parts, a Phase Generator and SIN/COS LUT, which can be used independently or together with an optional dither generator to create a DDS capability. A time-division multi-channel capability is supported, with independently configurable phase increment and offset parameters. Below Figure3.1 provides a block diagram of the DDS Compiler core.

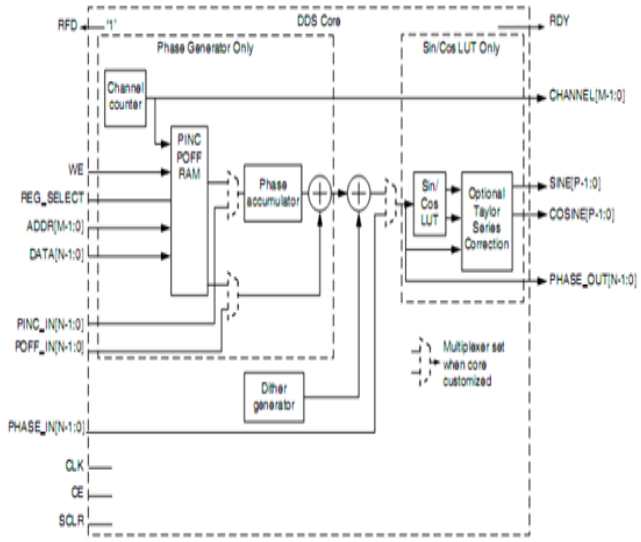

Figure.3.1. DDS Compiler Core.

Phase Generator

The Phase Generator consists of an accumulator followed by an optional adder to provide addition of phase offset. When the core is customized the phase increment and offset can be independently configured to be either fixed, programmable or supplied by the PINC_IN and POFF_IN input ports respectively.

When set to programmable, registers are implemented with a bus interface, consisting of ADDR, REG_SELECT, WE, and DATA signals. The address input, ADDR, specifies the channel for which DATA is to be written when multi-channel, with REG_SELECT specifying whether DATA is phase increment or offset.

When set to fix the DDS output frequency is set when the core is customized and cannot be adjusted once the core is embedded in a design.

SIN/COS LUT

When configured as a SIN/COS LUT, the Phase Generator is not implemented, and the phase is input via the PHASE_IN port, and transformed into the sine and cosine outputs using a look-up table. Efficient memory usage is achieved using half wave and quarter wave storage schemes. The presence of both outputs and their negation are configurable when the core is customized. Precision can be increased using optional Taylor Series Correction. This exploits Xtreme DSP slices on FPGA families that support them to achieve high SFDR with high speed operation.

Phase Generator and SIN/COS LUT (DDS)

The Phase Generator is used in conjunction with the SIN/COS LUT to provide either a Phase Truncated DDS or Taylor Series Corrected DDS. An optional dither generator can be added between the two blocks to provide a Phase Dithered DDS.

Interface, Control, and Timing:

The DDS Compiler core pin out is shown in below Figure. All of the possible pins are shown, though the specific pins in any instance depend upon parameters specified when the core is generated.

Single DDS Unit Principle:

Direct digital synthesizer table to uses a lookup generate sine and cosine signals. And since most of the signals can be decomposed into a number of sine and cosine signals, theoretically, the DDS unit can achieve signals with arbitrary waveform the basic structure of single DDS unit consists of phase accumulation, adder, lut cos/sin and phase accumulator. The process that Sin signal is generated through look-up table (LUT).

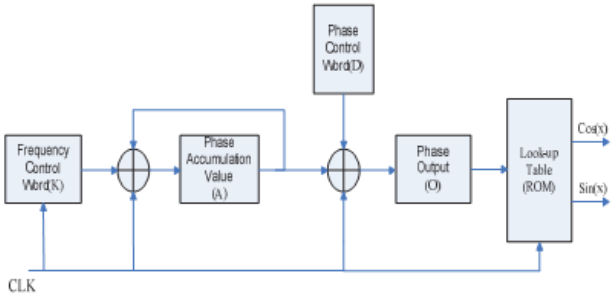

Fig 3.2: Basic structure of single DDS unit

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→Calculated the value of sin within a cycle (0~2π) and pre-stored them in the ROM. Stored quantity is determined by the accuracy of the sin signal. If an accuracy of 16bits is required, we segment the value of sin into 2^{16} =65526 pieces, and store them in the ROM. Besides that, the size of ROM is related to the bit wide of the output. When a LUT supports the accuracy for N bits and the output for M bits, the ROM needed for the LUT can be obtained.

$$LUT = \frac{2^N \times M}{8}$$

→The input terminal of LUT is output phase o whose range is determined by a LUT's accuracy N .The relationship between output phase o and output signal Sin(x) can be obtained by

$$\text{Sin}(x) = \text{Sin}(2 \times \pi \times \frac{O}{2^N})$$

→For each CLK, the output phase o is got by the addition of Phase Control Word D and Frequency Accumulation Value A. Phrase Control Word D determines the initial phase and the fixed offset of output phase while Frequency Accumulation Value A reflect the changes of each output phase.

→For each CLK, the Frequency Accumulation Value gets an accumulation and the new adder is determined by Frequency Control Word K. The signal is generated with single frequency when the value of K is fixed. Otherwise, it outputs a multi-frequency signal.

→ The frequency of output signal can be obtained by

$$f_{out} = f_{clk} \times \frac{K}{2^N}$$

Block Diagram of Multi DDS:

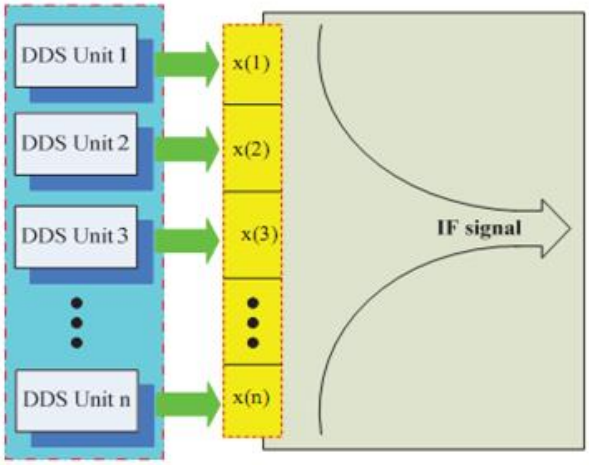

Fig 3.3: High-efficient digital up-conversion processing

Direct digital synthesizer uses a lookup table to generate sine and cosine signals. And since most of the signals can be decomposed into a number of sine and cosine signals, Seen by the sampling theorem, when system clock is CLK, the highest frequency that a DDS can generate is CLK ÷2. If the higher frequency is required with the same clock, Multi-DDS technology supports a high-efficient solution. N channel parallel DDS units work in the clock of CLK can produce a signal with the frequency of N .CLK ÷2 HZ.

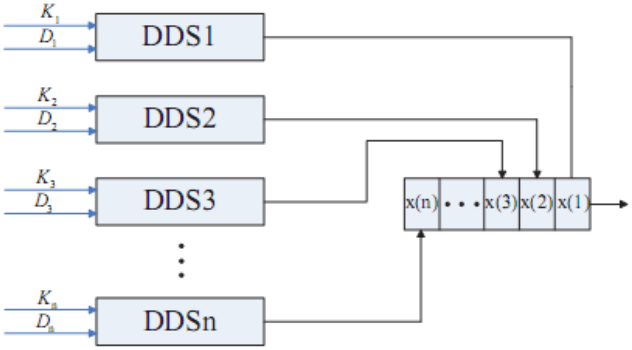

Fig 3.4: Structure of Multi-DDS

DDFS:

The basic block diagram of Universal Modulator using DDFS, all the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence

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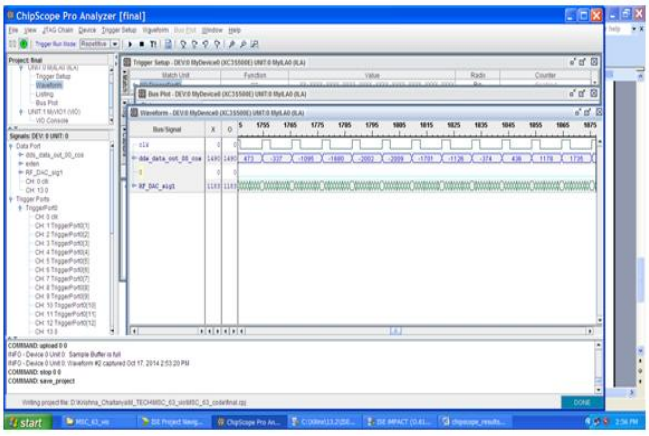
decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency. If the modulating signal is analog then an Analog Digital converter must be used to digitize the modulating signal which can be used in DDFS.

The phase accumulator produces accumulated phase value for each clock pulse. In case if the DDFS is used for phase modulation then instantaneous phase modulating signal value is added to the phase output of phase accumulator. This resulting phase value is given to the four Look Up Tables. Each Look Up Table is configured to produce a specific waveform. The logic used to generate the Look Up Tables is discussed in the further sections.

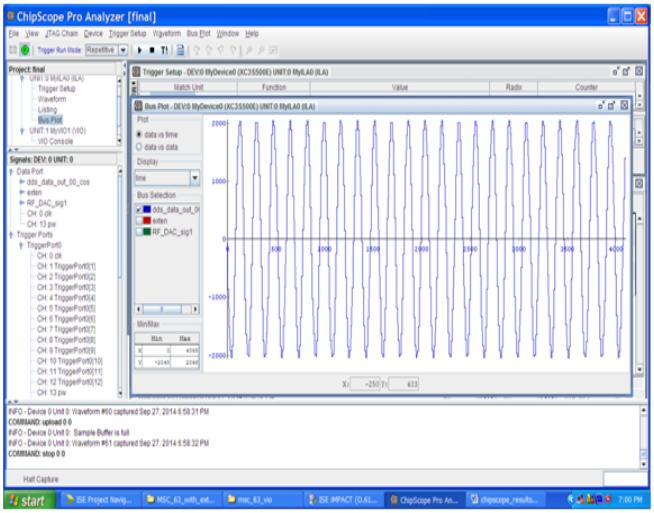
The outputs of the Look Up Tables are given to the input lines a 4 to 1 Multiplexer. This multiplexer connects one of the inputs to the output depending on the select lines. The output of Multiplexer consists the 8 amplitude bits which is the final output in case required modulation schemes are FM or PM. In case of Amplitude modulation, the output of Multiplexer is multiplied with instantaneous modulating signal. The basic blocks in DDFS can be identified as PIPO registers, adders, Look Up Tables,

Chipscope Results:

Waveform:



Busplot Outputs:



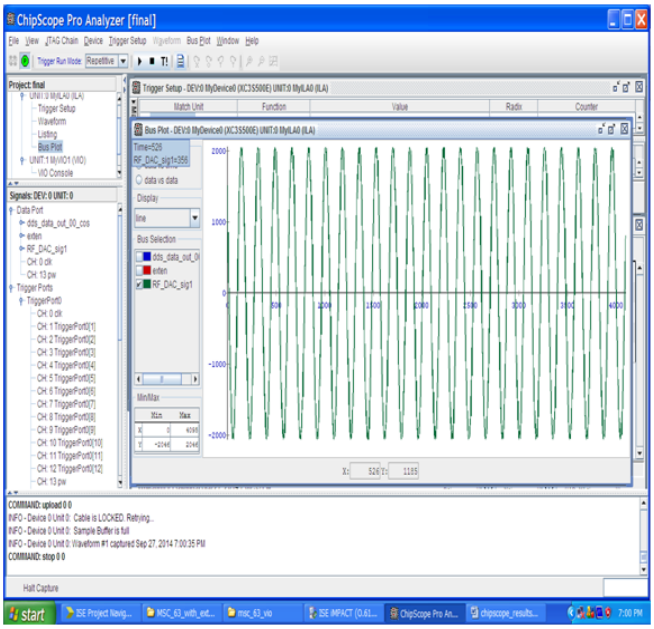


Fig: Chipscope Output Of RF_DAC_OUT

Applications

- Used in surveillance RADARs.
- Used in ATC's (Air traffic controllers)
- Military applications
- Weather RADARs
- Digital Up-conversion is the core technology in digital radar transmitter.
  such as software-defined radio.
- Also where high-speed streaming of narrow bandwidth signals is required.

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Conclusion

An efficient digital conversion process has been by researched using Multi-DDS technology which based on parallel processing, a large bandwidth signal can be produced at conditions of a lower hardware clock. Besides that this solution eliminates the need for filtering and modulation Process and directly generates IF signal. The program has been implemented in FPGA hardware platform and achieved very good results.

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