

# **A Build In Self Test Application For Motion Test Applications**

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**ABSTRACT:** Motion estimation plays a vital role in today'smedia applications. Hence testing of such a module is asignificant concern. Even though several algorithms have been proposed in the past testing of motion estimators are seldom addressed. The proposed system describes an Error Detection and Data Recovery (EDDR) architecture that detects and recovers data inthe motion estimator. The system uses the Mean Absolute Difference (MAD) method to compute the difference in the current and reference frames which overcomes some of the drawbacks in the existing techniques. The architecture comprises of an Error Detection Circuit (EDC) and a Data Recovery Circuit(DRC) to recover the original data. A Residue-Ouotient code is used to compute the change in value between the error and expected values. Result show that the errors are effectively recovered with a delay of a single cycle.

*Keywords* - Area overhead, data recovery, errordetection, motion estimation, reliability, residueand quotient(*RQ*) code.

# **INTRODUCTION:**

Motion estimation is the process of determining motion vectors that describe the transformation from one 2D image to another; usually from adjacent frames in a video sequence. It is an ill-posed problem as the motion is in three dimensions but the images are a projection of the 3D scene onto a 2D plane. The motion vectors may relate to the whole image (global motion estimation) or specific parts, such as rectangular blocks, arbitrary shaped patches or even per pixel. The motion vectors may be represented by a translational model or many other models that can approximate the motion of a real video camera, such as K.Vasavi

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rotation and translation in all three dimensions and zoom. Closely related to motion estimation is optical flow, where the vectors correspond to the perceived movement of pixels. In motion estimation an exact 1:1 correspondence of pixel positions is not a requirement. Applying the motion vectors to an image to synthesize the transformation to the next image is called motion compensation. The combination of motion estimation and motion compensation is a key part of video compression as used by MPEG 1, 2 and 4 as well as many other video codec.

# **Existing System:**

Coding approaches such as parity code, Berger code, and residue code have been considered for design applications to detect circuit errors. Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. Error detection logic for operations is typically derived by a separate residue code, making the detection logic is simple and easily implemented. However, only a bit error can be detected based on the residue code. Additionally, an error cannot be recovered effectively by using the residue codes. There-fore, this work presents a quotient code, which is derived from the residue code, to assist the residue code in detecting multiple errors and recovering.

#### **Proposed System:**

The conceptual view of the proposed EDDR scheme comprises of two major circuit designs, error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific Circuit Under Test (CUT) which is the systolic array. The test code generator (TCG) in Fig.1 utilizes the concepts of RQ code to generate the

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corresponding test codes for error detection and data recovery.

# **Test Code Generator**

Figure 2, illustrates the structure of the TCG module in the proposed EDDR architecture. Notably, TCG design is based on the ability of the RQCG circuit to generate the corresponding test codes in order to detect errors and recover data. The specific PEi estimates the absolute difference between the Cur\_pixel of the search area and the Ref\_pixel of the current macroblock. Thus the Residue and Quotient value for an array size of N X N is given by equations (3) and (5).

$$R_{T} = \left| \frac{1}{n^{2}} \sum_{i=1}^{n} \sum_{j=1}^{n} |X_{ij} - Y_{ij}| \right| m$$
(2)

 $R_{T} = [|r_{11}|m + |r_{12}|m + |r_{13}|m + \dots + |r_{nn}|m] (3)$ 

$$Q_{T} = \left[\frac{\left(\frac{1}{n^{2}}\right)\sum_{i=1}^{n}\sum_{j=1}^{n}|x_{ij}-y_{ij}|}{m}\right]$$
(4)
$$Q_{T} = \left[q_{11} + q_{12} + \dots + q_{nn}\right] + \left[\frac{r_{11}+r_{12}+\dots+r_{nn}}{m}\right]$$
(5)

(5)

Notably the error signal e is expressed as,

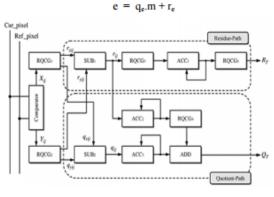


Figure 2. Test Code Generator

# **Numerical Example**

A numerical example of the 16 pixels for a 4x4 macroblock in a specific PEi of a ME is described as follows. Fig. 5 presents an example of pixel values of the Cur\_pixel and Ref\_pixel. Based on (1), the MAD value of the 4x4 macroblock is,

MAD =  $\frac{1}{n^2} \sum_{i=0}^{3} \sum_{j=0}^{3} |X_{ij} - Y_{ij}|$  $= \frac{1}{n^2} [|X_{00} - Y_{00}| + |X_{01} - Y_{01}| + \dots + |X_{33} - Y_{33}|]$  $= \frac{1}{16} \{ (128-1) + (128-1) + \dots + (128-5) \}$ = 132.750 1 2 0 128 128 64 255 0 2 3 1 1 2 128 64 255 64 1 з 4 2 64 255 64 128 2 2 з 4 5 255 4 5 64 128 128 3 5 3 3 Cur\_pixel Ref\_pixel



# **RESULTS AND DISCUSSION**

The proposed architecture was executed on Windows XP operating system at an operating frequency of 2.80GHz using ModelSim for functional verification and synthesized using Xilinx ISE simulator. Table 1 gives the synthesis report provides the device utilization which is analyzed in terms of percentage. The timing summary of the code execution is also obtained. The proposed architecture was simulated on XC3S100E device of Spartan3E family provided the following synthesis results.

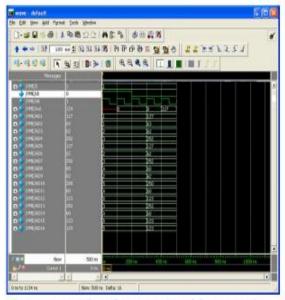
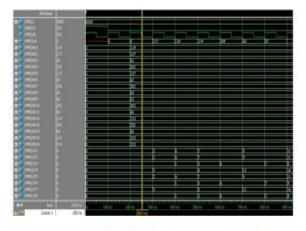


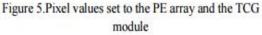
Figure 4. Screenshot of the operation of the proposed system

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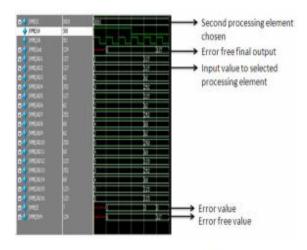


Figure 6. Comparison of error output with the recovered output

# **CONCLUSION:**

Our work presents an EDDR architecture for detecting the errors and recovering the data of PEs in a ME. Based on the RQ code, a RQCG-based TCG design is developed to generate the corresponding codes to detect errors and recover data. Experimental results obtained from ModelSim indicate that that the proposed EDDR architecture can effectively detect errors and recover data in PEs of a ME with reasonable area overhead and only a slight time penalty. Synthesis results show that the timing constraints and device utilization are minimum compared to error detection techniques available.

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