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Low Power Low Area Efficient Carry Select Adder

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I. INTRODUCTION:

Adders have a special significance in VLSI designs and it is used in computer and many other processors. It is used to calculate addresses, table indices and similar applications. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing. Now a days design of low power and area efficient high speed data path logic systems are most substantial area in the research of VLSI design. Number of fast adders can be used for addition.In digital adders the sum of each bit position is added and the generated carry is propagated into the next position. The propagated carry reduces the speed of addition.The carry select adder can be used to alleviate this problem. Carry select adder is one of thefastest adders having less area and powerconsumption. Itgenerates partial sum and carry by considering carry input Cin=0 and Cin=1, the final sum and carry are selected by the multiplexers. The main idea used in this project is to useBinary to Excess- 1 convertor(BEC) instead of RCA to reduce the area.This paper is organized in the following sections. II. Literature surveyIIIBEC.IV Explanation about regular SQRT CSLA and modified SQRT CSLAV.ResultVI Conclusion .

II. LITERATURE SURVEY:

There are different types of fast adders used in processors such as ripple carry adder(RCA),carry look aheadadder (CLA)and carry select adder. Ripple carry adder provides compact design but their computation time is high. Carry look ahead adder gives fast result but it leads to an increase in area. Carry select adder provides a compromise between RCA and carry look ahead adder. Ripple carry adder produces worst case delay, because it consists of N single bit full adders. Each adderproduces the sum and carry. The carry of the previous full adder is givenas the input to the next adder. The carry is transferred through every stage and produces a delaycalled worst case delay. In ripple carry adder as value of N increases, delay also increases. So ripple carry adder has the lowest speed among the fast adders. The CSLA is used to anticipate all possible values of input carry i.e. 0 and 1 and evaluates the result in advance. The result is selected by the multiplexer. The CSLA uses dual RCA's to generate partial sum and carry by considering Cin=0 and Cin=1 then the final sum and carry is selected by using multiplier. In regular CSLA area consumed is more due to the use of dual RCA's. The basic idea of this work is to use Binary to excess-1 convertor(BEC) instead of RCA with Cin=1to reduce the area and power. The advantage of BEC is that it uses less number of logic gates than N bit full adders. To reduce thedelay N bit ripple carry adders are replaced with N+1 bit BEC .So modified SQRT CSLA is area consuming than regular CSLA.

III .CSLA with BEC:

Modified CSLA uses BEC.BEC is a circuit used to add 1 to input numbers. The circuit of 4 bit BEC is shown in figure 1 and the truth table is shown in table 1.

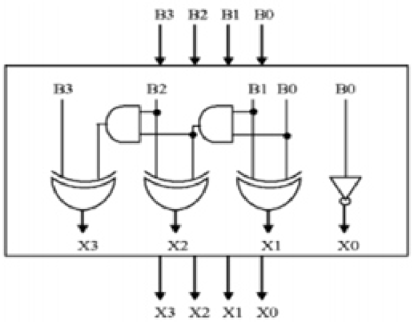

Fig1. 4 bit Binary to Excess-1 Convertor

BEC consist of 4 inputs and the result is obtained by adding 1 with each of it.The expressions of 4 bit BEC are listed below.

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$X0=\sim B0$
$X1=B0 \wedge B1$
$X2=B2 \wedge (B0\&B1)$
$X3=B3 \wedge (B0\&B1\&B2)$

TABLE1 TRUTH TABLE OF 4 BITS BINARY TO EXCESS -1 CONVERTOR

Binary logic B0,B1,B2,B3	Excess-1logic X0,X1,X2,X3
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

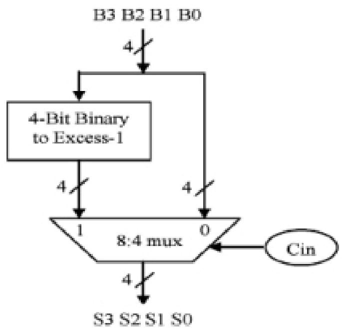

Fig2. 4 Bit Binary to excess-1 logic with 8:4 multiplexer Addition is achieved using BEC together with multiplexer as shown in figure 2 .If the select line of MUX is 0 then input is (B3,B2,B1 and B0) otherwise input is BECs output.

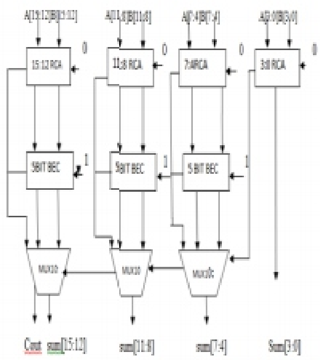

Fig3.Block diagram of modified carry select adder

Thus modified CSLA is designed such that it occupies less area and low power than regular CSLA. Also RCAis replaced with BEC.

IV.DELAY AND AREA OF REGULAR 16 BIT ADDER:

The delay can be calculated by adding up the number of gates in the longest path of logic block that contributes maximum delay.The area evolution is done by counting the total number of AOI gates required for each logic block. The structure of 16 bit regular SQRT CSLA is shown in fig 4, Proposed design has five groups of different size RCA .Each group contain dual RCA and MUX.The delay and area of each group is calculated and at last finds the total area and delay. The main disadvantage of regular CSLA is high area usage that can be overcome by using modified CSLA.

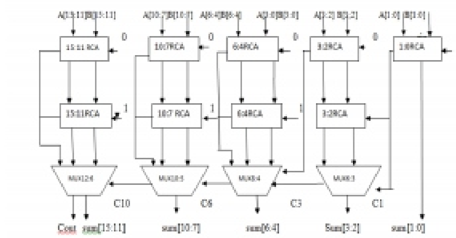

Fig4. Regular 16 bit SQRT CSLA

Modified SQRT CSLA is similar to that of regular SQRT CSLA the only difference we replace RCA withCin=1 with BEC.The replaced BEC perform the same operation as that of the replaced RCA with C in=1.Figure 5 shows the modified SQTR CSLA.This structure consumes less area, delay and power than regular SQRT CSLA.

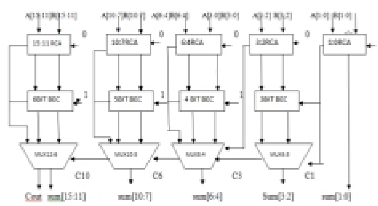

Fig5. Modified 16 bit SQRT CSLA

V.RESULT:

This work is developed using Xilinx tool. Table II shows the comparison between different adders like regular SQRT CSLA, modified SQRT CSLA etc.The parameters compared are area and power. Modified SQRT CSLA has lesser number of logic gates and hence less area.

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TABLE.IICOMPARISON OF ADDERS FOR AREA, DELAY.POWER

Adder	Area (No. of gate count)	Delay(ns)	Power(Mw)
Conventional (Dual RCA)	480	19.81	94.63
Modified(with BEC)	381	21.59	81.38
Regular SQRT (with dual RCA)	348	16.15	315
Modified SQRT(with BEC)	291	18.77	268

VI.CONCLUSION:

In VLSI design process power, delay and area are the important factors that determine the performance of any circuit. This work is to reduce the area, power and delay of CSLA.

The regular CSLA has the disadvantage of more power consumption and large area. So modified CSLA overcomes this .It reduces the area and power which make it simple and efficient for VLSI hardware implementation

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