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Design of Single Phase Continuous Clock Signal Set D-FF for Ultra Low Power VLSI Applications

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Abstract: - ***Nowadays low power consumption plays a vital role in many VLSI applications. This research aims at design of single phase continuous clock signal SET D-FF for ultralow power VLSI applications. Design is tested by using substrate biasing technique. The design is realized in 180nm technology and results are compared with different biasing techniques which are driven through SET D-FF is applicable for portable devices. The comparative results prove that the proposed design of SET D-FF is suitable for portable applications, as it is more efficient in power consumption.***

Keywords: ***LVSB, STGB, NBB, SET D-FF., Portable applications.***

I INTRODUCTION

Now a day's portable device such as mobile phones and laptops should reach high end customer satisfaction. High level performance of a digital device depends on power, delay and area there by power delay product. We can produce an optimal solution if we operate a MOSFET circuit at low frequencies and under sub-threshold region. Sub-threshold region can be achieved in MOSFET when gate to source voltage V_{gs} is less than the threshold voltage V_{th}.

We can operate CMOS circuit under sub-threshold current by maintaining supply voltage (V_{dd}) to be lower than the V_{th}. Sub-threshold current circuits are sensitive to temperature and process variations.

Another most important component while designing circuits is Flip-Flop. Flip-Flop needs more power to operate the circuit due to clock setup in it.

Previously so many papers dealt with reduction of power consumption under sub-threshold region. Existing one works under 45nm and 65nm technologies and proved that they are technology independent. They succeeded somewhat by implementing sub-threshold current but limited when dealing with number of transistors to realize this circuits.as more number of circuits used resulting in large area, more power and delay.so they are not preferable for low budget systems.

Flip-Flops are categorized into two types:-

1) SET: Single Edge Triggered
2) DET: Double Edge Triggered

Flip-flop is a synchronous bistable device because output changes its state only at a specified point on a triggering input called clock, that is either at positive edge or at negative edge i.e., output is sensitive to input only at this transition of clock.

SET the name itself says that in SET the data flows through one edge of clock either on rising or on falling. In DET the data flows through both edges of clock rising and falling edge. SET has simplest design when DET has complex design but can be operated at low frequencies and has lower performance compare to SET. More complex circuit means more signal fluctuations in the propagation path which results performance

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degradation. So DET performance can be said that it is not worthwhile. So the efficient idea is to work on SET.

Flip-Flops are of two types based on the clock condition.

Dynamic: The Flip-flop is said to be dynamic when it provides faulty logic on removal of the clock. Faulty logic is generated when it suffers from charge leakage of output node capacitances.

Static: The Flip-Flop is said to be static when the Flip-Flop maintains their output state even on the removal of clock. This leakage current is controllable by threshold voltage of transistor.

Biasing of the transistor affects the threshold voltage. So indirectly we have to realize the circuit using appropriate biasing technique to control the leakage current. Here substrate biasing technique is used to control the leakage current as well as to reduce power consumption. SET D-FF design is realized in 180nm technology by using substrate biasing technique. Biasing techniques are divided into three types STGB, LVSB and NBB.

The substrate biasing technique is main role in the LVSB, STGB and NBB designs are working on the biasing technique. Excitation results said that NBB is good one compare to LVSB and STGB. Then NBB is tested with sine and pulse. Results show that sine is far better than pulse by observing power delay product.

The rest of the paper is aligned to show that in CHAPTER II a brief discussion of SET D-FF designs.in CHAPTER III simulation results, in CHAPTER IV conclusions.

II DESIGN OF SET D FLIP-FLOP

SET single edge triggering:

A conventional SET D-flip flop is designed to be flow data through one edge of the clock i.e. either raising edge or falling. When flip flop is triggered to raising of the edge it delivers the stable output i.e. $t_{set\text{-}up}$. As well as when flip flop is triggered to falling edge the previous will be appeared as output.i.e $t_{hold.}$

$t_{set\text{-}up:}$ The setup time is the minimum time required to maintain a constant voltage levels (data) at the excitation inputs of the flip flop device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{setup}.

t_{hold} : The hold time is the minimum time for which the voltage levels (data) at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as $t_{hold.}$

LVSB: Low voltage swapped body bias

In this configuration all PMOS transistors are used to connect to ground and all NMOS transistors are used to give supply voltage i.e. v_{DD}.Lvsb is designed with biasing circuit which leads to stable output. In LVSB circuit is provided by a clock D,to drive the circuit which results in excitations of Q,Q,clock.The figure.1 shows schematic of low voltage swapped body bias (LVSB). The circuit is regulated as bulk voltage is less than the source voltage.

STGB: Sub –Threshold Grounded body bias.

In this circuit both PMOS and NMOS are neutralized. STGB uses a biasing circuit to provide stable circuit as in the case of LVSB. Usage of substrate connections reduces the complexity of STGB design. All NMOS transistors works under no body bias while all PMOS works under forward bias condition.The figure 2 shows schematic of sub threshold grounded body bias. connections reduces the complexity of STGB design. All NMOS transistors works under no body bias while all PMOS works under forward bias condition.The figure 2 shows schematic of sub threshold grounded body bias.

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NBB: No Body Bias.

V_{SB} of the MOSFET transistor always at null voltage because of its substrate to source connection hence it is named as No Body Bias (NBB).In NBB design Threshold voltage is always regulated to be zero in MOSFET transistor.The figure 3 shows schematic of No Body Bias(NBB).

III PROPOSED WORK

65nm and 45nm technology is used to realize this project. This design has been proved that it has technology independence. This design is excited using tanner tools v12.6.NBB is the best one compare to LVSB and STGB designs by power dissipation wise.

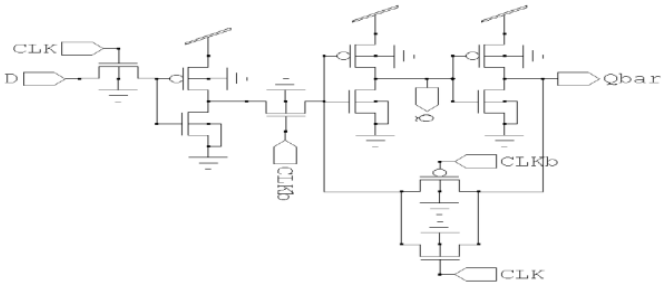

Fig 2. 10-Transistor SET D-FF of STGB

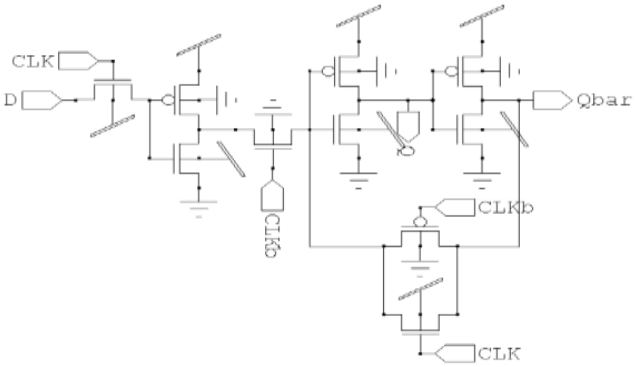

Fig 1. 10-Transistor SET D-FF of LVSB

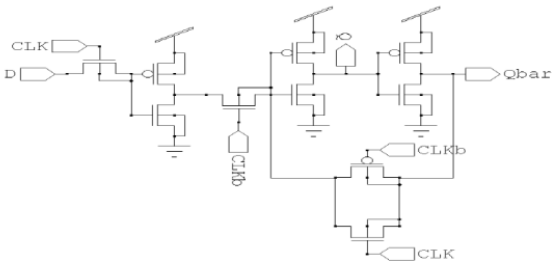

Fig 3. 10-transistor SET D-FF of NBB

IV SIMULATION

The 10-transistor SET D-Flip Flop designs are simulated in 180nm technology. table I shows the comparison of 10-transistor SET D-Flip Flop in case of LVSB, STGB and NBB power wise by applying pulse wave. By observing Table I NBB generates its best with pulse wave as source. Table II provides the comparison of 10-transistor SET D-Flip Flop in case of LVSB, STGB and NBB by applying sine wave, It is transparent that again NBB provides it's best with sine wave as input. By observing Table III it is clear that NBB is the best one with sine wave.

Hence power delay product is calculated for pulse and sine wave with NBB design. LVSB, STGB and NBB designs work under the principle of D Flip Flop. D Flip Flop is provided with clock to drive the output from the inputs. These designs generate output waveforms as clock is applied with high level Q will be high, because Q is clock follower. Q, Clock will generate it's against outputs respectively.

In this research this designs are tested with pulse and sine wave. Pulse wave is applied with a time period of 10 seconds. Sine wave is applied with a frequency 0.1Hz

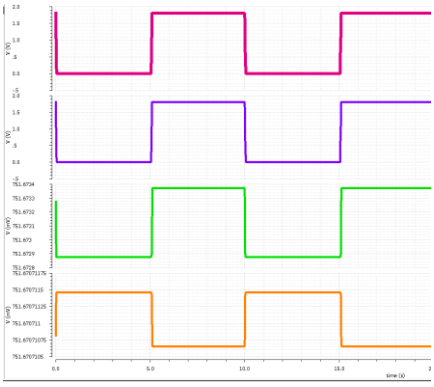

Fig 4. LVSB with Pulse Wave

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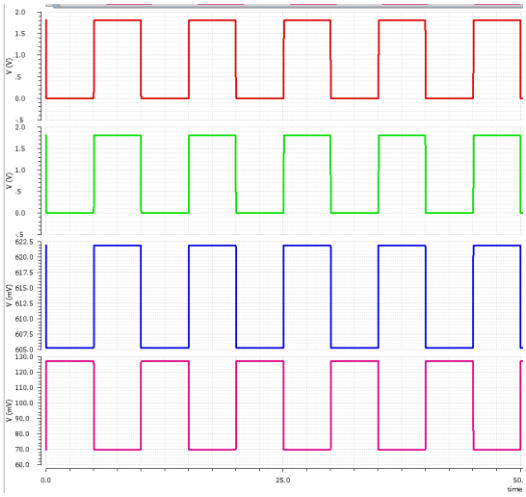

Fig 5. STGB With Pulse

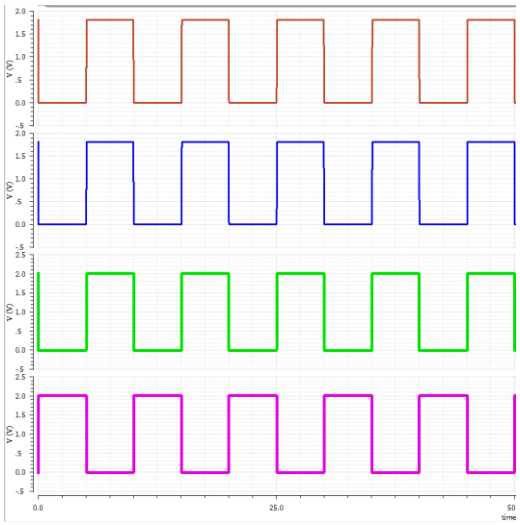

Fig 6. NBB With Pulse

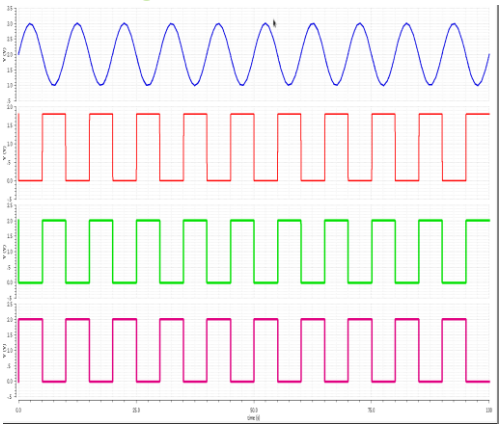

Fig 7. LVSB With Sine Wave

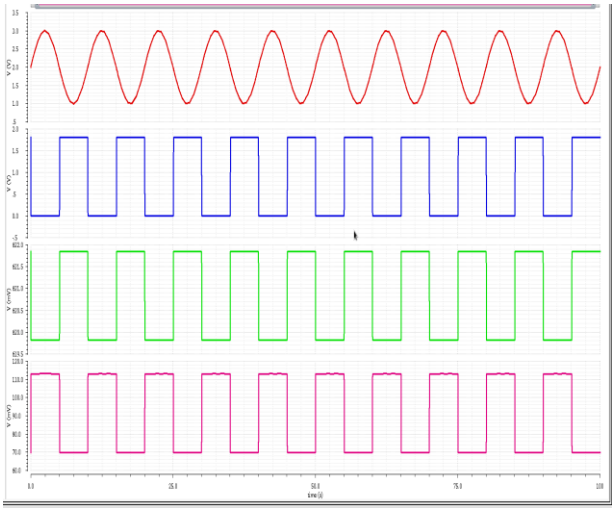

Fig 8. STGB With Sine

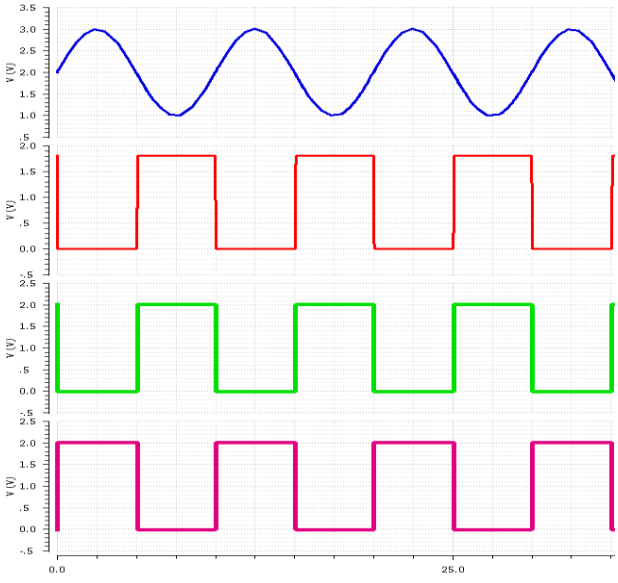

Fig 9. NBB With Sine

Comparison of 10-Transistor SET D-Flip Flop

If we see the Table7.4 we can observe that by applying pulse as input the power consumption of LVSB, STGB and NBB is 15.69Wt, 7.493Wt and 26.38μWt respectively. We can say that NBB consumes less power than LVSB and STGB.

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Table I. 10- Transistor SET D-Flip Flop Power Consumption

S.NO.	SET D-FLIP FLOP	POWER
1.	LVSB	15.69Wt
2.	STGB	7.493Wt
3	NBB	26.38µwt

Comparison of 10-Transistor SET D-Flip Flop With Sine

If we see the Table II we can observe that by applying sine as input the power consumption of LVSB, STGB and NBB is 15.69Wt, 7.493Wt and 24.11µWt respectively. We can say that NBB consumes less power than LVSB and STGB.

Table II. 10- Transistor SET D-Flip Flop Power Consumption

S.NO.	SET D-FLIP FLOP	POWER
1.	LVSB	15.69Wt
2.	STGB	7.493Wt
3	NBB	24.11µWt

Comparison of Quality Measures in case of Pulse and Sine

By providing pulse and sine wave to the No Body Bias (NBB) circuit power consumed is 26.38e-6,24.11e-6, Delay is 4.068, 1.495 and Power Delay Product is 107.3e-6,36.04e-6 respectively.

Table III. 10- Transistor SET D-Flip Flop Quality measures

S.NO.	NBB	POWER	DELAY	POWER DELAY PRODUCT
1.	Pulse	26.38e-6	4.068	107.3e-6
2.	Sine	24.11e-6	1.495	36.04e-6

V CONCLUSION

The project **"Design of SINGLE PHASE CONTINUOUS CLOCK SIGNAL SET D-FLIP FLOP FOR ULTRA LOW POWER VLSI APPLICATIONS"** has been successfully designed and tested. The NBB design of SET D-Flip Flop shows better performance in terms of power consumption, delay and power delay product. This design is tested in 180nm technology. NBB design of SET D-Flop Flop is suitable for portable applications as it is more power efficient.

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