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Analysis and Design of a Low offset high speed and low voltage double tail comparator

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Abstract: ***In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. A comparator is a circuit that accepts two voltages,V1 and V2 and outputs zero volts if V1>V2 or outputs a positive voltage level if V2>V1. Comparators can be built from operational amplifiers.Minimization in power consumption in analog-to-digital converter (ADCs) devices can be achieved by moving towards smaller feature size processes. On the other hand, as we move towards smaller feature size processes, the process variations and other non idealities will greatly affect the overall performance of the device. The performance limiting blocks in such ADCs are typically inter stage gain amplifiers and comparators. The power consumption, speed takes major roll on performance measurement of ADCs. In this paper we work on a dynamic Comparator circuit design for fast operation to work under small supply voltage conditions.***

Keywords: ***High speed analog-to-digital comparators(ADCs) , Dynamic clocked comparator, low power analog design, Double-taildynamic comparator, Voltage***

Introduction: In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals V+ and V- and one binary digital output V0. The output is ideally

$$V_o = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases}$$

A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs), as well as relaxation oscillators.

An operational amplifier (op-amp) has a well balanced difference input and a very high gain. This parallels the characteristics of comparators and can be substituted in applications with low-performance requirements.

In theory, a standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator. When the non-inverting input (V+) is at a higher voltage than the inverting input (V-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output. When the non-inverting input (V+) drops below the inverting input (V-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split-voltage power supply, (powered by ± V_S) has its transfer function typically written as: $V_{out} = A_o(V_1 - V_2)$. However, this equation may not be applicable to a comparator circuit which is non-linear and operates open-loop (no negative feedback).

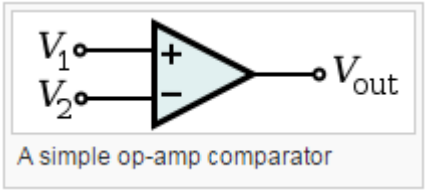

Fig : A simple Op –Amp Comparator

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A dedicated voltage comparator will generally be faster than a general-purpose operational amplifier pressed into service as a comparator. A dedicated voltage comparator may also contain additional features such as an accurate, internal voltage reference, an adjustable hysteresis and a clock gated input.

A dedicated voltage comparator chip such as LM339 is designed to interface with a digital logic interface (to a TTL or a CMOS). The output is a binary state often used to interface real world signals to digital circuitry (see analog to digital converter). If there is a fixed voltage source from, for example, a DC adjustable device in the signal path, a comparator is just the equivalent of a cascade of amplifiers. When the voltages are nearly equal, the output voltage will not fall into one of the logic levels, thus analog signals will enter the digital domain with unpredictable results. To make this range as small as possible, the amplifier cascade is high gain. The circuit consists of mainly Bipolar transistors. For very high frequencies, the input impedance of the stages is low. This reduces the saturation of the slow, large P-N junction bipolar transistors that would otherwise lead to long recovery times. Fast small Schottky diodes, like those found in binary logic designs, improve the performance significantly though the performance still lags that of circuits with amplifiers using analog signals. Slew rate has no meaning for these devices. For applications in flash ADCs the distributed signal across eight ports matches the voltage and current gain after each amplifier, and resistors then behave as level-shifters.

The LM339 accomplishes this with an open collector output. When the inverting input is at a higher voltage than the non inverting input, the output of the comparator connects to the negative power supply. When the non inverting input is higher than the inverting input, the output is 'floating' (has a very high impedance to ground). The gain of op amp as comparator is given by this equation V(out)=V(in).

Because comparators have only two output states, their outputs are near zero or near the supply voltage. Bipolar rail-to-rail comparators have a common-emitter output that produces a small voltage drop between the output and each rail. That drop is equal to the collector-to-emitter voltage of a saturated transistor. When output currents are light, output voltages of CMOS rail-to-rail comparators, which rely on a saturated MOSFET, range closer to the rails than their bipolar counterparts.

On the basis of outputs, comparators can also be classified as open drain or push–pull. Comparators with an open-drain output stage use an external pull up resistor to a positive supply that defines the logic high level. Open drain comparators are more suitable for mixed-voltage system design. Since the output is high impedance for logic level high, open drain comparators can also be used to connect multiple comparators on to a single bus. Push pull output does not need a pull up resistor and can also source current unlike an open drain output.

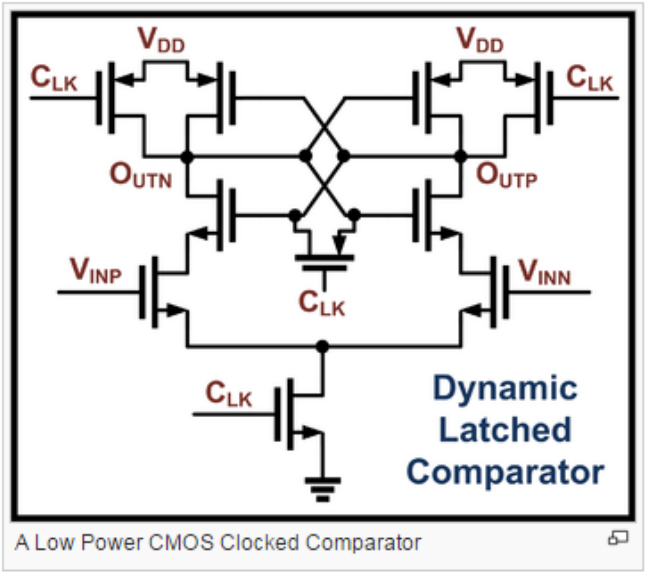

Fig : A Low Power CMOS Clocked Comparator

Proposed Dynamic Comparator

Figure demonstrates the schematic diagram of the proposeddynamic double-tail comparator. Due to the better performanceof double-tail architecture in low-voltage applications, theproposed comparator is designed based on the double-tail structure.

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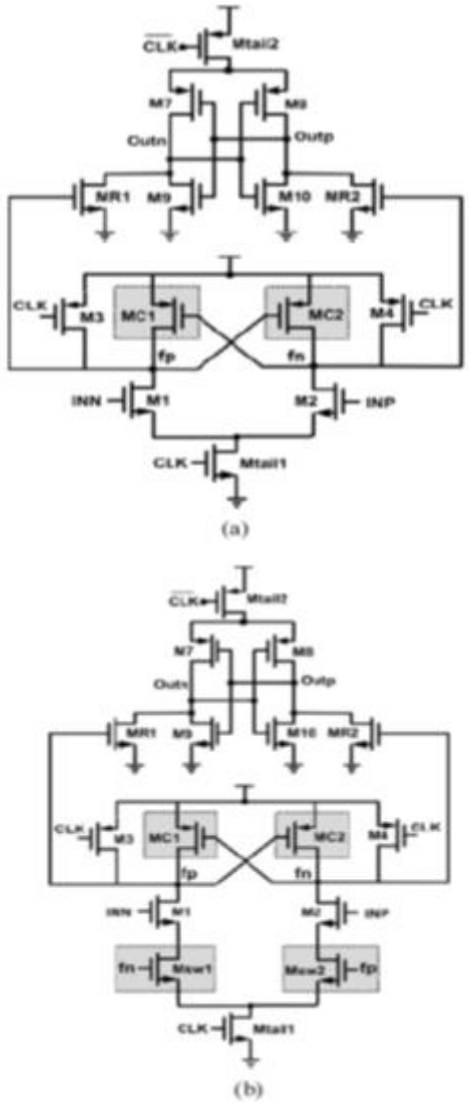

Fig.Schematic diagram of the proposed dynamic comparator. (a) Main idea. (b) Final structure.

The main idea of the proposed comparator is toincrease ΔVfn/fp in order to increase the latch regenerationspeed. For this purpose, two control transistors (*M*c1 and*M*c2) have been added to the first stage in parallel to *M*3/*M*4transistors but in a cross-coupled manner .

A. Operation of the Proposed Comparator

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off,avoiding static power), *M*3 and *M*4 pulls both fn and fp nodesto *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediatestage transistors, *M*R1 and *M*R2, reset both latch outputs toground.

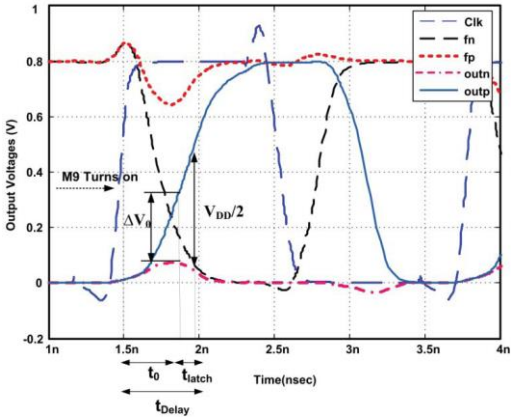

Fig. Transient simulations of the proposed double-tail dynamic comparator for input voltage difference of ΔVin= 5 mV, *V*cm= 0.7 V, and *V*DD = 0.8 V.

During decision-making phase (CLK = V_{DD}, *M*tail1, and*M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, atthe beginning of this phase, the control transistors are still off(since fn and fp are about *V*DD). Thus, fn and fp start to dropwith different rates according to the input voltages. Suppose*V*INP > *V*INN, thus fn drops faster than fp, (since *M*2 providesmore current than *M*1). As long as fn continues falling, thecorresponding pMOS control transistor (*M*c1 in this case) startsto turn on, pulling fp node back to the *V*DD; so another controltransistor (*M*c2) remains off, allowing fn to be dischargedcompletely. In other words, unlike conventional double-taildynamic comparator, in which ΔVfn/fp is just a function ofinput transistor transconductance and input voltage difference(9), in the proposed structure as soon as the comparator detectsthat for instance node fn discharges faster, a pMOS transistor(*M*c1) turns on, pulling the other node fp back to the V_{DD}.

Therefore by the time passing, the difference between fn andfp (ΔVfn/fp) increases in an exponential manner, leading tothe reduction of latch regeneration time (this will be shown inSection III-B). Despite the effectiveness of the proposed idea,one of the points which should be considered is that in thiscircuit, when

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one of the control transistors (e.g., *M*c1) turns on,a current from *V*DD is drawn to the ground via input and tailtransistor (e.g., *M*c1, *M*1, and *M*tail1), resulting in static powerconsumption. To overcome this issue, two nMOS switches are
used below the input transistors.

At the beginning of the decision making phase, due to thefact that both fn and fp nodes have been pre-charged to V_{DD} (during the reset phase), both switches are closed and fn andfp start to drop with different discharging rates. As soon as thecomparator detects that one of the fn/fp nodes is dischargingfaster, control transistors will act in a way to increase theirvoltage difference. Suppose that fp is pulling up to the $V_{DD}$and fn should be discharged completely, hence the switch inthe charging path of fp will be opened (in order to prevent anycurrent drawn from V_{DD}) but the other switch connected to fnwill be closed to allow the complete discharge of fn node. Inother words, the operation of the control transistors with theswitches emulates the operation of the latch.

B. Delay Analysis

In order to theoretically demonstrate how the delay isreduced, delay equations are derived for this structure as previously done for the conventional dynamic comparator andthe conventional double-tail dynamic comparator. The analysisis similar to the conventional double-tail dynamic comparator,however; the proposed dynamic comparator enhances thespeed of the double-tail comparator by affecting two importantfactors: first, it increases the initial output voltage difference($\Delta V0$) at the beginning of the regeneration ($t = t0$); andsecond, it enhances the effective transconductace ($g$meff) ofthe latch. Each of these factors will be discussed in detail.

Results:

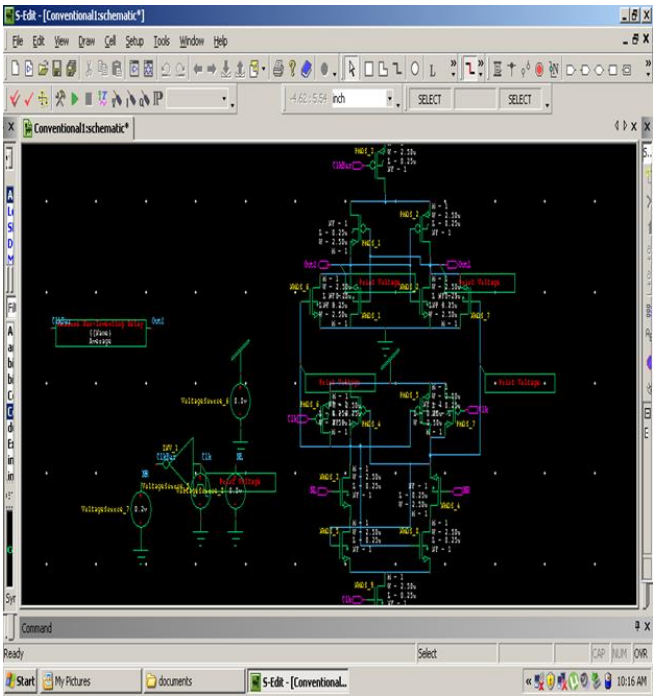

Fig :Schematic for Conventional Comparator

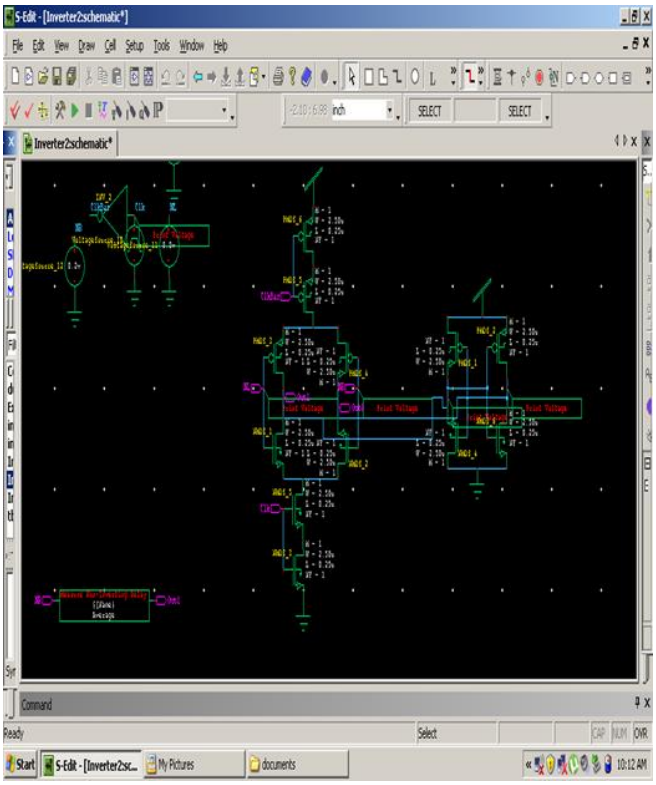

Fig :Schematic for Proposed Comparator

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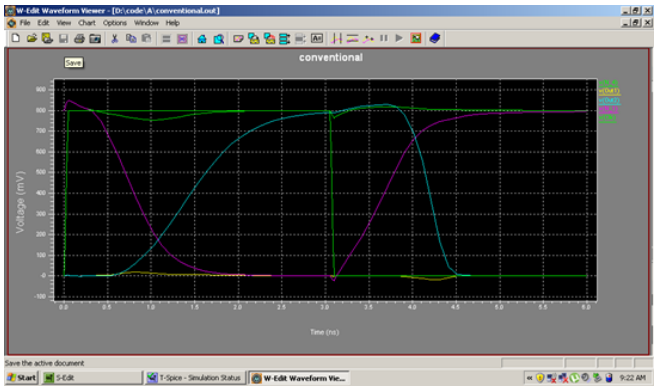

Fig :Waveforms for conventional comparator

Output Of Pre Layout Simulation Of Proposed Comparator

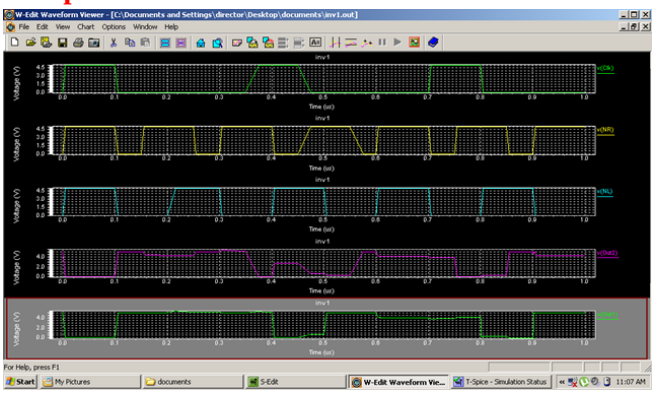

Fig :Waveforms for proposed comparator

Table Comparision Of Results

TYPE	AVERAGE POWER	MINIMUM POWER	MAXIMUM POWER	DELAY
CONVENTIONAL	7.342e-008 W	3.161e-004W	9.023e-011	-2.894e-009
PROPOSED	7.458e-011W	3.025e-004W	6.75e-011W	-3.094e-009

Conclusion :

A new proposed double-tail comparator shows better performance as compared to conventional dynamic and double-tail dynamic comparator. As it is shown that the delay of the proposed design is 263 Ps which is comparatively lesser than the earlier also energy per conversion is reducing from 1.108µ in conventional dynamic to 866 ns in proposed double-tail. The proposed double-tail dynamic comparator can be used for the design of high speed ADCs as the delay is reduced and hence the operation will be faster. As in the proposed structure the number of transistor is more so the area of the design is more which is one of the disadvantage of the above comparator.

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