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Design and Implementation of Network Topology for Digitally Enhanced Networks

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ABSTRACT:

VLSI technology has improved in integrating several Processor elements on the same chip. Connections between these Processor elements are the major issue and the Network on Chip (NoC) plays an important role in connecting these Processor elements. NoC has a high level of modularity, flexibility and throughput. The NoC comprises of routers, network interfaces and links allowing communication between the processing elements. The path to be traversed for a data packet between source and a destination through the routers is defined by the routing algorithm. In this paper, we are presenting a routing technique using Round Robin Method aimed at reducing the power dissipated by links of an NoC.

Index Terms: Neighbor position verification, mobile adhoc networks, vehicular networks.

I.INTRODUCTION:

RECENTLY the trend of embedded systems has been moving toward multiprocessor systems-on-chip(MPSoCs) in order to meet the requirements of real-time applications. The complexity of these SoCs is increasing and the communication medium is becoming a major issue of the MPSoC. The wiring modules on chip is not a viable solution in the billion transistor chips for the future.Generally, integrating a network-on-chip (NoC) into the SoC provides an effective means to interconnect several processor elements (PEs). The Network on Chip (NoC) is a good solution to support communication on System on Chip.

NoCs encounter many advantages (performance, structure and modularity) towards global signal wiring. The NoC architecture is characterized by the number of routers which is linked to processing elements in the array, the topology of the network and the mechanism used in data transmission.

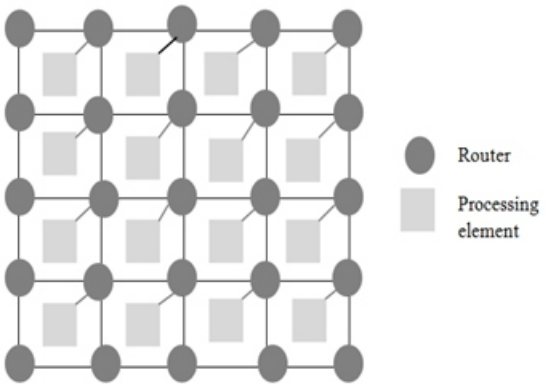

Fig.1. Network on Chip

The topology of the network is defined through the arrangement of routers and processor connection on the device. The most commonly used topology is the 2-D mesh topology, which looks like an arrangement of tiles as shown in Fig.1. NoC is built with routers and processing elements and/or IPs.The routers consists of FIFO buffers, control logic and arbiter. Buffers are used for storing the data in order to forward the message in First In First Out basis.The main function of the control logic is to synchronize the data transmission in the correct order to reach the destination from the source via particular router. The work of the arbiter is to avoid the congestion of data due to traffic, whereas the finite state machine in the arbiter forwards the data in a Round-robin scheduling.

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II.RELATED WORKS:

In order to meet the real time applications the trend of embedded system has been moving towards Multi-processor System on Chip (MpSoC), where the number of SoC is more. Increasing the number is becoming a burden for connecting medium.Connecting the SoC's through NoC gives an effective connection between the peripherals. The peripherals were connected through a shared bus in the earlier period, which can be either single or multiple shared busses connected using bypass bridges and pointto- point connection between the peripherals. Many applications adopt a low-voltage differential signaling (LVDS) system for data interface but it deals with analog signals which in this digital world is undesirable. This development of connection led to network on chip, where the peripherals are connected by splitting into certain sub circuits via NoC [2]. One of the main challenges of NoC is that it has to face the dynamically placed reconfigurable devices which later emerged as dynamic NoC [1]. Configurable network [11] was designed to obtain dynamic reconfiguration of FPGAs. The NoC is further modified to improve the performance and manage the dynamically placed modules using the inclusion of certain switching techniques [8] [6].

III.PROPOSED SYSTEM:

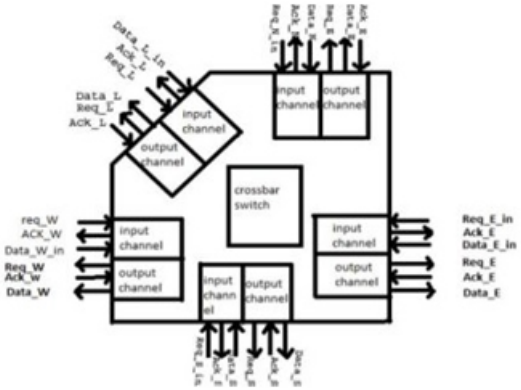
3.1 INTRODUCTION:

In packet switching the data transfers in the form of packets between cooperating routers and independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides.A router is a device that forwards data packets across computer networks. Routers perform the data "traffic direction" functions on the Internet.A router is a microprocessor-controlled device that is connected to two or more data lines from different networks. When a data packet comes in on one of the lines, the router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table, it directs the packet to the next network on its journey.

Data packet moves in to the input channel of one port of router by which it is forwarded to the output channel of other port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily. The buffering method used here is store and forward. Control logic is present to make arbitration decisions. Thus communication is established between input and output ports. According to the destination path of data packet, control bit lines of FSM are set. The movement of data from source to destination is called Packet Switching. The packet switching mechanism is used here, in which the flit size is 8 bits .Thus the packet size varies from 0 bits to 8 bits.

3.2 ROUTER ARCHITECTURE:

Fig 3.1 shows the router architecture of NoC. It consists of five ports such as east, west, north, south and local port. It also has a central cross bar switch. Inside each port there are two channels namely input and output channels. Data can be routed from any of the input port to the any of the output port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are used at all ports to store the data for a short time span. The store and forward method is used here for data transmission. Control logic is present to make decisions to grant access to a port request.



In this way communication is established between input and output ports. The connection or configuration is made between both with the central cross point matrix. According to the destination path of data packet, control bit lines of cross point matrix are set. The movement of data from source to destination is called switching mechanism. The packet switching mechanism is used here, in which the flit size is 8 bits .Thus the packet size varies from 8 bits to 120 bits.

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3.2 ROUND ROBIN ARBITRATION:

The arbiter traps the source and destination address from the output of buffer and generate the control signal so that input data from source side sending to the output port. Arbiter controls the arbitration of the ports and resolve contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the same priority and destined for the same output port are scheduled with a round-robin arbiter. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets could use the output by the arbitration of arbiter.

ARBITRATION METHOD:

Figure 3 shows the architecture of round robin arbitration which operates on the principle that a request-which was just served should have the lowest priority onthe next round of arbitration. Arbiter controls the arbitration of the ports and resolves contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the same priority and destined for the same output port are scheduled with a Round-Robin Arbiter. Supposing in a given period of time, there was many input ports request the same output or resource, the arbiter is in charge of processing the priorities among many different request inputs. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission.

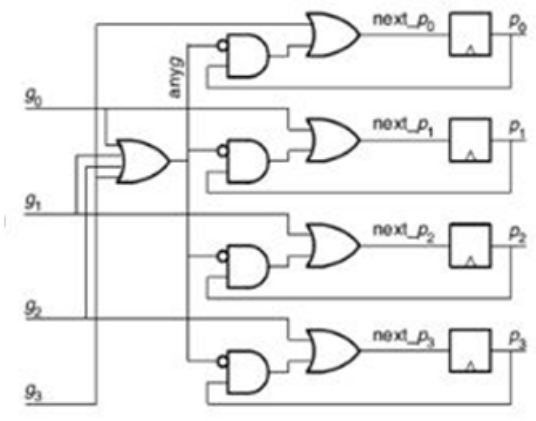


Fig..3. Architecture of Round Robin Arbitration

So that other waiting packets could use the output by the arbitration of arbiter. A round-robin arbiter operates on the principle that a request which was just served should have the lowest priority on the next round of arbitration. Depending upon the control logic arbiter generates select lines for multiplexer based crossbar and read or write signal for FIFO buffer. Contention resolution is an important task of arbiter. If two or more resources are sending data to one destination at same time then there isContention for destination. This contention can be resolved by assigning priorities to the resources based on different scheduling algorithms.

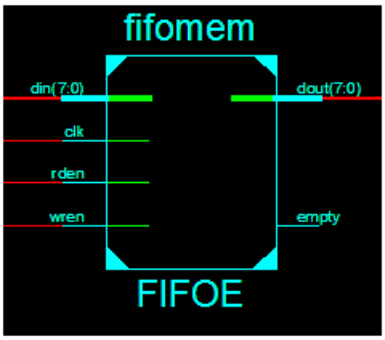
3.3 NOC ELEMENTS:

The router consists of the input ports, output ports and cross bar switch. Each input port and Output consists of the following elements:

a)FIFO
b)FSM
c)Cross Bar Switch

FIFO:

In the FIFO (First In First Out), the inputs are stored and forwarded. So this method is also called as store and forward technique.



Whenever data is loaded into the flipflop rden(Read Enable) is enabled data is stored in the flip flop. Similalrly, when data is transmitted to the cross bar switch wren(Write Enable) pin is enabled and data is transferred to switch. Each FIFO has clock signal(clk) and every operation is done at the rising edge of clock. The empty pin acts like an acknowledgement whether the data is transferred or not.

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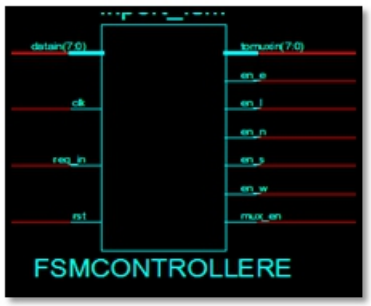
FSM:

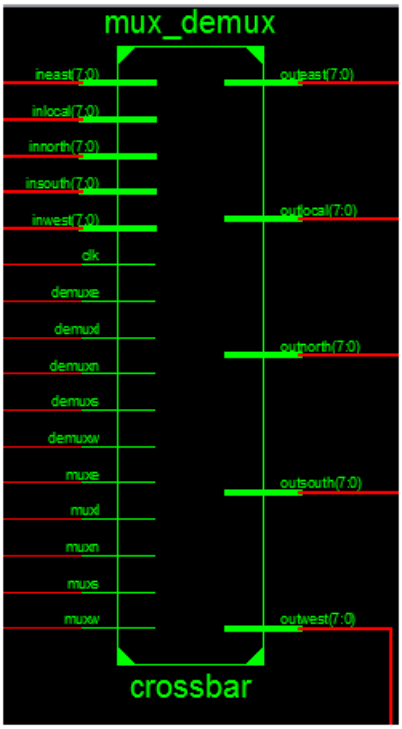
It defines the state. Initially the header is fixed along with the address followed by the data.



The FSM Controller transfers the data received from FIFO to the Cross Bar Switch. It has a request signal which enables the input to route to the exact destination.

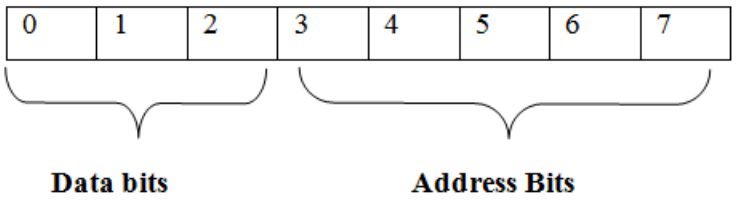
CROSS BAR SWITCH:

The Cross Bar Switch is a MUX DEMUX network.It operates on the request signal granted by the Round Robin Network. For example, if the request signal is 10000 it enables the datouts line and transmits the data to the particular output line.



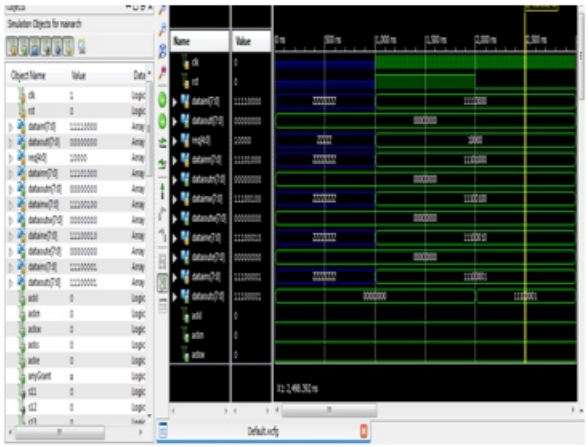
3.4 ROUTER DATA FORMAT:

The data transmitted is a 8-bit data. Out of the 8-bits First 3-bits are the actual data bits and the remaining bits are address bits of the output ports. The address bits and the request bits of the round robin arbitrary should match, then only the data is transmitted successfully.



RESULTS

OUTPUT:



POWER ANALYSIS:

Finally, we analyze and compare the power consumption of the two mechanisms. In Fig, we can see that the power consumption will increase as the number of inputs is increasing. The packet switching method consumes higher power than round-robin arbiter. In the design of our proposed scheme, we should make a trade-off among the resource, area, delay and power consumption, and choose suitable mechanism according to that.

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	232	2400	10
Signals	0.000	323	---	---
IOs	0.000	92	102	90
Leakage	0.014			
Total	0.014			

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CONCLUSION:

The proposed switching technique fulfilled the requirement of implementing a low area and low power communication path for on-chip networks. In this paper, address based packet switching round robin arbiter method are designed implemented on FPGA platform. Our proposed system is analyzed in terms of power and area by comparing with the existing scheme. The analysis shows that the arbiter which is designed based on address based the packet switching is having less area and power compared with the existing conventional matrix arbiter method.

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