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Reducing Network-on-Chip Energy Consumption through Data Encoding Techniques

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ABSTRACT:

We focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales As technology shrinks, the power dissipated by the links of a network-on-chip (NoC) starts to compete with the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces (NIs). In this paper, we present a set of data encoding schemes aimed at reducing the power dissipated by the links of an NoC. The proposed schemes are general and transparent with respect to the underlying NoC fabric (i.e., their application does not require any modification of the routers and link architecture). Experiments carried out on both synthetic and real traffic scenarios show the effectiveness of the proposed schemes, which allow to save up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation and with less than 15% area overhead in the NI.

Key words:

Coupling switching activity, data encoding, interconnection on chip, low power, network-on-chip (NoC),power analysis.

1. INTRODUCTION:

Shifting from a silicon technology node to the next one results in faster and more power efficient gates but slower and more power hungry wires [1]. In fact, more than 50% of the total dynamic power is dissipated in interconnects in current processors, and this is expected to rise to 65%–80% over the next several years [2].

Global interconnect length does not scale with smaller transistors and local wires. Chip size remains relatively constant because the chip function continues to increase and RC delay increases exponentially. At 32/28 nm, for instance, the RC delay in a 1-mm global wire at the minimum pitch is 25× higher than the intrinsic delay of a two-input NAND fanout of 5 [1]. If the raw computationhorsepower seems to be unlimited, thanks to the abilityy of instancing more and more cores in a single silicon die, scalability issues, due to the need of making efficient and reliable communication between the increasing number of cores, become the real problem [3].

The network on- chip (NoC) design paradigm [4] is recognized as the most viable way to tackle with scalability and variability issues that characterize the ultra deep sub micron meter era. Nowadays, the on-chip communication issues are as relevant as, and in some cases more relevant than, the computation related issues [4]. In fact, the communication subsystem increasingly impacts the traditional design objectives, including cost (i.e., silicon area), performance, power dissipation, energy consumption, reliability, etc.

As technology shrinks, an ever more significant fraction of the total power budget of a complex many-core system-on-chip (SoC) is due to the communication subsystem. In this paper, we focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales [5].In particular, we present a set of data encoding schemes operating at flit level and on an end-to-end basis, which allows us to minimize both the switching activity and the coupling switching activity on links of the routing paths traversed by the packets.

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The proposed encoding schemes, which are transparent with respect to the router implementation, are presented and discussed at both the algorithmic level and the architectural level, and assessed by means of simulation on synthetic and real traffic scenarios. The analysis takes into account several aspects and metrics of the design, including silicon area, power dissipation, and energy consumption. The results show that by using the proposed encoding schemes up to 51% of power and up to 14% of energy can be saved without any significant degradation in performance and with 15% area overhead in the NI.

RELATED WORKS AND CONTRIBUTIONS:

In the next several years, the availability of the chips with 1000 cores is foreseen [6]. In these chips, a significant fraction of the total system power budget is dissipated by interconnection network. Therefore, the design of power efficient interconnection networks has been the focus of many works published in the literature dealing with NoCarchitecture. These works concentrate on different components of the interconnection networks such as routers, NI, and links. Since the focus of this paper is on reducing the power dissipation by the links, in this section, briefly review some of the works in the area of link power reduction. These include the techniques that make use of shielding [7], [8], increasingline-to-line spacing [9], [10], repeater insertion [11]. They all increases the chip area.

The data encoding scheme is another method that was employed to reducing the link power dissipation. The data encoding techniques may be classified into two types. In the first type, encoding techniques concentrate on lowering the power due to self-switching activity of individual bus lines while ignoring the power dissipation owing to their coupling switching activity. In this type, bus invert (BI) [12] and INC-XOR [13] have been proposed for the case that random data patterns are transmitted through these lines. On the other hand, gray code [14], T0 [15], working-zone encoding [16], and T0-XOR [17] were suggested for the case of correlated data patterns. Application specific approaches have also been proposed [18]–[22].This category of encoding is not suitable to applied in the deep sub micron meter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance.

This causes the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption, making the above mentioned techniques, which ignore such contributions, inefficient [23].The works in the second type concentrate on reducing power dissipation through the reduction of the coupling witching [10], [22] Among these schemes [10], [24]– [28], the switching activity is reduced using many extra control lines. For example, data bus width grows from 32 to 55 in [24]. The techniques proposed in [20] have a smaller number of control lines but the complexity of their decoding logic is high. The technique is described as follows: first, the data are both odd inverted and even inverted, and the transmission is performed using the kind of inversion that reduces more the switching activity. In [30],the coupling switching activity is reduced up to 39%.

In this paper, compared to [30], we use a simpler encoder and decoder while achieving a higher activity reduction. Let us now discuss in more detail the works with which we compare our proposed data encoding schemes. In [12], the number of transitions from 0 to 1 for two consecutive flits (the flit that just traversed and the one which is about to traverse the link) is counted. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without worrying the coupling switching.

III. PROPOSED ENCODING SCHEMES:

In this section, present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activity on the links of the interconnection network. Let us first describe the power model that contains the different components of power dissipation of a link.. One can classify four types of coupling transitions. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high, other makes transition from high to low . A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change. The effective switched capacitance varies from type to type and hence, the coupling transition activity, is a weighted sum of different types of coupling transition contributions.

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Here, we calculate the occurrence probability for different types of transitions. Consider that flit (t – 1) and flit (t) refer to the previous flit which was transferred through the link and the flit is about to pass through the link, respectively. We consider only two adjacent bits of the physical channel. Sixteen different combinations of these four bits could occur (Table I). Note that the first bit is the value of the generic i th line of the link, whereas the second bit represents the value of its (i + 1)th line.

The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively. In the rest of this section, we present three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder.

A.SCHEME I:

In Scheme I, we focus on reducing Type I transitions while in Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert depending the amount of switching reduction. Finally, in Scheme III, we consider the fact that Type I transitions show different behaviors in the case of odd and even invert and make the inversion which leads to the higher power saving. In scheme I, we focus on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compare the current data with the previous data one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction.

Table I reports, for each transition, the relationship between the coupling transition activities of the flit when transmitted and when its bits are odd inverted. Data are organized as follows. The first bit is the value of the generic i th line of the link, whereas the second bit represent the value of its (i + 1)th line. For each partition, the first line represents the values at time t – 1(t). In the case of Type I transitions, the inversion leads to one of Types II, III, or Type IV transitions. In particular, the transitions indicated as T1, T1,andT1 in the table convert to Types II, III, and IV transitions, respectively.

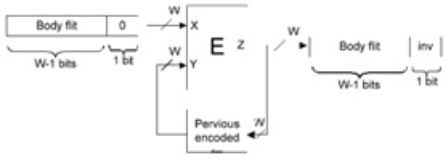

Fig:Circuit diagram of encoder architecture of scheme

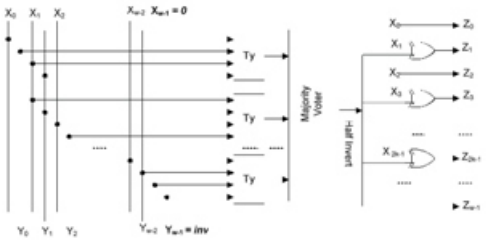

Fig: Internal view of encoder block

B.SCHEME II:

In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction. The w bits of the incoming body flit are indicated by Z I (R I), i = 0 , 1 ,...,w– 1. The w th bit of the body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). For the decoder, we only need to have the Ty block to determine which action has been taken place in the encoder. Based on the outputs of these blocks , the majority voter block checks the validity of the inequality .If the output is “0” (“1”) and the inv = 1,it means that half (full) inversion of the bits has been per-formed. Using this output and the logical gates, the inversion action is determined. If two inversion bits were used, the overhead of the decoder hardware could be substantially reduced.

This module determines if odd, even, full, or no invert action corresponding to the outputs “10,”“01,” “11,” or “00,”respectively, should be performed. The outputs “01,” “11,” and “10” show that whether respectively, are satisfied. In this paper, Module C was designed based on the conditions given .Similar to the procedure used to design the decoder for scheme II, the decoder for scheme III may be designed .This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception.

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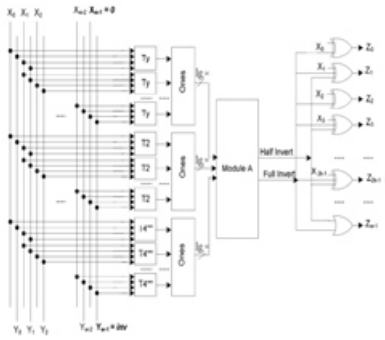

fig:Encoder architecture scheme II

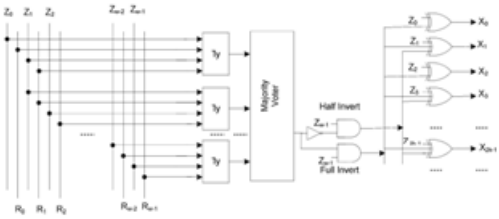

fig:Internal view of the decoder block scheme II

C.SCHEME III:

In the proposed encoding Scheme III, we add even inversion to Scheme II. The reason is that odd inversion converts some of Type I (T1) transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions indicated as T1/ T1 in the table are converted to Type IV/Type III transitions. Therefore, the even inversion may reduce the link power dissipation as well. The scheme compares the current data with the previous one to decide whether odd, even, full, or no inversion of the current data can give rise to the link power reduction.

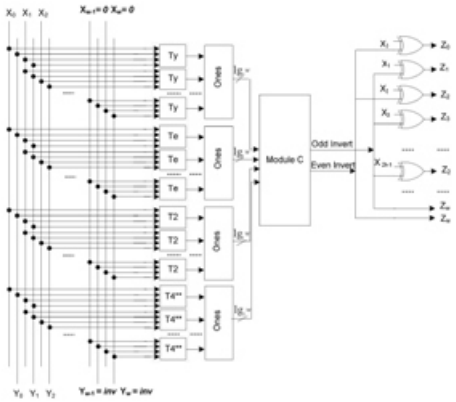

Fig:Encoder architecture scheme III

EFFECT OF EVEN INVERSION ON CHANGE OF TRANSITION TYPES:

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t-1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			00, 11		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			01, 10		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			10, 01, 11, 00		

IV. SIMULATION RESULTS:

The Data Encoding technique written in verilog, compiled and simulation using modelsim. The circuit simulated and synthesized. The simulated result for Data Encoding technique.

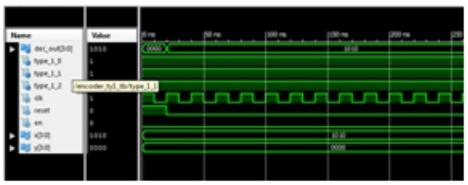

Fig. 5 Simulation Result.

V.CONCLUSION:

In this paper, a set of new data encoding schemes aimed at reducing the power dissipated by the links of an NoC. As compared to the previous encoding schemes the rationale behind the proposed schemes is to minimize not only the switching activity, but also the coupling switching activity which is mainly responsible for link power dissipation. By using the proposed encoding schemes in NoC architecture their application does not require any modification neither in the routers nor in the links. As per the performance evaluation results, the proposed system has lower dynamic power dissipation than classical one.

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