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An Improved Design of Router Structure for Fast Encoding

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ABSTRACT:

Network-On-Chip (NOC) structure makes a fitting substitution for system on chip designs incorporating large number of processing cores. In network the main source of power dissipation is in the network on chip links. The dynamic power dissipation in links is major contributor to the power consumption in NOC. This effort investigsates the reduction of transition activity using gray coding schemes. Our advanced scheme does not require any change of the routers and link architecture. The future scheme uses the binary to gray conversion at the transmitter and gray to binary conversion at the receiver. An investigational result has shown the effectiveness of the proposed schemes, with respect of power dissipation and area overhead in the Network Interface (NI) as compared with data encoding.

Index Terms—Neighbor position verification, mobile ad hoc networks, vehicular networks

INTRODUCTION:

In accordance with Moore‘s law density of transistors doubles every 18 months and currently we all know that there are millions of FETs on a single chip is known as VLSI. Integrating these FETs combine together to perform set of operations and applications such as DSP, Communications, Robotics and medical filed. Network on chip is a communication subsystem an on integrated circuit typical between IP cores in a system on a chip (SOC). NOC Technology applied methods to on chip communication and brings notable improvement over conventional bus and crossbar interconnections. NOC improves the scalability of SOC‘s and the power efficiency of complex SOC‘s compared to other designs. A network on chip uses packets to transfer data between IP core interfaces within a chip. The NOC based system on chips imposes various design issues on the fabrication of such integrated chips. Firstly, the suitable topology for the target NOCs such that the presentation supplies and design constraints are satisfied. Secondly, the design of network interfaces to access the on chip network and routers provide the physical interconnection mechanisms to transport data between processing cores. Finally, as technology scales and switching speed increases, future network on chips will become more responsive and prone to errors and faults.

Existing System

The accessibility of chips are growing every years. In the next several years, the availability of cores with 1000 cores is foreseen. Since the focus of this paper is on reducing the power dissipated by the links, here we briefly review some of the works in the area and link power reduction. Also these include some technique. There are, use of shielding increasing line-to-line spacing and repeater insertion . Thus the above all the techniques having large area overhead. Another one method is the data encoding technique it mainly focus on reducing the link power reduction. The data encoding technique is classified into two categories. In the first category is mainly concentrate on minimizing the power due to self-switching activity of each bus lines and avoid the power dissipation due to coupling switching activity.

Proposed System:

The basic idea of the proposed technique is the packets are transferred through the network after that the bits are encoded. This technique is more helping to reduce

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the switching activity and coupling switching activity in the links traversed by the packets. This self-switching activity and coupling switching activity are responsible for the link power dissipation. Here we refer to end-to-end scheme. Based on the end to end scheme we are having a better advantage. The advantage is a pipeline nature of the wormhole switching technique . Since the same sequence of all the packets passes through all the links of the routing path. The NI may provide the same power saving for all the links. The advanced scheme, an encoder and decoder block are added to the NI. The gray input is applied for all the three scheme encoders. The gray coding technique is used for the error correction application. The encoder encodes allthe leaving bits of the packets other than header bit such that the power dissipated by the inter router and point-to— point link is minimized.

CONFIGURABLE ELEMENTS

The FPGA has three major elements: Configurable logic blocks, input/output blocks and interconnects. The CLBs provide the functional elements for constructing user's logic. The IOBs provide the interface between the package pins and internal signal lines. The programmable interconnect resources provide routing paths to connect the inputs and outputs of the CLBs and IOBs into the appropriate networks. The field-programmable Gate Array provide the benefits of custom MOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array. The FPGAs are customized by loading configuration data into the internal memory cells. Complex programmable logic Devices and Field programmable Gate Array are becoming a critical part of every system design. There are many different FPGAs with different architectures/ processes. There are four main categories of FPGAs currently and sea-of-gates .In all of these FPGAs the interconnections and how they are programmed vary.

TECHNOLOGIES

Currently there are four technologies in use. They are: static RAM cells, anti-fuse, EPROM transistors, and EEPROM transistors. Depending upon the applications, one FPGA technology may have features desirable for that application.

1. Static RAM Technology

In the Static RAM EPGA programmable connections are made using pass-transmission, transmission gates, or multiplexers that are controlled by SRAM cells. This technology allows fast in-circuit reconfiguration. The major disadvantage is the size of the chip required by the RAM technology and that the chip configuration needs to be loaded to the chip from some external source (usually external non-volatile memory chip). The FPGA can either actively read its configuration data out of external serial or byte-parallel PROM (master mode), or the configuration data can be written into the FPGA (slave and peripheral mode). The FPGA can be programmed an unlimited number of times.

2. Anti-Fuse Technology

An anti-fuse resides in a high-impedance state; and can be programmed in to low impedance or "fused" state. This technology can be used to make program once devices that are less expensive than the RAM technology.

3.EPROM Technology

This method is the same as used in the EPROM memories. The programming is stored without external storage of configuration. EPROM based programmable chip cannot be re-programmed in circuit and need to be cleared with UV erasing.

4.EEPROM Technology

This method is the same as used in the EEPROM memories. The programming is stored without external storage of configuration. EEPROM based programmable chips can be electrically erased but generally cannot be re-programmed in-circuit FUSE-One-time programmable.

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DESIGN PROCESS ALGORITHM

Step 1: Understand the problem.
Step 2: Draw the block diagram (data path)
Step 3: Design the state machine (control)
Step 4: Code in VHDL or Verilog
Step 5: Simulate it (ensure the functional correctness)
Step 6: Synthesis it (get the EDIF file)
Step 7: Implement it (get the bit file)
Step 8: Write the software driver
Step 9: Download to FPGA and get results

Spartan applications

1.The Spartan series targets applications with a low-power footprint, extreme cost sensitivity and high-volume; e.g. displays, set-top boxes, wireless routers and other applications.
2.The Spartan-6 family is built on a 45-nanometer [nm], 9-metal layer, dual-oxide process technology. The Spartan-6 was marketed in 2009 as a low-cost solution for automotive, wireless communications, flat-panel display and video surveillance applications.

Modelsim

Modelsim is a widely used logic simulation tool for verification and debugging of digital circuits. Modelsim is a verification and simulation tool for VHDL, Verilog, System Verilog, and mixed language designs

Procedure

- Create a working library
- Compile design files
- Load and Run simulation
- Debug results

Representation

- Data flow representation
- Waveform representation
- Time representation

CONCLUSION:

In this work, the gray encoding technique is implemented for reducing the transition activity in the NOC. This gray encoding scheme aimed at reducing the power dissipated by the links of an NOC. In fact links are responsible for a significant fraction of the overall power dissipated by the communication system. The proposed encoding schemes are agnostic with respect to the underlying NOC architecture in the sense that our application does not require any modification neither in the links nor in the links. The proposed architecture is coded using VERILOG language and is simulated and synthesized using cadence software. Overall, the application scheme allows savings up to 42% of power dissipation and with less than 5% area overhead in the NI compared to the data encoding scheme. In the future, the Network On Chip (NOC) implementation using different types of router technique will be analyzed . Comparison on many encoding techniques such as gray encoding techniques will be analyzed in which the area, delay, power and the performance of the NOC will be investigated and use for high speed applications

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