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An Improved Image Compressor Using Fast DCT Algorithm

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ABSTRACT: ***Video processing systems such as HEVC requiring low energy consumption needed for the multimedia market has lead to extensive development in fast algorithms for the efficient approximation of 2-D DCT transforms. The DCT is employed in a multitude of compression standards due to its remarkable energy compaction properties. Multiplier-free approximate DCT transforms have been proposed that offer superior compression performance at very low circuit complexity. Such approximations can be realized in digital VLSI hardware using additions and subtractions only, leading to significant reductions in chip area and power consumption compared to conventional DCTs and integer transforms. In this paper, we introduce a novel 8-point DCT approximation that requires only 14 addition operations and no multiplications. The proposed transform possesses low computational complexity and is compared to state-of-the-art DCT approximations in terms of both algorithm complexity and peak signal-to-noise ratio. The proposed DCT approximation is a candidate for reconfigurable video standards such as HEVC. The proposed transform and several other DCT approximations are mapped to systolic-array digital architectures and physically realized as digital prototype circuits using FPGA technology and mapped to 45 nm CMOS technology.***

Index Terms—Approximate DCT, low-complexity algorithms, image compression, HEVC, low power consumption.

INTRODUCTION:

RECENT years have experienced a significant demand for high dynamic range systems that operate at high resolutions [1]. In particular, high-quality digital video in multimedia devices [2] and video-over-Internet protocol networks [3] are prominent areas where such requirements are evident. Other noticeable fields are geospatial remote sensing [4], traffic cameras [5], automatic surveillance [1], homeland security [6], automotive industry [7],and multimedia wireless sensor networks [8], to name but a few. Often hardware capable of significant throughput is necessary; as well as allowable area-time complexity [8]. In this context, the discrete cosine transform (DCT) [9]–[11] is an essential mathematical tool in both image and video coding [8], [11]–[15]. Indeed, the DCT was demonstrated to provide good energy compaction for natural images, which can be described by first-order Markov signals [10], [11], [13]. Moreover, in many situations, the DCT is a very close substitute for the Karhunen-Loève transform (KLT), which has optimal properties [9]–[11], [13], [14], [16]. As a result, the two-dimensional (2-D) version of the 8-point DCT was adopted in several imaging standards such as JPEG [17], MPEG-1 [18], MPEG-2 [19], H.261 [20], H.263, and H.264/AVC. Additionally, new compression schemes such as the High Efficiency Video Coding (HEVC) employs DCT-like integer transforms operating at various block sizes ranging from 4 4 to 32 32 pixels . The distinctive characteristic of HEVC is its capability of achieving high compression performance at approximately half the bit rate required by H.264/AVC with same image quality. Also HEVC was demonstrated to be especially effective for high-resolution video applications. However, HEVC possesses a significant computational complexity in terms of arithmetic operations. In fact, HEVC can be 2–4 times more computationally demanding when compared to H.264/AVC. Therefore,

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low complexity DCT-like approximations may benefit future video codecs including emerging HEVC/H.265 systems

Existing System:

RECONFIGURABLE DCT-LIKE FAST ALGORITHMS IN VIDEO CODECS

In current literature, several approximate methods for the DCT calculation have been archived [11]. While not computing the DCT exactly, such approximations can provide meaningful estimations at low-complexity requirements. In particular, some DCT approximations can totally eliminate the requirement for floating-point operations—all calculations are performed over a fixed-point arithmetic framework. Prominent 8-point approximation-based techniques were proposed in [14], [15]. Works addressing 16-point DCT approximations are also archived in literature. In general, these approximation methods employ a transformation matrix whose elements are defined over the set . This implies null multiplicative complexity, because the required operations can be implemented exclusively by means of binary additions and shift operations. Such DCT approximations can provide low-cost and low-power designs and effectively replace the exact DCT and other DCT-like transforms. Indeed, the performance characteristics of the low complexity DCT approximations appear similar to the exact DCT, while their associate hardware implementations are economical because of the absence of multipliers [14], [15]. As a consequence, some prospective applications of DCT approximations are found in real-time video transmission and processing.

REVIEW OF APPROXIMATE DCT METHODS

In this section, we review the mathematical description of the selected 8-point DCT approximations. All discussed methods here consist of a transformation matrix that can be put in the following format: The diagonal matrix usually contains irrational numbers in the form , where is a small positive integer. In principle, the irrational numbers required in the diagonal matrix would require an increased computational complexity. However, in the context of image compression, the diagonal matrix can simply be absorbed into the quantization step of JPEG-like compression procedures [15]. Therefore, in this case, the complexity of the approximation is bounded by the complexity of the low-complexity matrix. Since the entries of the low complexity matrix comprise only powers of two in, null multiplicative complexity, Is achieved.

Proposed System:

We aim at deriving a novel low-complexity approximate DCT. For such end, we propose a search over the 8 8 matrix space in order to find candidate matrices that possess low computation cost. Let us define the cost of a transformation matrix as the number of arithmetic operations required for its computation. One way to guarantee good candidates is to restrict the search to matrices whose entries do not require multiplication operations. Thus we have the following optimization problem:

$$\mathbf{T}^* = \arg\min_{\mathbf{T}} \text{cost}(\mathbf{T}), \qquad (1)$$

where $\mathbf{T}^*$ is the sought matrix and $\text{cost}(\mathbf{T})$ returns the arithmetic complexity of $\mathbf{T}$. Additionally, the following constraints were adopted:

1) Elements of matrix $\mathbf{T}$ must be in $\{0, \pm 1, \pm 2\}$ to ensure that resulting multiplicative complexity is null;
2) We impose the following form for matrix $\mathbf{T}$:

$$\mathbf{T} = \begin{bmatrix} a_3 & a_3 & a_3 & a_3 & a_3 & a_3 & a_3 & a_3 \\ a_0 & a_2 & a_4 & a_6 & -a_6 & -a_4 & -a_2 & -a_0 \\ a_1 & a_5 & -a_5 & -a_1 & -a_1 & -a_5 & a_5 & a_1 \\ a_2 & -a_6 & -a_0 & -a_4 & a_4 & a_0 & a_6 & -a_2 \\ a_3 & -a_3 & -a_3 & a_3 & a_3 & -a_3 & -a_3 & a_3 \\ a_4 & -a_0 & a_6 & a_2 & -a_2 & -a_6 & a_0 & -a_4 \\ a_5 & -a_1 & a_1 & -a_5 & -a_5 & a_1 & -a_1 & a_5 \\ a_6 & -a_4 & a_2 & -a_0 & a_0 & -a_2 & a_4 & -a_6 \end{bmatrix}$$

where $a_i \in \{0, 1, 2\}$, for $i = 0, 1 \ldots, 6$;

3) All rows of $\mathbf{T}$ are non-null;
4) Matrix $\mathbf{T} \cdot \mathbf{T}^\top$ must be a diagonal matrix to ensure orthogonality of the resulting approximation [49].

Constraint 2) is required to preserve the DCT-like matrix structure. We recall that the *exact* 8-point DCT matrix is given by [35]:

$$\mathbf{C} = \frac{1}{2} \cdot \begin{bmatrix} \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 \\ \gamma_0 & \gamma_2 & \gamma_4 & \gamma_6 & -\gamma_6 & -\gamma_4 & -\gamma_2 & -\gamma_0 \\ \gamma_1 & \gamma_5 & -\gamma_5 & -\gamma_1 & -\gamma_1 & -\gamma_5 & \gamma_5 & \gamma_1 \\ \gamma_2 & -\gamma_6 & -\gamma_0 & -\gamma_4 & \gamma_4 & \gamma_0 & \gamma_6 & -\gamma_2 \\ \gamma_3 & -\gamma_3 & -\gamma_3 & \gamma_3 & \gamma_3 & -\gamma_3 & -\gamma_3 & \gamma_3 \\ \gamma_4 & -\gamma_0 & \gamma_6 & \gamma_2 & -\gamma_2 & -\gamma_6 & \gamma_0 & -\gamma_4 \\ \gamma_5 & -\gamma_1 & \gamma_1 & -\gamma_5 & -\gamma_5 & \gamma_1 & -\gamma_1 & \gamma_5 \\ \gamma_6 & -\gamma_4 & \gamma_2 & -\gamma_0 & \gamma_0 & -\gamma_2 & \gamma_4 & -\gamma_6 \end{bmatrix}$$

where $\gamma_k = \cos(2\pi(k+1)/32), k = 0, 1, \ldots, 6.$

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Above optimization problem is algebraically intractable. Therefore we resorted to exhaustive computational search. As a result, eight candidate matrices were found, including the transform matrix proposed in [39]. Among these minimal cost matrices, we separated the matrix that presents the best performance in terms of image quality of compressed images according the JPEG-like technique employed in [36]–[39], [41]–[44], and briefly reviewed in next Section V.

Proposed Architectures

We propose digital computer architectures that are custom designed for the real-time implementation of the fast algorithms described in Section III. The proposed architectures employs two parallel realizations of DCT approximation blocks, as shown in Fig. 5. The 1-D approximate DCT blocks (Fig. 5) implement a particular fast algorithm chosen from the collection described earlier in the paper. The first instantiation of the DCT block furnishes a row-wise transform computation of the input image, while the second implementation furnishes a column-wise transformation of the intermediate result. The row- and column-wise transforms can be any of the DCT approximations detailed in the paper. In other words, there is no restriction for both row- and column-wise transforms to be the same. However, for simplicity, we adopted identical transforms for both steps.

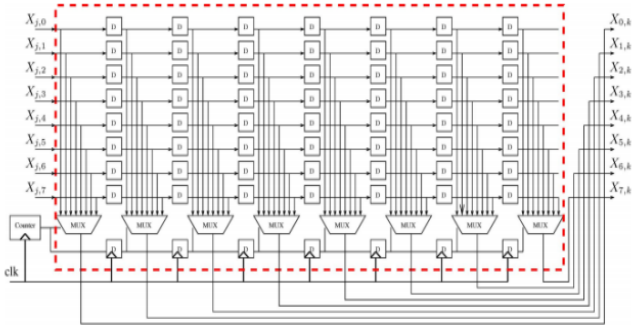


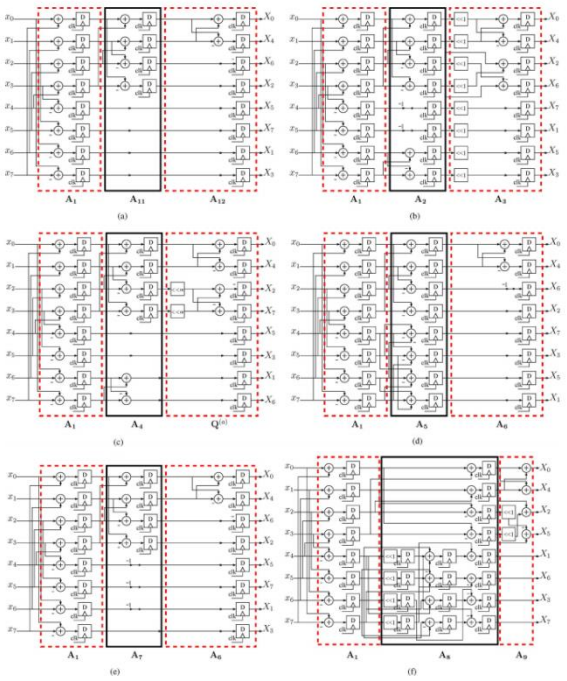
Fig. 6. Details of the transposition buffer block.

Xilinx FPGA Implementations

Discussed methods were physically realized on a FPGA based rapid prototyping system for various register sizes and tested using on-chip hardware-in-the-loop co-simulation. The architectures were designed for digital realization within the MATLAB environment using the Xilinx System Generator (XSG) with synthesis options set to generic VHDL generation. This was necessary because the auto-generated register transfer language (RTL) hardware descriptions are targeted on both FPGAs as well as custom silicon using standard cell ASIC technology

CMOS 45 nm ASIC Implementation

The digital architectures were first designed using Xilinx System Generator tools within the Matlab/Simulink environment. Thereafter, the corresponding circuits were simulated using bit-true cycle-accurate models within the Matlab/Simulink software framework. The architectures were then converted to corresponding digital hardware description language designs using the auto-generate feature of the System Generator tool. The resulting hardware description language code led to physical implementation of the architectures using Xilinx FPGA technology, which in turn led to extensive hardware co-simulation on FPGA chip. Hardware co-simulation was used for verification of the hardware description language designs which were contained in register transfer language (RTL) libraries



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CONCLUSION

In this paper, we proposed (i) a novel low-power 8-point DCT approximation that require only 14 addition operations to computations and (ii) hardware implementation for the proposed transform and several other prominent approximate DCT methods, including the designs by Bouguezel-Ahmad-Swamy. We obtained that all considered approximate transforms perform very close to the ideal DCT. However, the modified CB-2011 approximation and the proposed transform possess lower computational complexity and are faster than all other approximations under consideration. In terms of image compression, the proposed transform could outperform the modified CB-2011 algorithm. Hence the new proposed transform is the best approximation for the DCT in terms of computational complexity and speed among the approximate transform examined. Introduced implementations address both 1-D and 2-D approximate DCT. All the approximations were digitally implemented using both Xilinx FPGA tools and CMOS 45 nm ASIC technology. The speeds of operation were much greater using the CMOS technology for the same function word size. Therefore, the proposed architectures are suitable for image and video processing, being candidates for improvements in several standards including the HEVC. Future work includes replacing the FreePDK standard cells with highly optimized proprietary digital libraries from TSMC PDK [67] and continuing the CMOS realization all the way up to chip fabrication and post-fab test on a measurement system. Additionally, we intend to develop the approximate versions for the 4-, 16-, and 32-point DCT as well as to the 4-point discrete sine transform, which are discrete transforms required by HEVC.

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