ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System

Konduru Sumalatha
M.Tech (Power Electronics),
Shree Institute of Technical Education,
Mallavaram(v), Renigunta-Srikalahasti Highway
Tirupati(R), Chittoor (D), A.P.

M.Purushotham
Assistance Professor,
Dept of EEE,
Shree Institute of Technical Education,
Mallavaram(v), Renigunta-Srikalahasti Highway
Tirupati(R), Chittoor (D), A.P.

Abstract:

This paper proposes a new breed of high-voltage dc (HVDC) transmission systems based on a hybrid multilevel voltage source converter (VSC) with ac-side cascaded H-bridge cells. The proposed HVDC system offers the operational flexibility of VSC based systems in terms of active and reactive power control, black start capability, in addition to improved ac fault ride-through capability and the unique feature of current-limiting capability during dc side faults. Additionally, it offers features such as smaller footprint and a larger active and reactive power capability curve than existing VSC-based HVDC systems, including those using modular multilevel converters. To illustrate the feasibility of the proposed= HVDC system, this paper assesses its dynamic performance during steady-state and network alterations, including its response to ac and dc side faults.

Index Terms:

DC fault reverse blocking capability, hybrid multilevel converter with ac side cascaded H-bride cells, modular multilevel converter, voltage-source-converter high-voltage dc (VSCHVDC) transmission system.

I. INTRODUCTION:

I N the last decade, voltage-source-converter high-voltage dc (VSC-HVDC) transmission systems have evolved from simple two-level converters to neutral-point clamped converters and then to true multilevel converters such as modular converters [1]–[5]. This evolution aimed to lower semiconductor losses and increase power-handling capability of VSC-HVDC transmission systems to the level comparable to that of conventional HVDC systems based on thyristor current-source converters, improved ac side waveform quality in order to minimize or eliminate ac filters, reduced voltage stresses on converter transformers, and reduced converter overall cost and footprint [6]–[15]. With increased demand for clean energy, power system networks need to be reengineered to be more efficient and flexible and reinforced to accommodate increased penetration of renewable power without compromising system operation and reliability.

A VSC-HVDC transmission system is a candidate to meet these challenges due to its operational flexibility, such as provision of voltage support to ac networks, its ability to operate independent of ac network strength therefore makes it suitable for connection of weak ac networks such as offshore wind farms, suitability for multiterminal HVDC network realization as active power reversal is achieved without dc link voltage polarity change, and resiliency to ac side faults (no risk of commutation failure as with line-Commutating HVDC systems) [12], [16]–[22]. However, vulnerability to dc side faults and absence of reliable dc circuit breakers capable of operating at high-voltage restrict their application to point-to-point connection.

Present VSC-HVDC transmission systems rely on their converter station control systems and effective impedance between the point-of-common-coupling (PCC) and the converter terminals to ride-through dc side faults. With present converter technology, the dc fault current comprises the ac networks contribution through converter free-wheeling diodes and discharge currents of the dc side capacitors (dc link and cable distributed capacitors) [23], [24]. The magnitude of the dc-side capacitors' discharge current decays

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with time and is larger than the ac networks contribution. For this reason, dc fault interruption may require dc circuit breakers that can tolerate high let-through current that may flow in the dc side during the first few cycles after the fault, with high current breaking capacity and fast interruption time. Recent HVDC converter topologies with no common dc link capacitors, such as the modular multilevel converter (M2C), may minimize the magnitude and duration of the discharge current first peak [2], [12], [14], [23], [25]. There are two approaches to assist VSC-HVDC transmission systems to ride-through dc side faults. The first approach is to use a fast acting dc circuit breaker, with considerably high let-through current to tolerate the high dc fault discharge current that may flow in the dc side. This breaker must be capable of operating at high voltage and isolates temporary or permanent dc faults, plus have a relatively high-current-breaking capacity. Reference [26] presents a prototype 80-kV dc circuit breaker with dc current breaking capacity of 9 kA within 2ms. However, this first step is inadequate, as the operating voltage of present

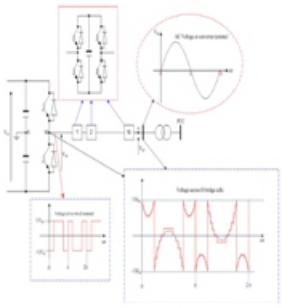

Fig. 1. Hybrid voltage multilevel converter with ac side cascaded H-bridge cells.

VSC-HVDC transmission systems reach 640 kV pole-to-pole (or 320 kV for a bi-polar configuration), with power-handling capability of 1 GW. This breaker approach may introduce significant steady-state losses due to the semiconductors in the main current path. The second approach is to use converter stations with dc fault reverse-blocking capability [1], [4], [23]. Each converter station must be able to block current flow between the ac and dc sides during a dc fault, allowing dc-side capacitor discharge current, which is the major component of the dc fault current, to decay to zero and then isolate the fault. Several converter topologies with this inherent feature have been proposed, including an H-bridge modular multilevel converter, an alternative arm modular multilevel converter, and a hybrid multilevel converter with ac-side cascaded H-bridge cells. However, the drawback is that the active power exchange between the ac networks reduces to zero during the dc fault period. Commensurate with the second approach, this paper presents a new HVDC transmission systems based on a hybrid-voltage-source multilevel converter with ac-side cascaded H-bridge cells.

The adopted converter has inherent dc fault reverse-blocking capability, which can be exploited to improve VSC-HVDC resiliency to dc side faults. With coordination between the HVDC converter station control functions, the dc fault reverse-blocking capability of the hybrid converter is exploited to achieve the following:

- eliminate the ac grid contribution to the dc fault, hence minimizing the risk of converter failure due to uncontrolled over current during dc faults;

- facilitate controlled recovery without interruption of the VSC-HVDC system from dc-side faults without the need for opening ac-side circuit breakers;

- simplify dc circuit breaker design due to a reduction in the magnitude and duration of the dc fault current; and

- improve voltage stability of the ac networks as converter reactive power consumption is reduced during dc-side faults.

Section II of this paper describes the operational principle and control of the hybrid voltage source multilevel converter with ac-side cascaded H-bridge cells. Section III describes the HVDC system control design, specifically, ac current controller in synchronous reference frame, dc link voltage, and active power, and ac voltage controllers.

A detailed block diagram that summarizes how different control layers of the proposed HVDC transmission system are interfaced is presented. Section IV presents simulations of a hybrid converter HVDC= transmission system, which demonstrate its response during steady-steady and network disturbances.

Included are simulations of four quadrant operation, voltage support capability, and ac and dc fault ride-through capabilities.

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II. HYBRID MULTILEVEL VSC WITH AC-SIDE CASCADED H-BRIDGE CELLS:

Fig. 1 shows one phase of a hybrid multilever VSC with N H-bridge cells per phase. It can generate voltage 4N+1 levels at converter terminal "a" relative to supply midpoint "0." Therefore, with a large number of cells per phase, the converter presents near pure sinusoidal voltage to the converter transformer as depicted in Fig. 1 [1]. The two-level converter that blocks high-voltage controls the fundamental voltage using selective harmonic elimination (SHE) with one notch per quarter cycle, as shown in Fig. 1. Therefore, the two-level converter devices operate with 150-Hz switching losses, hence low switching losses and audible noise are expected. The H-bridge cells between "M" and "a" are operated as a series active power filter to attenuate the voltage harmonics produced by the two-level converter bridge.

These H-bridge cells are controlled using level-shifted carrier-based multilevel pulsewidth modulation with a 1-kHz switching frequency. To minimize the conversion losses in the H-bridge cells, the number of cells is reduced such that the voltage across the H-bridge floating capacitors sum to (1/2) Vdc This may result in a small converter station, because the number of H-bridge cells required per converter with the proposed HVDC system is one quarter of those required for a system based on the modular multilevel converter. With a large number of cells per phase, the voltage waveform generated across the H-bridge cells is as shown in Fig. 1, and an effective switching frequency per device of less than 150 Hz is possible.

The dc fault reverse-blocking capability of the proposed HVDC system is achieved by inhibiting the gate signals to the converter switches, therefore no direct path exists between the ac and dc side through freewheel diodes, and cell capacitor voltages will oppose any current flow from one side to another. Consequently, with no current flows, there is no active and reactive power exchange between ac and dc side during dc-side faults. This dc fault aspect means transformer coupled H-bridges cannot be used. The ac grid contribution to dc-side fault current is eliminated, reducing the risk of converter failure due to increased current stresses in the switching devices during dc-side faults.

From the grid standpoint, the dc fault reverse-blocking capability of the proposed HVDC system may improve ac network voltage stability, as the reactive power demand at converter stations during dc-side faults is significantly reduced. The ac networks see the nodes where the converter stations are connected as open circuit nodes during the entire dc fault period.

However, operation of the hybrid multilevel VSC requires a voltage-balancing scheme that ensures that the voltages across the H-bridge cells are maintained Vdc/N at under all operating conditions, where Vdc is the total dc link voltage. The H-bridge cells voltage balancing scheme is realized by rotating the H-bridge cell capacitors, taking into account the voltage magnitude of each cell capacitor and phase current polarity. An additional PI regulator is used to ensure that the cell capacitors be maintained at Vdc/N as depicted in Fig. 2(b) (inner control layer).

III. CONTROL SYSTEMS:

A HVDC transmission system based on a hybrid multilevel VSC with ac-side cascaded H Bridge cells requires three control system layers. The inner control layer represents the modulator and capacitor voltage-balancing mechanism that generates the gating signals for the converter switches and maintains voltage balance of the H-bridge cell capacitors. The intermediate control layer represents the current controller that regulates the active and reactive current components over the full operating range and restraints converter station current injection into ac network during network disturbances such as ac and dc side faults. The outer control layer is the dc voltage (or active power) and ac voltage (or reactive power) controller that provide set points to the current controllers.

The inner controller has only been discussed to a level appropriate to power systems engineers. The intermediate and outer Control layers are presented in detail to give the reader a sense of HVDC control system complexity. The current, power, and dc link voltage controller gains are selected using root locus analysis, based on the applicable transfer functions. Some of the controller gains obtained using root locus analysis give good performance in steady state but failed to provide acceptable network disturbance performance.

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International Journal & Magazine of Engineering, Technology, Management and Research
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Therefore, the simulation final gains used are adjusted in the time domain to provide satisfactory performance over a wide operating range, including ac and dc side faults. Fig. 2 summarizes the control layers of the hybrid multilevel VSC. Current Controller Design: The differential equations describing the ac-side transient and steady-state are

$$\frac{di_d}{dt}=\frac{R}{L}i_d+\frac{R}{L}(V_{cd}-V_d+wLi_q) \quad (1)$$

$$\frac{di_q}{dt}=\frac{R}{L}i_q+\frac{R}{L}(V_{cq}-V_q+wLi_d) \quad (2)$$

Assume

$$\lambda_d = V_{cd}-V_d+wLi_q \text{ and } \lambda_q = V_{cq}-V_q+wLi_d$$

$$\frac{di_d}{dt}=-\frac{R}{L}i_d+\frac{R}{L}\lambda_d \quad (3)$$

$$\frac{di_q}{dt}=\frac{R}{L}i_q+\frac{R}{L}\lambda_q \quad (4)$$

The new control variables λ_d and λ_q can be obtained from two proportion-integral controllers (PI) having the same gains:

$$\lambda_d=K_d(i_d^*-i_d)+K_i\int(i_d^*-i_d)dt \quad (5)$$

$$\lambda_q=K_q(i_q^*-i_q)+K_i\int(i_q^*-i_q)dt \quad (6)$$

Where $i_d^* and\ i_q^*$ represent reference direct and quadrature current components. To facilitate control design in state space, the integral parts of $\lambda_d and\ \lambda_q$ are replaced by $W_d = K_i\int(i_d^*-i_d)dt$ and $W_q = K_i\int(i_q^*-i_q)dt$ rearranged in the following form:

$$\lambda_d=K_p(i_d^*-i_d)+W_d \quad (7)$$

$$\lambda_q=K_p(i_q^*-i_q)+W_q \quad (8)$$

The integral parts, in differential equations form, are

$$\frac{dW_d}{dt}=-K_ii_d+K_ii_d^* \quad (9)$$

$$\frac{dW_q}{dt}=-K_ii_q+K_ii_q^* \quad (10)$$

After substitution of (7) and (8) into (3) and (4), two identical and independent sets of equations, suitable for control design, are obtained as

$$\begin{bmatrix}\frac{di_d}{dt}\\ \frac{dW_d}{dt}\end{bmatrix}=\begin{bmatrix}-\frac{(R+K_p)}{L} & \frac{1}{L}\\ -K_i & 0\end{bmatrix}\begin{bmatrix}i_d\\ W_d\end{bmatrix}+\begin{bmatrix}\frac{K_p}{L}\\ K_i\end{bmatrix}i_d^* \quad (11)$$

$$\begin{bmatrix}\frac{di_q}{dt}\\ \frac{dW_q}{dt}\end{bmatrix}=\begin{bmatrix}-\frac{(R+K_p)}{L} & \frac{1}{L}\\ -K_i & 0\end{bmatrix}\begin{bmatrix}i_q\\ W_q\end{bmatrix}+\begin{bmatrix}\frac{K_p}{L}\\ K_i\end{bmatrix}i_q^*. \quad (12)$$

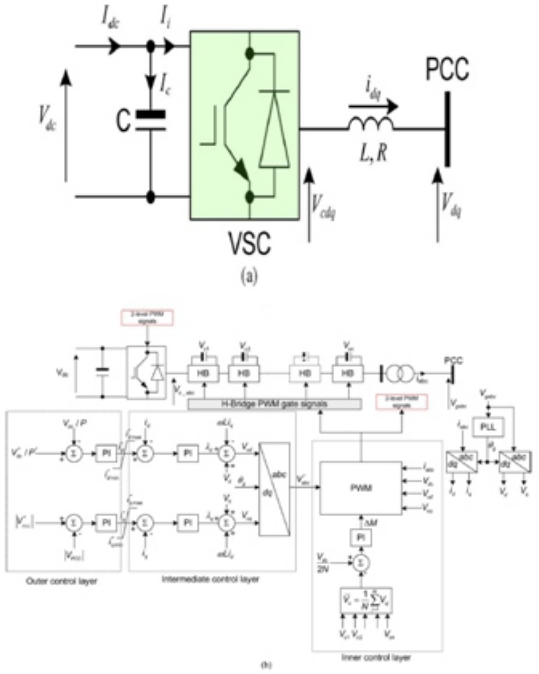

Fig. 2. (a) Representation of VSC station and (b) schematic diagram summarizing the control layer of the hybrid multilevel converter with ac side cascaded H-bridge cellsAfter Laplace manipulations of the state-space equations in (11) and (12), one transfer function is obtained forid and iq , which is used for the current controller design.

$$\frac{i_d(s)}{i_d^*(s)}=\frac{i_q(s)}{i_q^*(s)}=\frac{\frac{K_p}{L}s+\frac{K_i}{L}}{s^2+\frac{(R+K_p)}{L}s+\frac{K_i}{L}}$$

Equations relating the reference voltages to the modulator V_{cd}^* and V_{cq}^* , current controller output, and feedforward terms can be obtained from expressions for $\lambda_d and\ \lambda_q$ as follows:

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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$$V_{cd}^* = \lambda_d + V_d - wLi_q \quad (13)$$

$$V_{cq}^* = \lambda_q + V_q - wLi_q \quad (14)$$

Based on (5), (6), (13), and (14), the structure of the current controller shown in Fig. 2(b) (intermediate layer) is obtained. DC Voltage Controller: Based on Fig. 2, the differential equation describing the converter dc-side dynamics is

$$C\frac{dV_{dc}}{dt} = I_{dc} - I_i \quad (15)$$

Assuming a lossless VSC, dc power at the converter dc link must equal the ac power at converter terminal $I_i = (V_{dc} i_d + V_{cq} i_q)/V_{dc}$. Therefore, (15) can be written as

$$C\frac{dV_{dc}}{dt} = I_{dc} - \frac{(V_{dc} i_d + V_{cq} i_q)}{V_{dc}} \quad (16)$$

Equation (16) can be linearized using a Taylor series with the higher order terms neglected. Therefore, the linearized form of (16) is

$$\frac{d\Delta V_{dc}}{dt} = \frac{\Delta I_{dc}}{C} - \frac{V_{cd}}{CV_{dc}}\Delta i_d - \frac{V_{cq}}{CV_{dc}}\Delta i_q - \frac{i_d}{CV_{dc}}\Delta V_{cd} - \frac{i_q}{CV_{dc}}\Delta V_{cq} + \frac{(V_{cd} i_d + V_{cq} i_q)}{CV_{dc}^2}\Delta V_{dc} \quad (17)$$

Let $P_{ac} = V_{cd} i_d + V_{cq} i_q$ and

$$\Delta u_{dc} = \Delta I_{dc} - \left(V_{cd}/V_{dc}\right)\Delta i_d - \left(V_{cq}/V_{dc}\right)\Delta i_q - \left(i_d/V_{dc}\right)\Delta V_{cd} - \left(i_q/V_{dc}\right)\Delta V_{cq}$$

and the variable can be obtained from the DC voltage controller based on the PI control as follows:

$$\Delta u_{dc} = k_{pdc}(\Delta V_{dc}^* - \Delta V_{dc}) + k_{idc}\int (\Delta V_{dc}^* - \Delta V_{dc})\, dt. \quad (18)$$

Equation (17) can be reduced to

$$\frac{d\Delta V_{dc}}{dt} = \frac{\Delta u_{dc}}{C} + \frac{P_{ac}}{CV_{dc}^2}\Delta V_{dc} \quad (19)$$

Where V_{dc}^* represents reference dc link voltage. Let the new control variable introduced for the integral part of the dc voltage controller be , Δz_{dc} therefore:

$$\frac{d\Delta V_{dc}}{dt} = -\frac{1}{C}\left(K_{pdc} - \frac{p_{ac}}{V_{dc}^2}\right)\Delta V_{dc} + \frac{1}{C}\Delta z_{dc} + \frac{\Delta V_{dc}^*}{c} \quad (20)$$

$$\frac{d\Delta z_{dc}}{dt} = K_{idc}(\Delta V_{dc}^* - \Delta V_{dc}) \quad (21)$$

The state equations in (20) and (21) in matrix form are:

$$\frac{d}{dt}\begin{bmatrix}\Delta V_{dc} \\ \Delta z_{dc}\end{bmatrix} = \begin{bmatrix}\frac{K_{pdc}}{C} - \frac{P_{oc}}{CV_{dc}^2} & \frac{1}{C} \\ -K_{idc} & 0\end{bmatrix}\begin{bmatrix}\Delta V_{dc} \\ \Delta z_{dc}\end{bmatrix} + \begin{bmatrix}\frac{k_{pdc}}{c} \\ k_{idc}\end{bmatrix}\Delta V_{dc}^* \quad (22)$$

Equation (22) in the s-domain is

$$\begin{bmatrix}\Delta V_{dc}(s) \\ \Delta z_{dc}(s)\end{bmatrix} = \frac{1}{\square}\begin{bmatrix} s & \frac{1}{c} \\ -K_{ide} & s + \left(\frac{K_{pdc}}{c} - \frac{P_{oc}}{cV_{dc}^2}\right)\end{bmatrix}\begin{bmatrix}\frac{K_{pdc}}{c} \\ K_{idc}\end{bmatrix}\Delta V_{dc}^* \quad (23)$$

where

From (24), the transfer function for the dc voltage controller

$$\frac{V_{dc}(s)}{V_{dc}^*(s)} = \frac{\frac{K_{pdc}}{C}S + \frac{K_{idc}}{C}}{S^2 + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{Cv_{dc}^2}\right)8 + \frac{k_{idc}}{C}} \quad (24)$$

Normally, the voltage angle at the converter terminal relative to the PCC is sufficiently small, resulting in $V_{cq} \approx 0$ and $\Delta V_{cq} \approx 0$ Therefore, the reference current i_d^* for the current controller can be obtained from the outer dc voltage controller as follows:

$$\Delta i_d^* = -\frac{1}{\bar{v}_{cd}}(\Delta u_{dc} + i_d \Delta\bar{v}_{cd} - \Delta I_{dc}) \quad (25)$$

where $\bar{v}_{cd}$ and $\Delta\bar{v}_{cd}$ are normalized by V_{dc}^*. Active Power Controller: The active power controller sets the reference active current component i_d^* assuming a constant voltage at the PCC as follows:

$$i_d^* = K_{pp}(P^* - V_d^* i_d) + K_{Ip}\int (P^* - V_d^*) \quad (26)$$

Assume the voltage vector at the PCC is aligned with the d-axis and its magnitude is regulated at

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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V_d^* as V_q^*=0,and p^* represents active power reference. After replacing the integral part with a new control variablez_p, the following sets of equations result:

$$i_d^* = K_{pp}(P^* - V_d^* i_d) + z_p \quad (27)$$

$$\frac{dz_p}{dt} = K_{ip}(P^* - V_d^* i_d) \quad (28)$$

After substituting (28) into (11), the following state space representation for the power controller is obtain

$$\begin{bmatrix}\frac{di_d}{dt}\\ \frac{dz_d}{dt}\\ \frac{dz_p}{dt}\end{bmatrix} = \begin{bmatrix}-\frac{(R+K_p+k_pk_{pp}v_d^*)}{L} & \frac{1}{L} & \frac{k_p}{L}\\ -(k_i+k_ik_{pp}v_d^*) & 0 & k_i\\ -k_{ip}v_d^* & 0 & 0\end{bmatrix}\begin{bmatrix}i_d\\ z_d\\ z_p\end{bmatrix} + \begin{bmatrix}\frac{k_pk_{pp}}{L}\\ k_ik_{pp}\\ k_{ip}\end{bmatrix}P^* \quad (29)$$

where we have (29), shown at the bottom of the page. AC Voltage Controller: The reference reactive power current component is set by the ac voltage controller as

$$i_q^* = k_{pv}(|V_{ac}^*| - |V_{ac}|) + K_{iv}\int (|V_{ac}^*| - |V_{ac}|)\,dt \quad (30)$$

Where $|V_{ac}^*|$ represents reference voltage magnitude at PCC However, the gains for the ac voltage controllers are obtained using a trialoand-error search method that automatically runs the overall system simulation several

Table-1: Converter Transformer Parameters:

Transformers 1 and 2	
Power rating	687MA
Voltage ratio	330KV/400KV
Per unit impedance	(0.0008+j0.32)

Table-II:Converter Stations Parameters

Converters 1and 2	
Power ratings	687MVA
Maximum active power capability	600Mw
Maximum reactive power capability	335mvar
Two-level do link voltage	600kv
H-bridge do link voltage	42,86kv
H-bridge cell capacitance	150μf
H- bridge frequency	1khz
Converter 1 controller	
Current controller : KP	35
Current controller : Ki	3000
Power controller : kpp	0.0015
Power controller : ki	20
Ac voltage controller :kpv	30
Ac voltage controller : kiv	500
Converter 2 controller	
Current controller : kp	38
Current controller : ki	2000
Dc voltage controller : kbdc	0.015
Dc voltage controller : kidc	0.0573
AC voltage controller : kpv	0.00015
Ac voltage controller : kiv	400

Table-III: Transmission System Parameters

Lines parameters(based on lumped model)	
ac line length	60Km
ac line series impedance	(0.0127+j0.2933)Ω/Km
ac line shunt capacitance	12.74NF/Km
dc transmission distance	75km
dc line series resistance	13.9mΩ/Km
	0.159mH/Km
	0.231μF/Km

gains for all of the controllers and test network parameters used in this paper are listed in Tables I–III.

IV. PERFORMANCE EVALUATION:

The viability of the VSC-HVDC system that uses a hybrid multilevel VSC with ac-side cascaded H-bridge cells is investigated here, with emphasis on its dynamic performance during network alterations.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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In the steady state, the test network in Fig. 3(a) is used to assess its power control and voltage support capabilities. To further illustrate the advantages of the hybrid multilevel converter during ac and dc network disturbances, the same test network is subjected to a three-phase ac-side fault and a pole-to-pole dc-side fault at locations depicted in Fig. 3(a), both for a 140-ms duration. Converter stations 1 and 2 in Fig. 3(a) are represented by detailed hybrid VSC models with seven cells per phase, with the controllers in Fig. 2(b) incorporated.Seven cells per arm are used in this paper in order to achieve acceptable simulation times without compromising result accuracy, as each system component is represented in detailed. Also, the hybrid converter with seven H-bridge cells per phase generates 29 voltage levels per phase, which is the same as the two-switch modular multilevel converter with 28 cells per arm, for the same dc link voltage such that devices in both converters experience the same voltage stresses. The converters are configured to regulate active power exchange and dc link voltage, and ac voltage magnitudes PCC1 at and PCC 2respectively. The test system in Fig. 3(a) is simulated in the MATLAB Simulink environment.

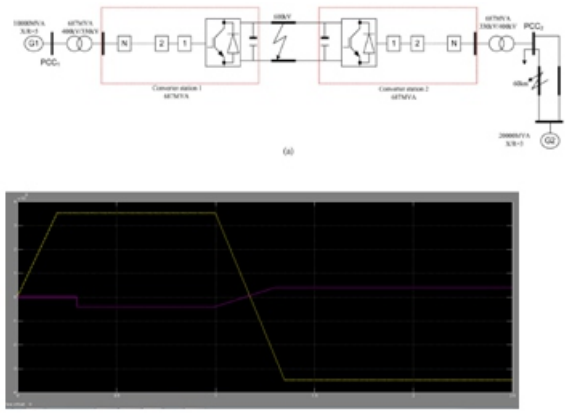
A.Four-Quadrant Operation and Voltage Support:

To demonstrate fouroquadrant operation and voltage support capability of the presented VSC-HVDC system, converter station 1 is commanded to increase its output power export from grid G1 to G2 from 0 to 0.5 pu (343.5 MW) at 2.5 pu/s. At time t=1 s it is commanded to reverse the active power flow in order to import 343.5 MW from grid G2 , at 2.5 pu/s. At t=2 a load of120+j90 MVA is introduced to PCC2 , illustrating the voltage support capability of converter station 2 during network alteration.Fig. 3(b) and (c) how converters 1 and 2 active and reactive power exchange with PCC1and PCC2 respectively. The converters are able to adjust their reactive power exchange with PCC1and PCC2 in order to support the voltage during the entire operating period. Fig. 3(c) and (d) show that converter 2 adjusts its reactive power exchange with PCC2 when the load is introduced at t= 2 s to support the voltage magnitude. Fig. 3(e) and (f) show that converter 2 injects and presents high-quality current and voltage waveforms into PCC2 with no ac filters installed).

Fig. 3(g) demonstrates that the voltage stresses across the H-bridge cell capacitors of converter 1 are controlled to the desired set point during the entire period. Fig. 3(h) displays the total dc link voltage across converter 2, which regulates the dc link voltage. Based on these results, the proposed VSC-HVDC system is able to meet basic steady-state requirements, such as provision of voltage support and four quadrant operation without compromising the voltage and current stresses on the converters switches.

B. AC Network Faults:

To demonstrate the ac fault ride-through capability of the presented HVDC system, the test network is subjected to a 140 ms three-phase fault to ground at the location shown in Fig. 3(a). During the fault period the power command to converter 1 is reduced in proportion to the reduction in the ac voltage magnitude (this is achieved by sensing PCC2 voltage). This is to minimize the two-level converter dc link voltage rise because of the trapped energy in the dc side, since power cannot be transferred as the voltage at PCC2 collapses. Fig. 4 displays the results when the test network exports 0.5 pu (343.5 MW) from gridG1 toG2 and is subjected to the three-phase fault at t=1. Fig. 4(a) shows the active and reactive powers converter 1 exchanges withPCC1 . Note that converter 1 matches its active power export to G2 in order to minimize the rise of converter 2 dc link voltage as its ability to inject active power into grid G2 reduces with the voltage collapse at PCC2 , as shown in Fig. 4(d) and stated above. Fig. 4(b) shows the active and reactive powers that converter 2 injects into PCC2 . The system is able to recover as soon as the fault is cleared, and converter



A: Test network used to illustrate the viability

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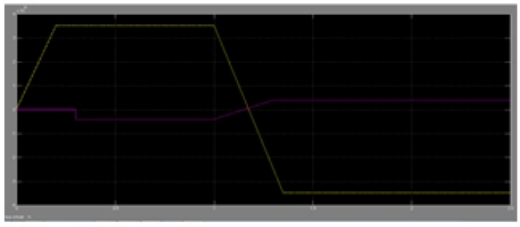
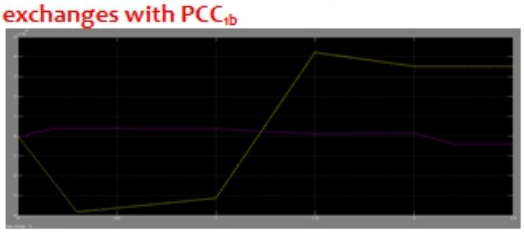
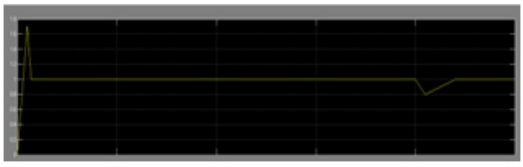


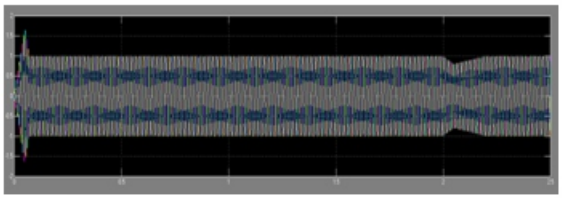
B: active and reactive power converter station 1 exchanges with PCC_{1b}



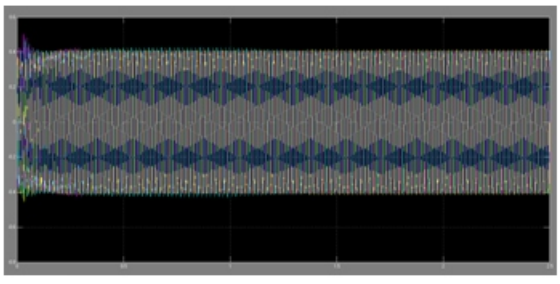
C: active and reactive power converter station 2 exchanges with PCC_2



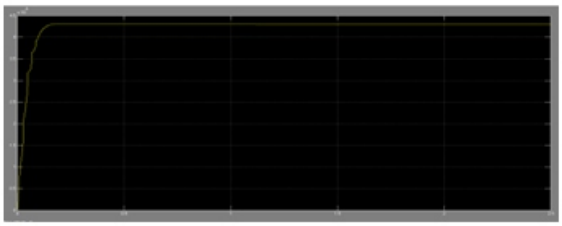
D: active and reactive power converter station 2 exchanges with PCC_2



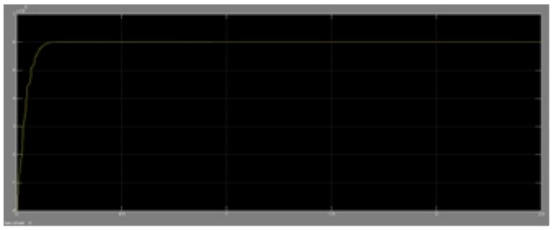
E: voltage waveforms at PCC_2



F: current waveforms converter station 1 exchanges with PCC_1



G: voltage across 21 cell capacitors of the three phases of converter 1



H: voltage across the dc link of converter station 2.

Fig. 3. Test network and waveforms demonstrating the steady-state operation of HVDC system based on hybrid voltage source multilevel converter with ac side cascaded H-bridge cells. (a) Test network used to illustrate the viability of the hybrid multilevel voltage source converter HVDC systems; (b) active and reactive power converter station 1 exchanges with PCC1 ; (c) active and reactive power converter station 2 exchanges with PCC2; (d) voltage magnitude at PCC2 ; (e) voltage waveforms at PCC2 ; (f) current waveforms converter station 1 exchanges with PCC1 ; (g) voltage across 21 cell capacitors of the three phases of converter 1; (h) voltage across the dc link of converter station 2.

2 adjusts its reactive power exchange with grid G2 in order support voltage at PCC2 [see Fig. 4(d)]. The transients shown of active and reactive powers at PCC2 are related to the reaction of the ac voltage controller that regulates the ac voltage at PCC2. Fig. 4(c) shows that the voltage magnitude at PCC1 remains unaffected; confirming that the hybrid voltage source

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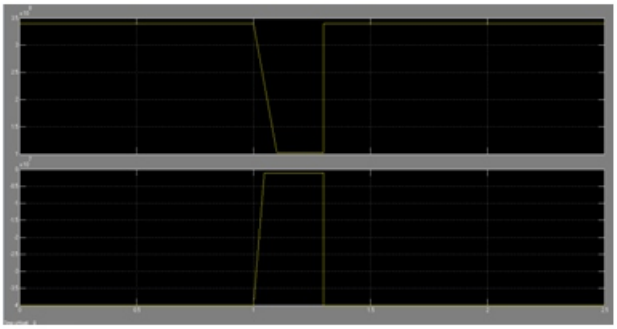
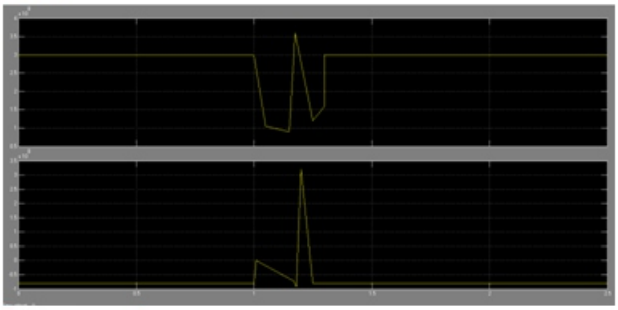
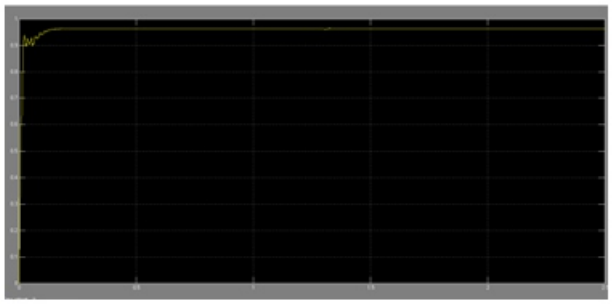


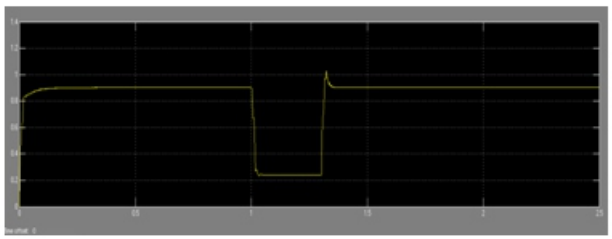
A: Active and reactive power converter 1 exchanges with PCC_1.



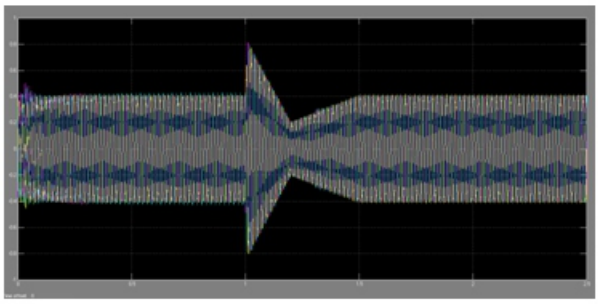
B: Active and reactive power converter 2 injects into PCC_2.



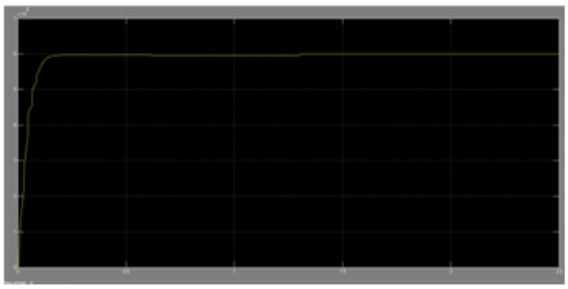
C: Voltage magnitude at PCC_1.



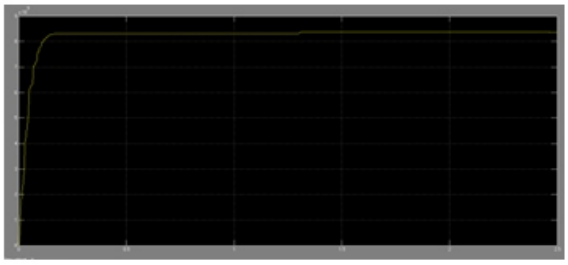
D: Voltage magnitude at. PCC_2



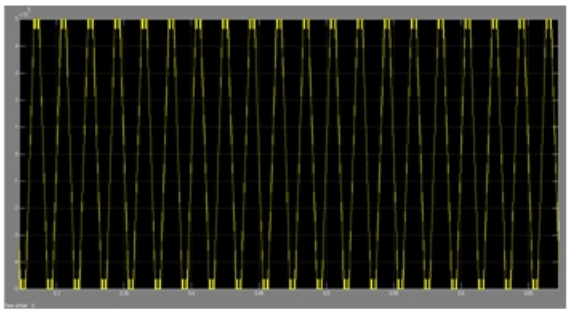
E: waveforms converter 2 injects into PCC_2.



F: Converter 2 dc link voltage



G: Voltage across 21 H-bridge cells of the converter 2



H: Line-to-line voltage waveform at the terminal of converter 1

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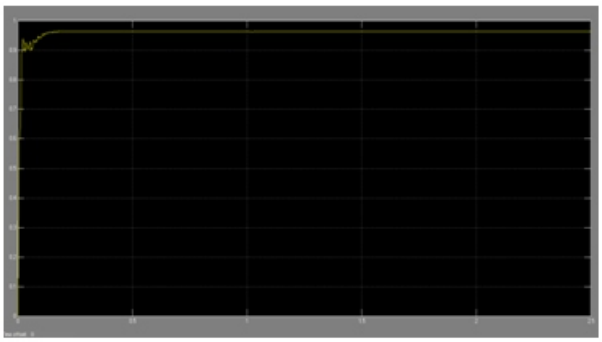
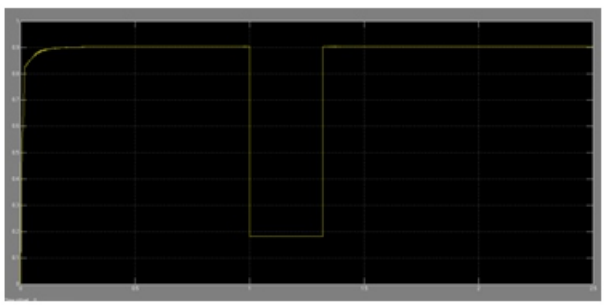
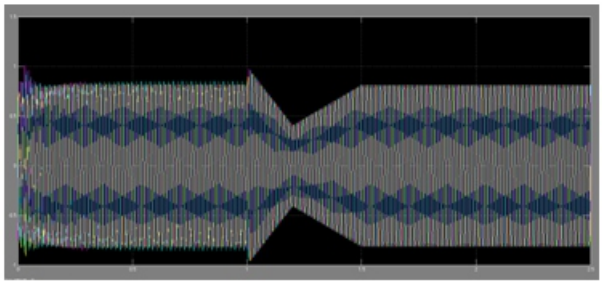
Fig. 4. Waveforms demonstrating ac fault ride-through capability of HVDC transmission systems based on hybrid voltage multilevel converter with ac side cascaded H-bridge cells. (a) Active and reactive power converter 1 exchanges with PCC1. (b) Active and reactive power converter 2 injects into PCC2. (c) Voltage magnitude at PCC1. (d) Voltage magnitude at . PCC2 (e) Current waveforms converter 2 injects into PCC2 . (f) Converter 2 dc link voltage. (g) Voltage across 21 H-bridge cells of the converter 2. (h) Line-to-line voltage waveform at the terminal of converter 1 (before transformer). (i) Active and reactive power at PCC1. (j) Active and reactive power at PCC2. Results in (i)–(o) demonstrate the case when the converter stations operate close to their maximum active power capabilities (power command at converter 1 is set to 0.75 pu, which is 515 MW) and system is subjected to a three-phase fault with a 300-ms duration.multilevel converter does not compromise the HVDC transmission system's decoupling feature despite adopting active power matching at converter 1, as explained. Fig. 4(e) shows that converter 2 restrains its contribution to the fault current to less than full load current despite the voltage at PCC2 collapsing to 20% of its rated voltage, due to converter 2's current controller. Fig. 4(f) shows that coordination of the HVDC controllers, as illustrated, minimizes the impact of ac-side faults on the transient



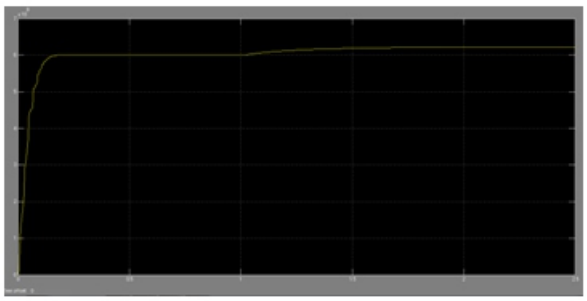
K: Voltage magnitude at PCC1



L: Voltage Magnitude at PCC2.



M: Current Waveforms Converter 2 Injects Into PCC2.



N: Converter 2 Dc Link Voltage.

Fig. 4. (Continued.) Waveforms demonstrating ac fault ride-through capability of HVDC transmission systems based on hybrid voltage multilevel converter with ac side cascaded H-bridge cells. (k) Voltage magnitude at PCC1. (l) Voltage magnitude at PCC2. (m) Current waveforms converter 2 injects into PCC2. (n) Converter 2 dc link voltage. (o) Voltage across the 21 H-bridge cell capacitors of converter 2. Results in (i)–(o) demonstrate the case when the converter stations operate close to their maximum active power capabilities (power command at converter 1 is set to 0.75 pu, which is 515 MW) and system is subjected to a three-phase fault with a 300-ms duration.

power flow on the dc side, hence minimizing disturbance on the dc link voltage. Fig. 4(g) shows that the H-bridge cell voltage stresses are controlled as the system rides through the ac-side fault. This confirms that the complexity of a HVDC system based on the hybrid multilevel VSC does not compromise its ac fault ride-through capability. Fig. 4(h) shows the hybrid multilevel VSC presents high-quality voltage to the converter transformer, with low harmonic content and DU/DT . This may permit elimination of ac-side filters and the use of standard insulation ac transmission transformers.

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The results in Fig. 4(i)–(o) are presented to demonstrate the ability of the proposed HVDC system to operate in faulty networks, independent of its operating point and fault duration. This case demonstrates the superiority of current-limiting VSCs over a synchronous generator during ac network disturbances. (Converter 2 current injectionPCC2 into is always controlled and less than full load rated current despite the fault duration and the amount of power exchange between ac networks G1and G2.)

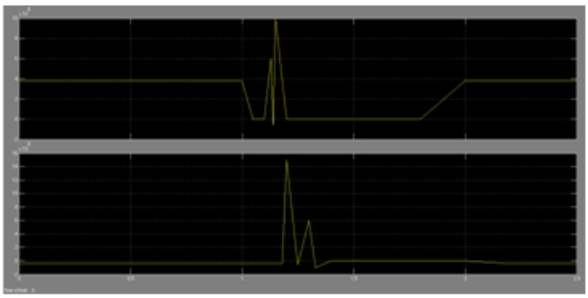
B.DC Network Faults :

The inherent current-limiting capability of the hybrid multilevel VSC with ac-side cascaded H-bridge cells that permits the VSC-HVDC system to ride-through dc-side faults will be demonstrated here. The test network is subjected to a 140 ms solid pole-to-pole dc-side fault at the location indicated in Fig. 3(a).

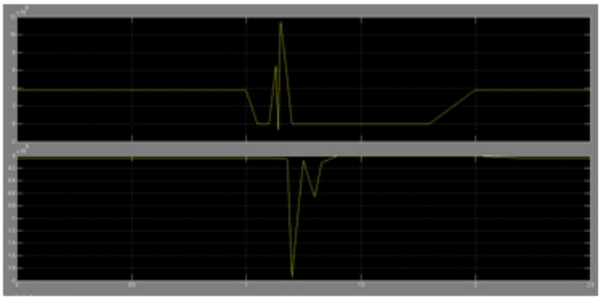
During the dc-side fault period, active power exchange between the two grids G1and G2 is reduced to zero. This facilitates uninterruptable system recovery from the temporary dc fault with minimal inrush current, since the power paths between the converter's ac and dc sides are blocked (by inhibiting all converter gate signals) to eliminate a grid contribution to the dc fault.

Fig. 5 shows the results when the test network is subjected to a temporary solid pole-to-pole dc fault at the middle of the dc Link. Fig. 5(a) and (b) shows the active and reactive powers that converter stations 1 and 2 exchange with PCC1 and PCC2 .Observe zero active and reactive power exchange between the converter stations and ac grids G1 and G2 during the fault period, hence there is no current flow in the switches of converters 1 and 2. However, a large surge in active and reactive power is observed when the gating signals to converters 1 and 2 are restored after the fault is cleared,

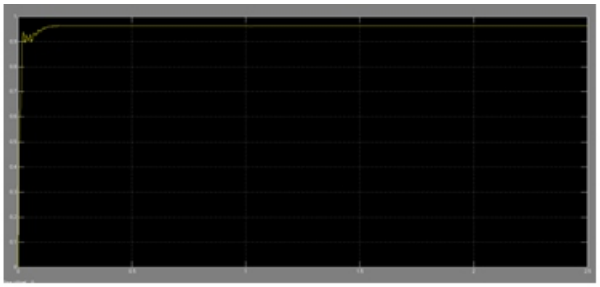
in order to restart the system. Fig. 5(c) and (d) shows that the current surge experienced by both converter stations causes noticeable voltage dipping at PCC1 and PCC2 due to increased consumption of reactive power during system start-up and dc link voltage build-up following fault clearance. The surge in active and reactive powers in both converter stations occurs as the dc side capacitors try t O



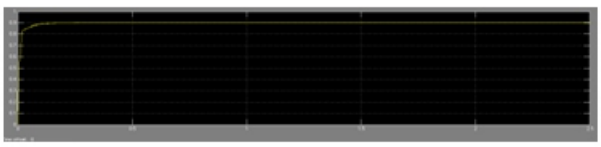
A: Active and reactive power converter 1 exchanges with PCC



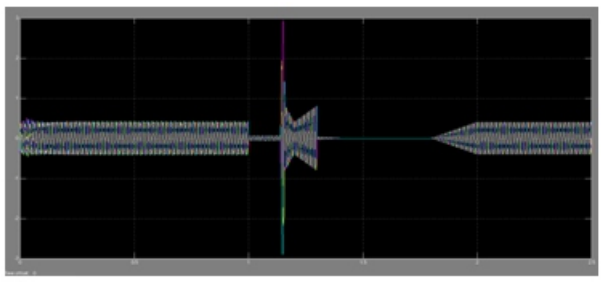
B: Active and reactive power converter 2 exchanges with PCC_2



C: Voltage magnitude at PCC_1 . (d) Voltage magnitude at PCC_2



D: Voltage magnitude at PCC_2



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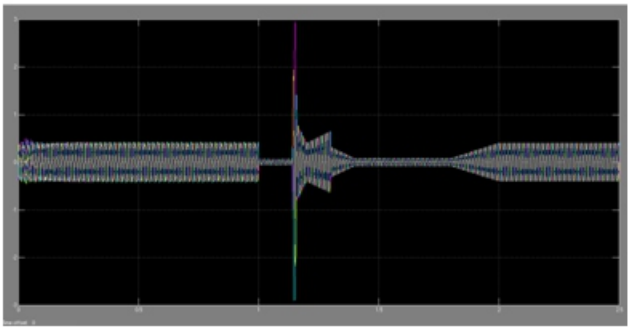
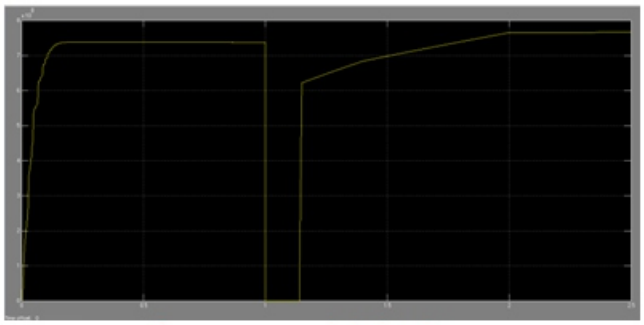
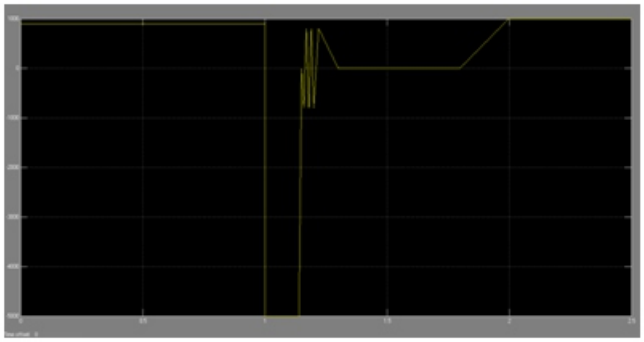
E: Current waveforms converter 1 exchange with grid G1 at PCC_1



F: Current waveforms converter 2 exchange with grid G2 at PCC_2



G: Converter 2 dc link voltage



H: Zoomed version of dc link current demonstrating

Fig. 5. Waveforms demonstrating dc fault ride-through capability of HVDC transmission systems based on hybrid voltage multilevel converter with ac side cascaded H-bridge cells. (a) Active and reactive power converter 1 exchanges with PCC1. (b) Active and reactive power converter 2 exchanges with PCC2 (c) Voltage magnitude at PCC1 . (d) Voltage magnitude at PCC2. (e) Current waveforms converter 1 exchange with grid G1 at PCC1 . (f) Current waveforms converter 2 exchange with grid G2 at PCC2. (g) Converter 2 dc link voltage. (h) Zoomed version of dc link current demonstrating the benefits of dc fault reverse blocking capability.

charge from both ac sides; this causes a large current flow from both ac sides to the dc side to charge the dc link capacitors and cable distributed capacitors as shown in Fig. 5(e) and 5(f). The results in Fig. 5(e) and 5(f) also demonstrate the benefits of dc fault reverse blocking capability inherent in this hybrid system, as the converter switches experience high current stresses only during dc link voltage build-up. Fig. 5(g) shows that converter 2 dc link voltage recovers to the pre-fault state after the fault.

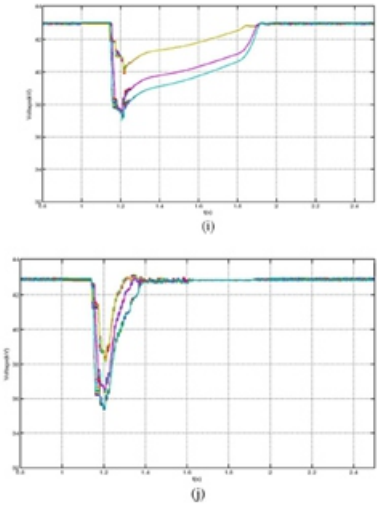


Fig. 5. (Continued.) Waveforms demonstrating dc fault ride-through capability of HVDC transmission systems based on hybrid voltage multilevel converter with ac side cascaded H-bridge cells. (i) Voltage across the H-bridge cell capacitors of converter 1. (j) Voltage across the H-bridge cell capacitors of converter 2.is cleared. Notice the recovery period for the dc link voltage is relatively long; this is the major disadvantage of the proposed HVDC systems as it uses a common dc link capacitor. Fig. 5(h) expands the dc fault current and shows the 60-kA peak decays to zero in less than four cycles (for 50 Hz) after discharge of dc link and cable distributed capacitors.

This result confirms the possibility of eliminating dc circuit breakers to isolate permanent dc side faults in dc networks that use HVDC converters with current limiting capability.Fig. 5(h) also shows the ac grids start to contribute to the dc link current after the fault is cleared, to charge the dc side capacitors. Fig. 5(i) and (j) shows the voltage across the 21 H-bridge cells of the converter stations 1 and 2 (each group of traces represent voltages across 7 H-bridge cell capacitors in each phase).

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The voltage across the H-bridge cell capacitors remains unaffected during the entire fault period as the converters are blocked. The cell capacitors start to contribute energy to the main dc link capacitors during dc link voltage build-up after restoration of the converter gating signals. This contribution creates a noticeable reduction in the cell capacitor voltages during system restart. The cell capacitors of converter 2 that regulate dc link voltage, experience a larger voltage dip than converter 1, which regulates active power. However, the reduction in H-bridge cell capacitor voltages is minimized if large capacitance is used.

V. CONCLUSION:

This paper presented a new generation VSC-HVDC transmission system based on a hybrid multilevel converter with ac-side cascaded H-bridge cells. The main advantages of the proposed HVDC system are:

• potential small footprint and lower semiconductor losses compared to present HVDC systems.

• low filtering requirements on the ac sides and presents high-quality voltage to the converter transformer.

• does not compromise the advantages of VSC-HVDC systems such as four-quadrant operation; voltage support capability; and black-start capability, which is vital for connection of weak ac networks with no generation and wind farms.

• modular design and converter faultmanagement (inclusion of redundant cells in each phase may allow the system to operate normally during failure of a few H-bridge cells; whence a cell bypass mechanism is required).

• resilient to ac side faults (symmetrical and asymmetrical).

• inherent dc fault reverse blocking capability that allows converter stations to block the power paths between the ac and dc sides during dc side faults (active power between ac and dc sides, and reactive power exchange between a converter station and ac networks), hence eliminating any grid contribution to the dc fault current.

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