Implementation of UART with BIST Technique for High Fault Coverage

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Abstract:

Testing of VLSI chips are becoming very much complex day by day due to increasing exponential advancement of nano technology. Asynchronous serial communication is usually implemented by Universal Asynchronous Receiver Transmitter (UART), mostly used for short distance, low speed, low cost data exchange between processor and peripherals. UART allows full duplex serial communication link, and is used in data communication and control system. BIST is a design technique that allows a system to test automatically itself with slightly larger system size. In this paper, the simulation result performance achieved by BIST enabled UART architecture the extra hardware needed in BIST architecture. This technique generate random test pattern automatically, so it can provide less test time compared to an externally applied test pattern and helps to achieve much more productivity at the end . This paper presents a novel test pattern generator which is more suitable for built in self test (BIST) structures used for testing of VLSI circuits. The objective of the BIST is to reduce power dissipation without affecting the fault coverage. The proposed test pattern generator reduces the switching activity among the test patterns at the most.

Keywords:

FPGA, BIST, LP-LFSR, Switching activity.

I.INTRODUCTION:

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly.

These applications require low power dissipation for VLSI circuits [1]. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC. Hardware components in a SOC may include one or more processors, memories and dedicated components for accelerating critical tasks and interfaces to various peripherals. One of the approaches for SOC design is the platform based approach. Power dissipation is a challenging problem for today's System-on-Chips (SOCs) design and test. In general, the power dissipation of a system in test mode is more than in normal mode [2]. Four reasons are blamed for power increase during test [3].Real time imaging processes require intensive scientific computations for Digital Signal Processing (DSP). Fast and efficient parallel multipliers are required for DSP, General Purpose Signal Processing(GPSP) and application specific architecture for DSP.DSP algorithm implementation demands using Application Specific Integrated Circuits (ASICs); costs for ASICs are high as well as algorithms should be verified and optimized before realization. The contemporary Field Programmable Gate Arrays (FPGAs) have emerged as a platform for efficient hardware implementation of such complex and computation intensive algorithms.

- High switching activity due to nature of test patterns
- Parallel activation of internal cores during test
- Power consumed by extra design-for-test(DFT) circuitry
- Low correlation among test vectors

This extra power consumption (average or peak) can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime.

Solutions that are commonly applied to alleviate the excessive power problem during test include reducing frequency and test partitioning/scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time. Built-In Self-Test (BIST) is a DFT methodology that aims at detecting faulty components in a system by incorporating the test logic on chip. BIST is well known for its numerous advantages such as at-speed testing and reduced need for expensive external automatic test equipment (ATE). In BIST, a linear feedback shift register (LFSR) generates pseudorandom test patterns for primary inputs (for a combinational circuit) or scan chain inputs (for a sequential circuit).

On the observation side, a multiple input signature register (MISR) compacts test responses received from primary outputs or scan chain outputs. Unfortunately,BIST-based structures are very vulnerable to high-power consumption during test. Test vectors, applied to a circuit under test at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The main reason is that the random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among adjacent bits within each pattern.

The rest of the paper is organized as follows. In section II, previous works relevant to power reduction are discussed, which mainly concentrated to reduce the average and peak power. In section III, an overview of power analysis for testing is presented. In section IV, Braun array multiplier is discussed briefly, which is taken here as a circuit under test (CUT) to verify the effectiveness of the proposed technique. In Section V, the proposed technique in the test pattern generator is discussed. Section VI describes the algorithm for the proposed LP-LFSR. In section VII, the implementation details and the results are presented. Section VIII summarizes the conclusion.

II. REVIEW OF PREVIOUS WORK:

Different techniques are available to reduce the switching activities of test pattern, which reduce the power in test mode. For linear feedback shift register (LFSR), Giard proposed a modified clock scheme in which only half of the D flip-flops works, thus only half of the test pattern can be switched [7].

S.K. Guptha proposed a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by original LFSR is rearranged to reduce the switch frequency. LT-TPG is proposed to reduce the average and peak power of a circuit during test [4]. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR). Modifying the LFSR by adding weights to tune the pseudorandom vectors for various probabilities decreases energy consumption and increases fault coverage [7], [8]. A low-power random pattern generation technique to reduce signal activities in the scan chain is proposed in [9]. In this technique, an LFSR generates equally probable random patterns. The technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power.

A better low power can be achieved by using single input change pattern generators. It is proposed that the combination of LFSR and scan shift register is used to generate random single input charge sequences [9 & 10]. In [10 &11], it is proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR, m is length of LFSR. In [5], it is proposed that 2m single input changing data is inserted between two neighboring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

III. ANALYSIS OF POWER FOR TESTING:

In CMOS technology, the power dissipation can be classified into static and dynamic. Static power dissipation is mainly due to the leakage current. Dynamic power dissipation is due to switching transient current and charging and discharging of load capacitances. Some significant parameters for evaluating the power consumption of CMOS circuits are discussed below.

$$E = V_{dd}^2 C_0 F_i S_i \qquad (1)$$

Where V_{dd} is the supply voltage, C_o is the load capacitance. The product of F_i and S_i is called weighted switching activity of internal circuit node i. The average power consumption of internal circuit node I can be given by,

$$P = V_{dd}^2 C_0 F_i S_i f \qquad (2)$$

f is the clock frequency .The summary of Pi of all the nodes is named as average power consumption. It can be observed from (1) and (2) that the energy and power consumption mainly depends on the switching activities, clock frequency and supply voltage. This paper reduces the switching activity at the inputs of the circuit under test (CUT) as low as possible.

A.BIST approach:

BIST is a design for testability (DFT) technique in which testing is carried out using built –in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.1 needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a
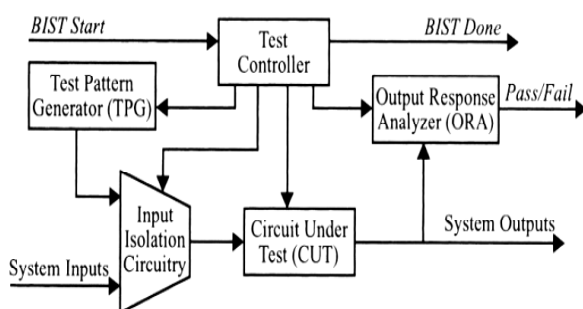
Figure 1. BIST Basic block diagram

counter or a linear feedback shift register (LFSR).A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer. A controller provides a control signal to activate all the blocks. BIST has some major drawbacks where architecture is based on the linear feedback shift register[LFSR].The circuit introduces more switching activities in the circuit under test (CUT)during test than that during normal operation[5].It causes excessive power dissipation and results in delay penalty into the design[6].

B.Classification of test strategies:

1. Weighted Pseudorandom: Testing: In weighted pseudorandom testing, pseudorandom patterns are applied with certain 0s and 1s distribution in order to handle the random pattern resistant fault undetectable by the pseudorandom testing. Thus, the test length can be effectively shortened.

2. Pseudo exhaustive Testing: Pseudo exhaustive testing divides the CUT into several smaller sub circuits and tests each of them exhaustively. All detectable flaws within the sub circuits can be detected. However, such a method involves extra design effort to partition the circuits and deliver the test patterns and test responses. BIST is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. BIST is the commonly used design technique for self testing of circuits.

3. Pseudorandom Testing: Pseudorandom testing involves the application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a deterministic order. The test length and the contents of the patterns are used to impart fault coverage.

4. Exhaustive Testing: Exhaustive testing involves the application of all possible input combinations to the circuit under test (CUT). It guarantees that all detectable faults that divert from the sequential behavior will be detected. The strategies are often applied to complex and well isolated small modules such as PLAs.

5.Stored Patterns: Stored-pattern approach tracks the pre generated test patterns to achieve certain test goals. It is used to enhance system level testing such as the power-on self test of a computer and microprocessor functional testing using micro programs.

IV.DESIGN OF UART:

In several control systems, UART a kind of serial communication circuit is used widely. A universal asynchronous receive/transmit (UART) is an integrated circuit which plays the most important role in serial communication. It handles the conversion between serial and parallel data. Serial communication reduces the distortion of a signal, therefore makes data transfer between two systems separated in great distance possible. To send data with the UART, the processor simply writes data to the transmitter address as if it was a memory space. The transmitter will take care of the entire transmission process. The transmitter performs parallel-to-serial conversions, and sends data on the serial line. The processor pushes data (5 to 8 bits wide) into the transmit FIFO, which is 128 bytes deep. When the transmit FIFO is full, no new data can be pushed into it.

The transmitter pops the data off the FIFO, and shifts it out at the baud rate. The Divisor Registers determine the baud rate.Using the Line Control Register, the user can configure the number of data bits (5, 6, 7, or 8) per frame, as well as the number of stop bits (1, 1.5, or 2) to be sent at the end of a frame. The transmitter also has a parity generation circuit that is capable of creating even, odd, sticks even, or sticks odd parity. When parity generation is disabled, no parity will be sent after the data bits. There is one interrupt associated with the transmitter it is a third-level priority interrupt that occurs when the transmit FIFO is empty.

Logically, the transmitter follows the steps below:

1. If there is data available in the FIFO, load a byte into the shift register.

2. Send a start bit on the serial line, indicating the beginning of a frame.

3. Shift out data bits from the shift register to the serial line.

4. If parity is enabled, send Parity Bit after all data bits are sent.

5. Send stop bit(s) on the serial line, indicating the end of a frame.

4.2.6 THE UART RECEIVER:

To receive data with the UART, the processor simply reads data from the receiver address as if it was a memory space. The receiver is responsible for capturing data from the serial line and validating data integrity.The receiver performs serial-to-parallel conversions, and pushes data into the receive FIFO at the baud rate. The processor can pop data from the 128-byte deep receive FIFO at the system clock frequency. The supplied RCLK should be 16 times faster than the baud rate.

The receiver monitors the serial line. When a valid start bit is detected, the receiver begins to shift data bits from the serial line, and saves the received data in the receive FIFO. Using the Line Control Register, the user can configure the number of data bits (5, 6, 7, or 8) per frame, as well as the type of parity to expect on the serial line.

The receiver has a parity generation circuit that is capable of creating even, odd, stick even, or stick odd parity as data is shifted in from the serial line. The calculated parity is then checked with the received parity to determine data integrity. When parity generation is disabled, no parity will be expected after the data bits. Besides parity errors, the receiver is also capable of detecting frame errors, overrun errors, and break errors. Frame errors occur when the receiver is expecting a stop bit but received a 'o' on the serial line. Overrun errors occur when they receive FIFO is full and the newly received data is destroyed because it cannot be saved in the FIFO. Break errors occur when the serial line is 'o' for more than a full frame.

Break errors, frame errors, and parity errors are associated with the particular pieces of data in the FIFO that contains the errors. In other words, these errors are revealed to the processor only when the data with error is at the top of the receive FIFO.LSR indicates if there are any errors in the entire receive FIFO. In addition to error detection capabilities, the receiver also feature false start bit detection and self-recovery from frame error. The serial line may be subject to noise, so it is essential that the receiver be able to differentiate noise from a valid start bit. In order for the receiver to recognize a 'o' on the serial line as a valid start bit, this 'o' value must remain for at least half a baud cycle from the falling edge of the serial input.

If the start bit does not remain stable in that period, it is disregarded and the receiver will return to its idle state. The asynchronous nature of a serial line means it is possible that the receiver is out of synch from the transmitter, resulting in a frame error. When a frame error occurs, the receiver will try to resynchronize itself to the transmitter. To achieve this self-recovery feature, the receiver assumes that the invalid stop bit is actually the start bit of the next frame, and will proceed to shift in data bits from the serial line. There are three interrupts associated with the receiver. The highest-level priority interrupt occurs when the received data has an error. A second-level priority interrupt occurs when they receive FIFO has reached its trigger level.

1. Hunt for a valid start bit, which indicates the beginning of a frame.

2. Shift in data bits from the serial line to the shift register.

3. If parity is enabled, compare received parity bit with the expected value.

V. IMPLEMENTATION AND RESULTS:

The proposed uart designed using Verilog hardware description language and structural form of coding. The proposed system simulation results are as follows:

VI. CONCLUSION:

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

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