ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

High-Frequency AC Power Distribution System with a Cascaded Multilevel Inverter Based on Switched-Capacitor.

M.Sandeep
MTech Student
Department of EEE
AnuBose Institute of Technology(ABIT)
Paloncha, Khammam, India.

K.Aravinda Swamy
Associate Professor
Department of EEE
AnuBose Institute of Technology(ABIT)
Paloncha, Khammam, India.

ABSTRACT:

The increase of transmission frequency reveals more merits than low- or medium-frequency distribution among different kinds of power applications. High-frequency inverter serves as source side in high-frequency ac (HFAC) power distribution system (PDS). However, it is complicated to obtain a high-frequency inverter with both simple circuit topology and straightforward modulation strategy. A novel switched-capacitor-based cascaded multilevel inverter is proposed in this paper, which is constructed by a switched-capacitor frontend and H-Bridge backend. Through the conversion of series and parallel connections, the switched capacitor Front end increases the number of voltage levels. The output harmonics and the component counter can be significantly reduced by the increasing number of voltage levels. A symmetrical triangular waveform modulation is proposed with a simple analog implementation and low modulation frequency comparing with traditional multicarrier modulation. The circuit topology, symmetrical modulation, operation cycles, Fourier analysis, parameter determination, and topology enhancement are examined. An experimental prototype with a rated output frequency of 25 kHz is implemented to compare with simulation results. The experimental results agreed very well with the simulation that confirms the feasibility of proposed multilevel inverter.

Index Terms—Cascaded H-Bridge, high-frequency ac (HFAC), multilevel inverter, switched capacitor (SC), symmetrical phase shift modulation (PSM).

INTRODUCTION:

High-Frequency ac (HFAC) power distribution system (PDS) potentially becomes an alternative to traditional dc distribution due to the fewer components and lower cost. The existing applications can be found in computer , telecom , electric vehicle , and renewable energy micro grid. However, HFACPDS has to confront the challenges from large power capacity, high electromagnetic interference (EMI), and severe power losses . A traditional HFAC PDS is made up of a high-frequency (HF) inverter, an HF transmission track, and numerous voltage-regulation modules (VRM). HF inverter accomplishes the power conversion to accommodate the requirement of point of load (POL). In order to increase the power capacity, the most popular method is to connect the inverter output in series or in parallel. However, it is impractical for HF inverter, because it is complicated to simultaneously synchronize both amplitude and phase with HF dynamics. Multilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power capacity is easy to be achieved by multilevel inverter with lower switch stress.

Existing System:

The proposed circuit is made up of the SC frontend and cascaded H-Bridge backend. If the numbers of voltage levels obtained by SC frontend and cascaded H-Bridge backend are $N1$ and $N2$, respectively, the number of voltage levels is $2 \times N1 \times N2+1$ in the entire operation cycle.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Circuit Topology

Fig. 1 shows the circuit topology of nine-level inverter (*N*1 =2, *N*2 = 2), where *S*1, *S*2, *S*_1 , *S*_2 as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of *C*1 and *C*2 . *S*1*a*, *S*1*b*, *S*1*c*, *S*1*d*, *S*2*a*, *S*2*b*, *S*2*c*, *S*2*d* are the switching devices of cascaded H-Bridge. *Vdc*1 and *Vdc*2 are input voltage. *D*1 and *D*2 are diodes to restrict the current direction. *I* out and *vo* are the output current and the output voltage, respectively.

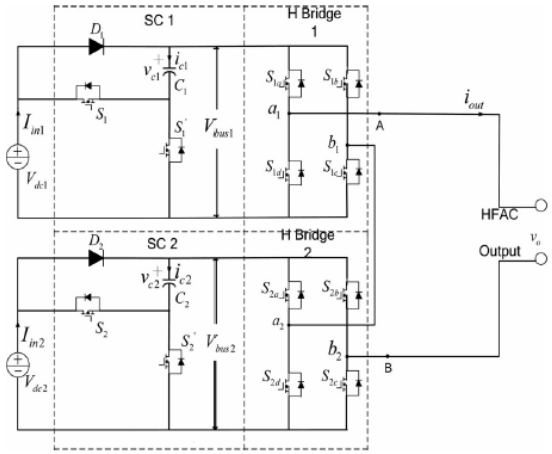

Fig. 1. Circuit topology of cascaded nine-level inverter ($N_1 = 2, N_2 = 2$).

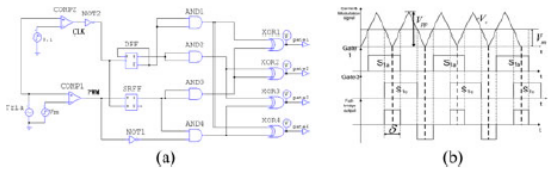

Fig. 2. Circuit and operational waveforms of symmetrical PSM. (a) Circuit of symmetrical PSM. (b) Operational waveforms of symmetrical PSM.

Proposed System:

The number of voltage levels can be further increased via two approaches. One is to increase the level number generated by SC circuit; the other one is to increase level number generated by cascaded H-Bridge. Thirteen-level inverters, as shown in Fig. 9, explain these two methods. A 3 × 2 structure, as shown in Fig. 9(a), is derived by the enhancement of SC circuit, which needs 6 diodes, 4 capacitors, 14 switches, and 2 dc inputs. 2×3 structure as shown in Fig. 9(b) is derived by the enhancement of H-Bridge circuit, which needs 3 diodes, 3 capacitors, 18 switches, and 3 dc inputs. It can be found that 3 × 2 structure requires more diodes and capacitors than 2 ×3 structure. However, the number of power switches in 3 × 2 structure is less than that in 2 × 3 structure. Because the traditional cascaded H-bridge needs 24 switches and 6 inputs to produce 13 voltage levels, the numbers of power switches and inputs are greatly decreased by proposed inverter. In order to accomplish the staircase output with 4*n* + 1 voltage levels, the component counts are compared in Table II.

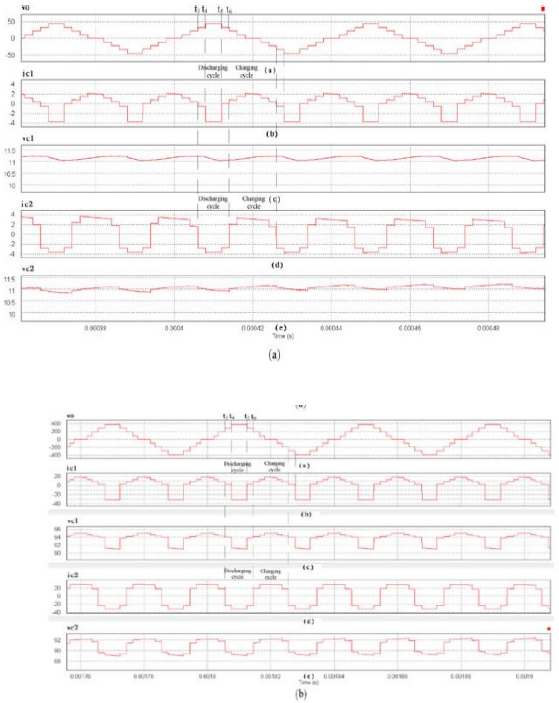

Fig. 10. Simulation waveforms of nine-level SC-based cascaded inverter, output frequency f_s = 25 kHz ($k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$, mode 1). (a) Low power at 50 W. (b) High power at 4 kW.

PERFORMANCE EVALUATION

A. Simulation Evaluation

The simulation based on PSIM is performed for the proposed inverter. The waveforms of output voltage *vo* , capacitor currents (*iC*1, *iC*2) and capacitor voltages (*vC*1, *vC*2) are shown in Fig. 10. The following parameters are used for low power simulation. The input voltage is *V*in = 12 V, the module 1 capacitor is *C*1 = 100 μF with 80 mΩ ESR, the module 2 capacitor is *C*2 = 220 μF with 50 mΩ ESR, the diodes *D*1 and *D*2 have 0.6 V forward voltage drop and 50 mΩ internal on-state resistance, and the load resistance is *Ro* = 12 Ω. The following parameters are used for

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

high-power simulation. The input voltage is *Vin* =100 V, the module 1 capacitor is *C*1 = 300 μF with 30 Mω ESR, the module 2 capacitor is *C*2 = 560 μF with 20 mΩ ESR, and the load resistance is *Ro* = 12 Ω. The output frequency *fs* is 25 kHz. The waveforms of low power and high power are demonstrated in Fig. 10(a) and (b), respectively. It can be seen that the proposed inverter can work at higher power. *C*1 and *C*2 can be converted to resonant switched-capacitor topology easily , and hence the less power loss can be achieved in the front end SC stage.

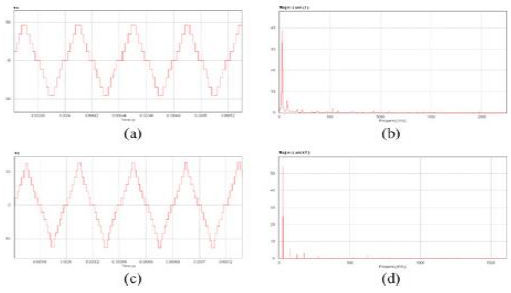

Fig. 11. Simulation waveforms of 9-level and 13-level inverter, output frequency $f_s = 25$ kHz. (a) Output voltage of nine-level inverter ($k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$). (b) Spectrum of nine-level output. (c) Output voltage of 13-level inverter (same duration of each voltage level). (d) Spectrum of 13-level output.

Experimental Evaluation

An experimental prototype was implemented with output frequency of 25 kHz and output power of 50 W. The schematic of modulation circuit is shown in Fig. 12 that is made up of DFF, RSFF, NOT, and XOR. LM393 is a dual comparator operated at single voltage mode. The LOCMOS logic components consisting of HEF4013 (dual D flip-flop), HEF4070 (Quad 2- input XOR), HEF4081 (Quad 2-inputANDgate), and HEF4069 (Hex Inverters) accomplish the symmetrical PSM. 5 V output in CMOS logic is magnified by boot-strap IC IR2113 to drive power switches. The schematic of power circuit is same as shown in Fig. 1. The switching devices are IRF540 MOSFETs with about 50 mΩ on-state resistances. Capacitor *C*1 is 100 μF electrolytic capacitor with ESR 80 mΩ, while *C*2 is 220 μF electrolytic capacitor with ESR 50 mΩ. *Vin* is 12 V supplied by dc power supply KIKUSUI PAS40-9. The switching frequency of H-bridge backend is 25 kHz, while the switching frequency of SC frontend is 50 kHz. *Ro* is 12 Ω resistive load.

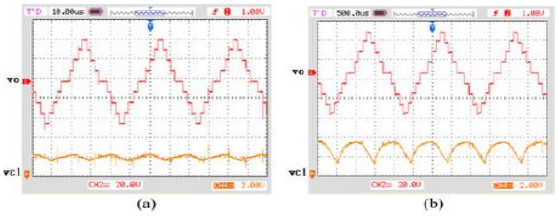

Fig. 15. Observed output and capacitor voltage at condition of $k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$, and 12 Ω load. (a) Output waveforms of 25 kHz frequency. Upper trace: output voltage v_o; lower trace: capacitor voltage v_{c1}. (b) Output waveforms of 500 Hz frequency. Upper trace: output voltage v_o; lower trace: capacitor voltage v_{c1}.

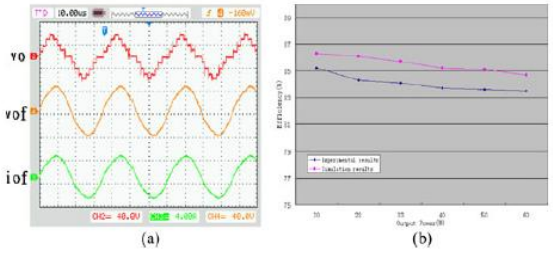

Fig. 16. Output waveforms after *LC* filter and conversion efficiency. (a) Upper trace: staircase output v_o; middle trace: output voltage after *LC* filter v_{of}; lower trace: output current after *LC* filter i_{of}. (b) Conversion efficiency comparisons of nine-level inverter with 25 kHz output under the condition of $k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$.

CONCLUSION

In this paper, a novel SC-based cascaded multilevel inverter was proposed. Both 9-level and 13-level circuit topology are examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The accordant results of simulation and experiment further confirm the feasibility of proposed circuit and modulation method. Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by SC frontend. For instance, the number of voltage levels increases twice in half cycle of 9-level circuit, and the number of voltage levels increases three times in half cycle of 13-level circuit. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology. Meanwhile, the magnitude control can be accomplished by pulse width regulation of voltage level, so the proposed multilevel inverter can serve as HF power source with controlled magnitude and fewer harmonics. This paper mainly analyzes nine-level and 13-level inverters.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

REFERENCES:

[1] P. Jain and H. Pinheiro, "Hybrid high frequency AC power distribution architecture for telecommunication systems," *IEEE Trans. Aerospace Electron. Syst.*, vol. 35, no. 1, pp. 138–147, Jan. 1999.

[2] J. Drobnik, "High frequency alternating current power distribution," in *Proc. 16th Int.Telecommun. Energy Conf., (INTELEC '94)*, Oct. 30–Nov. 3, pp. 292–296.

[3] B. K. Bose, M.-H. Kin, and M. D. Kankam, "High frequency AC vs. DC distribution system for next generation hybrid electric vehicle," in *Proc. IEEE Int. Conf. Ind. Electron., Control, Instrum. (IECON)*, Aug. 5–10, 1996, vol. 2, pp. 706–712.

[4] S. Chakraborty and M. G. Simoes, "Experimental evaluation of active filtering in a single-phase high-frequency AC microgrid," *IEEE Trans. Energy Convers.*, vol. 24, no. 3, pp. 673–682, Sep. 2009.

[5] R. Strzelecki and G. Benysek, *Power Electronics in Smart Electrical Energy Networks*. London, U.K.: Springer-Verlag, 2008.

[6] Z.Ye, P. K. Jain, and P. C. Sen, "A two-stage resonant inverter with control of the phase angle and magnitude of the output voltage," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2797–2812, Oct. 2007.

[7] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel PWM methods at low modulation indices," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 719–725, Jul. 2000.

[8] C. C. Antaloae, J. Marco, and N. D. Vaughan, "Feasibility of highfrequency alternating current power for motor auxiliary loads in vehicles," *IEEE Trans. Veh. Technol.*, vol. 60, no. 2, pp. 390–405, Feb. 2011.

[9] K. W. E. Cheng, "Computation of the AC resistance of multistranded conductor inductors with multilayers for high frequency switching converters," *IEEE Trans. Magn.*, vol. 36, no. 4, pp. 831–834, Jul. 2000.

[10] P. P. Rodriguez, M. M. D. Bellar, R. R. S.Mu˜noz-Aguilar, S. S. Busquets- Monge, and F. F. Blaabjerg, "Multilevel clamped multilevel converters (MLC)," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1055–1060, Mar. 2012.

[11] K. Ilves, A. Antonopoulos, S. Norrga, and H.-.P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482–3494, Aug. 2012.

[12] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[13] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.

[14] H. L. Chan, K. W. E. Cheng, and D. Sutanto, "Bidirectional phase-shifted DC–DC converter," *IEEE Electron. Lett.*, vol. 35, no. 7, pp. 523–524, Apr. 1999.

[15] O.-C. Mak and A. Ioinovici, "Switched-capacitor inverter with high power density and enhanced regulation capability," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 45, no. 4, pp. 336–347, Apr. 1998.

[16] S.-J. Park, F.-S. Kang, M. H. Lee, and C.-U. Kim, "A new single-phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 831–843, May 2003.

[17] B. Axelrod, Y. Berkovich, and A. Ioinovici, "A cascade boost-switchedcapacitor- converter—Two level inverter with an optimized multilevel output

waveform," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 52, no. 12, pp. 2763–2770, Dec. 2005.

[18] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel DC voltage sources," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2643–2650, Aug. 2010.

[19] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/ parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.

[20] M. S. W. Chan and K. T. Chau, "A new switched-capacitor boostmultilevel inverter using partial charging," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 54, no. 12, pp. 1145–1149, Dec. 2007

AUTHOR'S BIOGRAPHIES

Mr.M Sandeep, PG Scholar and Completed B.Tech degree in Electrical & Electronics Engineering in 2012 from Jawaharlal Nehru Technological University, Hyderabad, presently pursuing M.Tech in "Power Electronics " in Anubose Institute of Technology, Paloncha, India.

Mr. K Aravind Swamy was born in 1988. He graduated from Jawaharlal Nehru Technological University, Hyderabad in the year 2009. He received M.Tech degree from Jawaharlal Nehru Technological University, Hyderabad in the year 2011. He is presently working as Assistant Professor in the Department of Electrical and Electronics Engineering at Anubose Institute of Technology, Paloncha,India.