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Implementation of High-Efficiency Adaptive Power Using VLSI

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ABSTRACT
High-efficiency input power range adaptive rectifier is presented. In this rectifier consists of two differential type sub-rectifiers and one control circuit unit . the proposed control unit circuit is used to detect the input power level by using sensing the converted output voltage rectifier is generating two control signals and to switch the rectifier between two operation modes. This IC chip device has been fabricated with 0.18-μm CMOS technology. With two three-stage differential-type of rectifiers as the sub-rectifiers, the low power conversion efficiency (PCE) region is extended.

Keyword : Micro wind ,DSCH , adaptive, low power conversion efficiency (PCE)
Region, rectifier.

I INTRODUCTION
The result of semiconductor technology, electronic circuits are becoming high complicated,
And the power consumption is increasing very high .However, the resulting in battery capacity is failed to receive the chip power consumption, this technique fallows Moore's law. To low power applications .like wireless sensor nodes and human interface devices, have been intensely researched and deployed. To extend the battery life for never ending or changing operation, a power and human consumption technique can be employed for use as an alternative power source. There are many types of power sources, such as ambient light ,vibration, thermal energy, radio frequency (RF) signal, and so on. This sources are different applications like wireless applications ,Wi-Fi and Bluetooth applications, to convert received RF signal into a DC voltage signals .and in this project rectifier is most important component .and different types of architectures are designed, and one of the most important application of rectifier is power consumption efficiency which is defined

PCE =Pout put/P input

In this principle P output is output is output power and P input is input power of the rectifier ,when the input power reaches certain level the power loss transistor will increase the faster than the output power, and many models and analyzes have been developed.

II DESIGN TECHNIQUES
The harvesting and storing of the power in a power harvester requires a rectifier with high PCE. As shown in Fig. 1, a typical hill-shaped PCE curve as a function of two major input power functions, one is the peak PCE and other one optimal PCE range. The peak PCE is the maximum PCE and one rectifier can reach, At the peak PCE condition, the required input power level is defined by *P*in ,peak. At this input power level, the rectifier can operate most efficiently. Obviously, the PCE will drop when the input power is below this level since the rectifier pumps a lower voltage with a limited input power. Although the pumped-up voltage keeps going higher with a larger input power, the loss in the rectifier itself starts to increase faster than the power it can provide if the input power is larger than *P*in ,peak. This indicates the rectifier can only operate efficiently with in a certain input power range. The input power range over which the PCE of the rectifier is still more than 80% of its peak value is defined as the optimal PCE range of the rectifier. The optimal

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PCE range describes the suitable input power range for a rectifier.

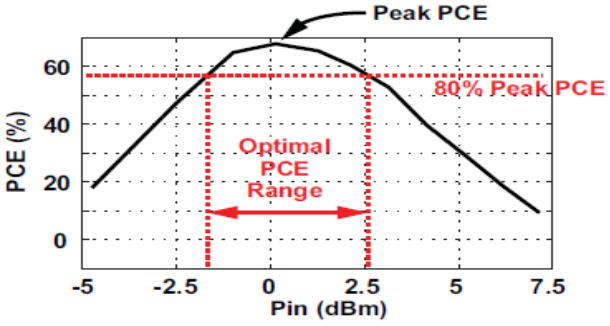

Fig 1. Typical PCE curve as a function of input power.

III. PROPOSED ADAPTIVE RECTIFIE

The proposed adaptive rectifier consists of two sub-rectifiers, a control circuit, and three transistor switches. The sub rectifiers scalable according to the RF input power and its harvested output voltage. In this brief, a three-stage differential-type rectifier is used. The sub-rectifiers receive differential RF input signals and then charge up the storing capacitors (included in the sub-rectifier block).The control circuit senses the output voltage of the rectifier *V*out and generates two control signals*V*ctrl1 and *V*ctrl2 which will be used to control the transistor switches. *R* load is the loading resistor, and it is2-k_ in this brief. The operation of the proposed adaptive rectifier can be divided into three regions as shown In Region I, the input power is very weak and therefore the output voltage is very small. Both control voltages are zero. The transistor *M*p1 is turned on, and *M*n1and *M*n2 are turned off. The entire rectifier is operated by only one sub-rectifier, as shown in Fig. 5, and hence, the entire rectifier still works under this condition. Regions II and III correspond to the two major operation modes, i.e., parallel mode in Region II and series mode in Region III. when the input power is small (Region II), the control voltages *V*ctrl1 and *V*ctrl2 are equal to the high level (*V*out) and ground, respectively. The transistors *M*n1and *M*p1 are turned on, and *M*n2 is turned off. The whole circuit is now operating with the two sub-rectifiers in parallel, as shown in fig.

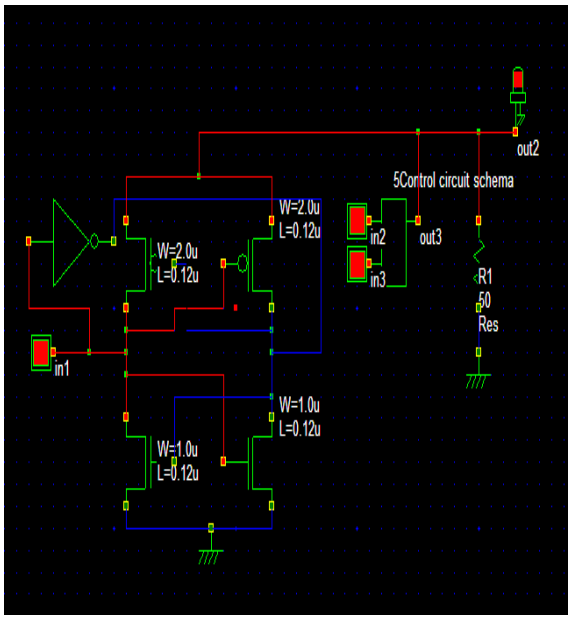

Fig 2ADAPTIVE REGION I

The input power is very weak and therefore the output voltage is very small. Both control voltages are zero. The transistor is turned on, and *M*n1and *M*n2 are turned off. The entire rectifier is operated by only one sub-rectifier, and hence, the entire rectifier still works under this condition.

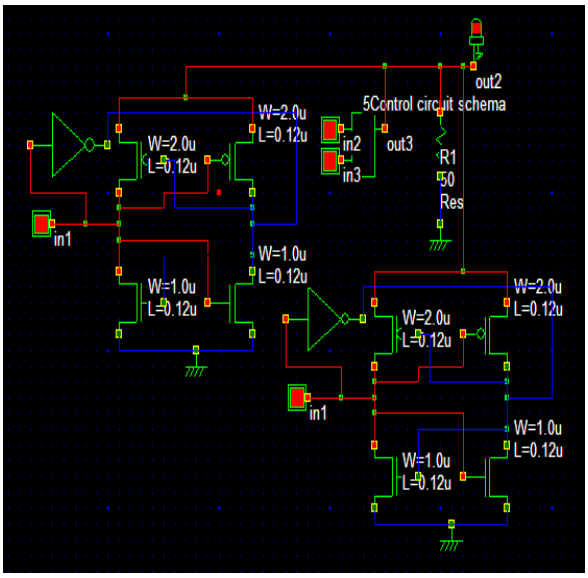

Fig 3. ADAPTIVE REGION II

This circuit shows the parallel mode operation of the adaptive power region.

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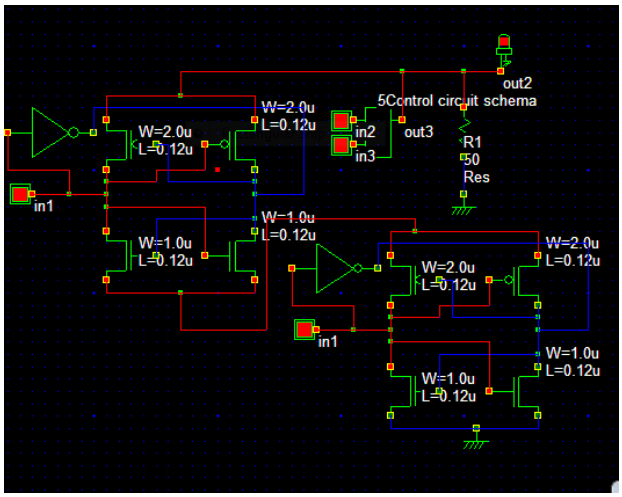

Fig 4 shows adaptive region III

This schematic shows the series mode operation of adaptive power region operation. The sub-rectifier is only needs to provide half of the loading current, and the rectifier can supply power is more efficient. Under this high input power level (Region III), on the other hand, the output voltage is *V*out will be provided over the switching point and drive *V*ctrl1to a low voltage level and *V*ctrl2 to a high. The transistor *M*n2 is turned on, and the transistors *M*n1 and *M*p1 are turned off. The whole circuit is now equivalent to two sub-rectifiers in series that the circuit can increase the output voltage is *V*out higher, providing more power to the load. The entire circuit can switch between these three regions according to the input power level adaptively by sensing the output voltage.

Control unit operation

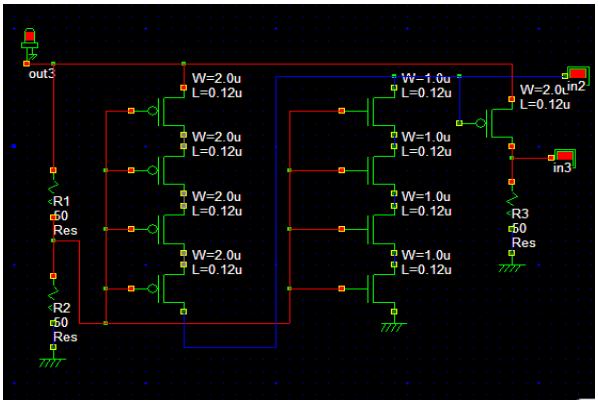

Fig 5 This circuit it shows the adaptive power operation in control unit technique

IV DESIGN TECHNIQUES:

Differential-Type Rectifier Circuit

This type of rectifiers are used for the sub-rectifiers in this operation . This unit cell is shown in The differential input signals are coupled to nodes A and B by the capacitors *C*1 and*C*2. The operation of the unit cell can be divided into two phases operations .In the phase that *RF* +in is positive and *RF*−in is negative, the transistor*M*2 is turned on and the current flows from the ground to node B. At the peak value , node B will be charged to the ground. Then, in the phase that *RF*+ in is negative and *RF*−in is positive ,node B will be pushed up and turn on the transistor *M*1. Node A is therefore charged up by the current flowing from the ground. At the peak, node B will be involved.

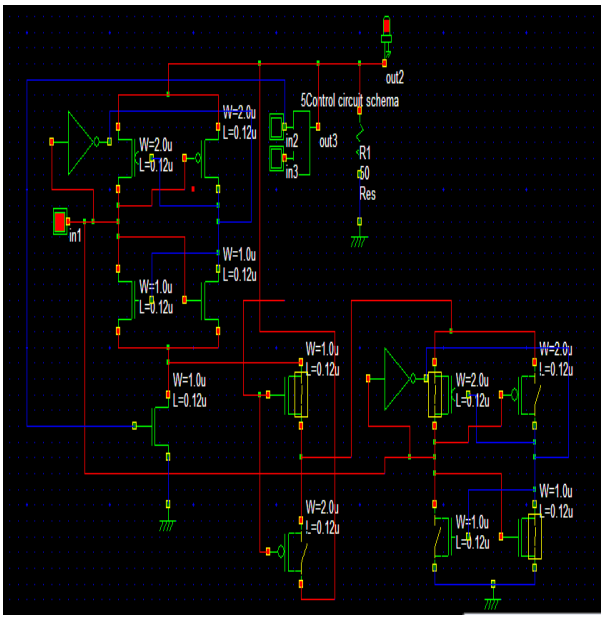

Fig 6 Proposed system schematic diagram related adaptive power

The proposed control circuit is shown where *V* out is the output voltage of the entire adaptive rectifier. To eliminate the maximum PCE, the control circuit has to reduce the minimum power . Hence, the resistors *R*1, *R*2, and *R*3 the ratio of *V* sg, *p*/*V* gs, *n* is equal to R1/R2, which is much larger than the unity. So the output voltage increases to zero. the proposed rectifier is activated even without the active control circuit

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V SIMULATION RESULT

Proposed schematic diagram related simulation result

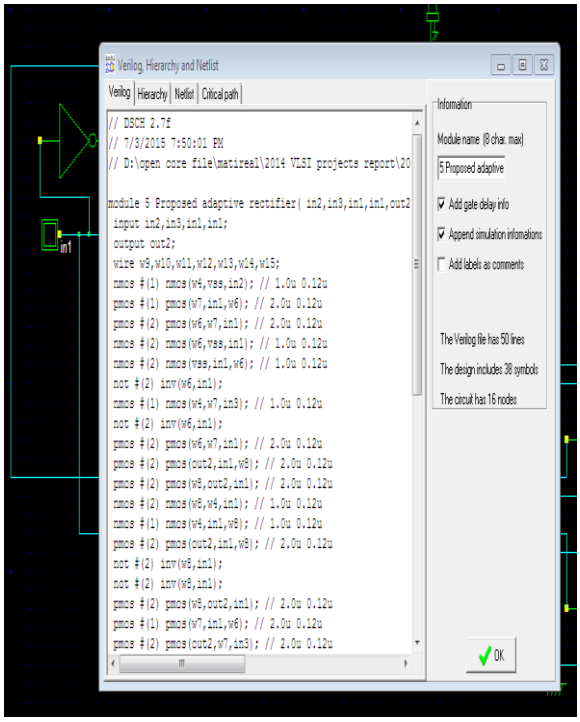

Fig 7 Verilog code generation related to proposed schematic diagram

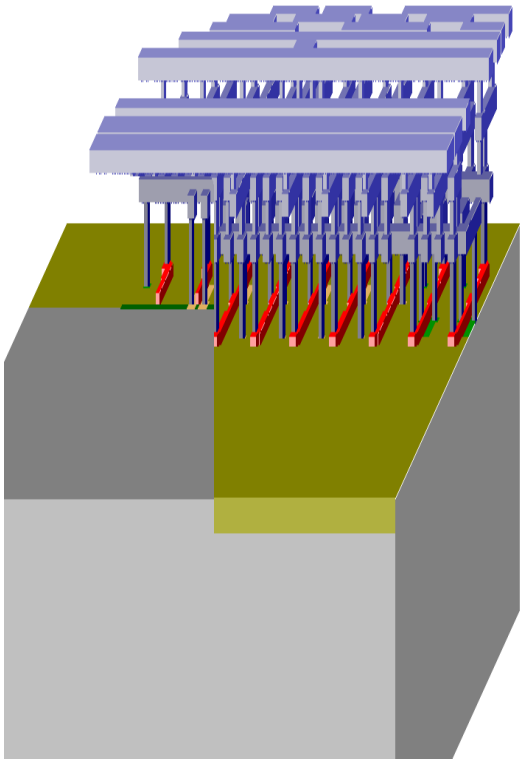

Fig 9.3D design for schematic diagram

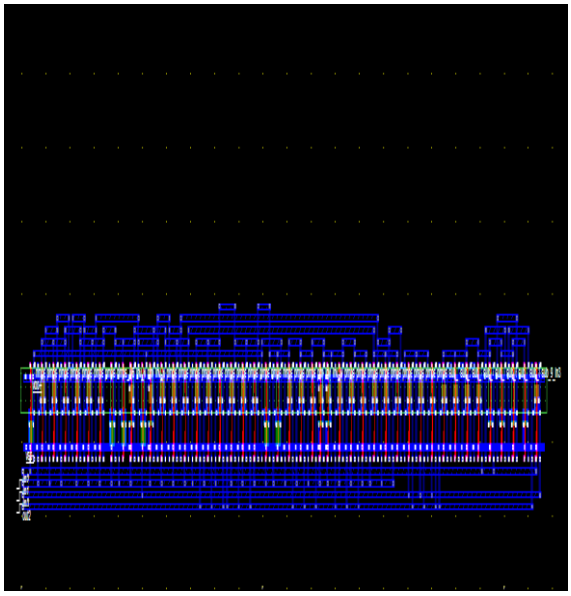

Fig 8 layout diagram for proposed system

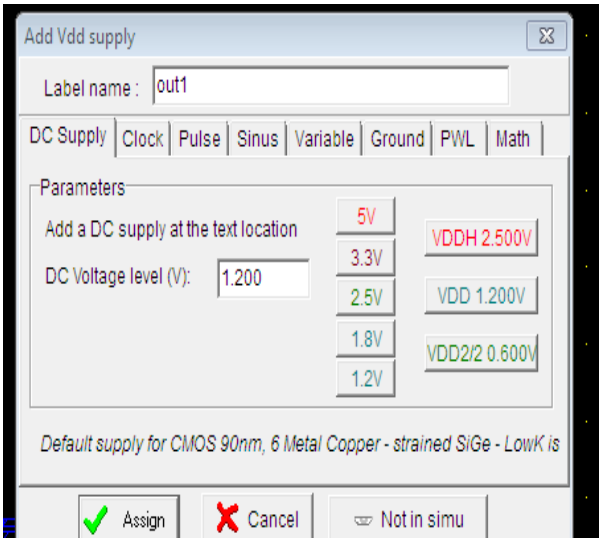

Fig 10.Voltage levels of proposed system

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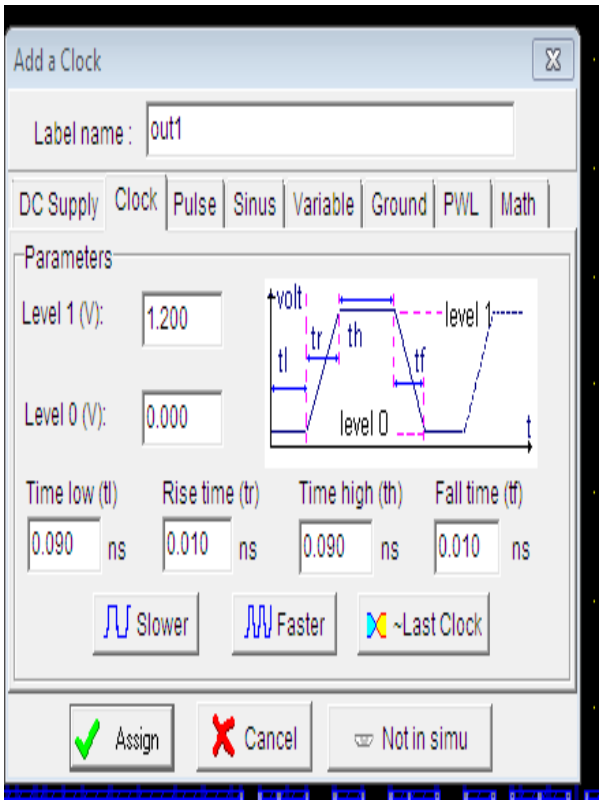

Fig 11.Clock signal generation

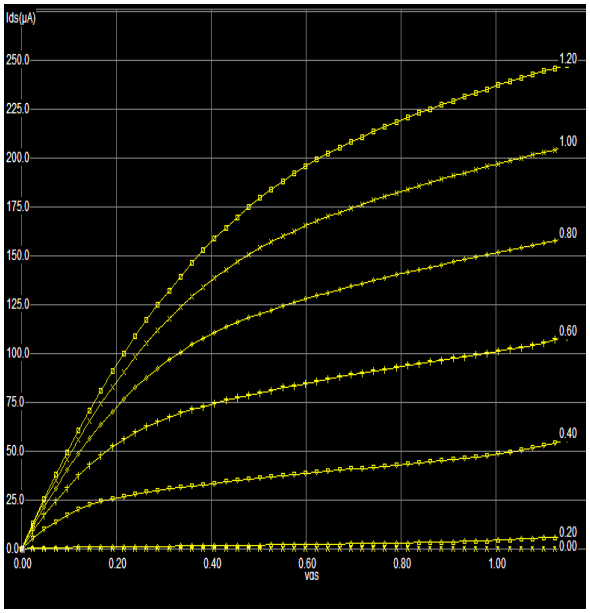

Fig 12.Characteristics of MOS transistor

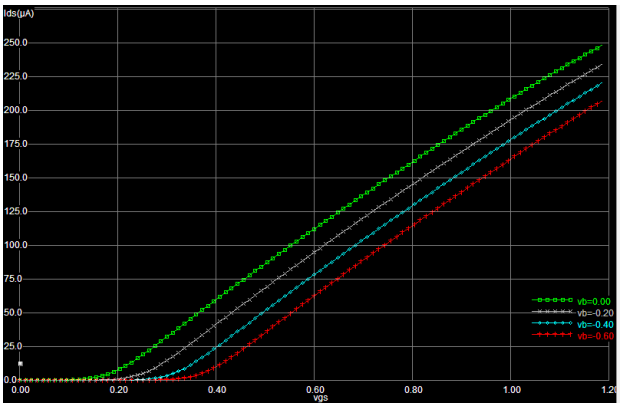

Fig 13.Drain current vs drain voltage

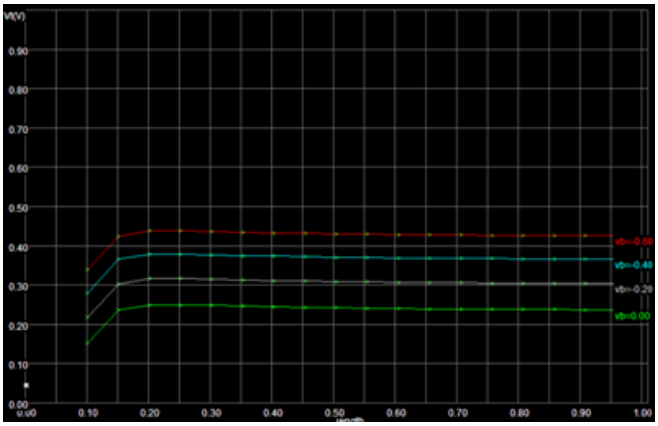

Fig14.Proposed system threshold voltage values

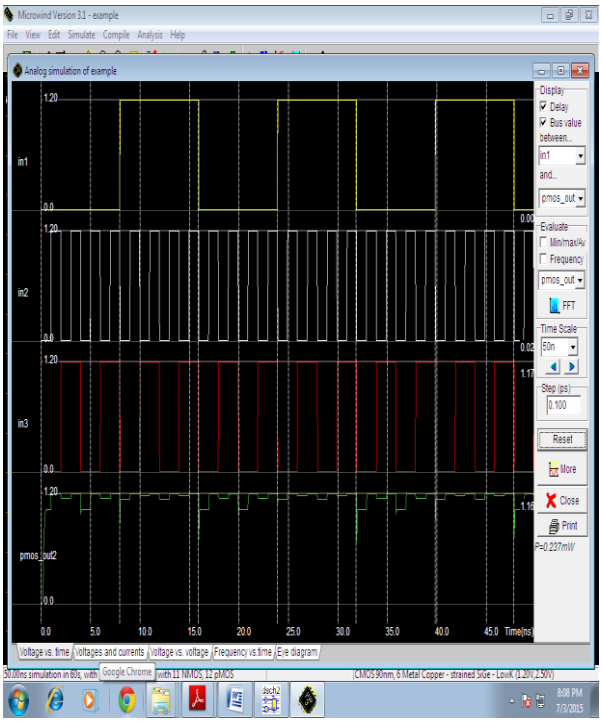

Fig 15.Voltage vs time variation simulation result

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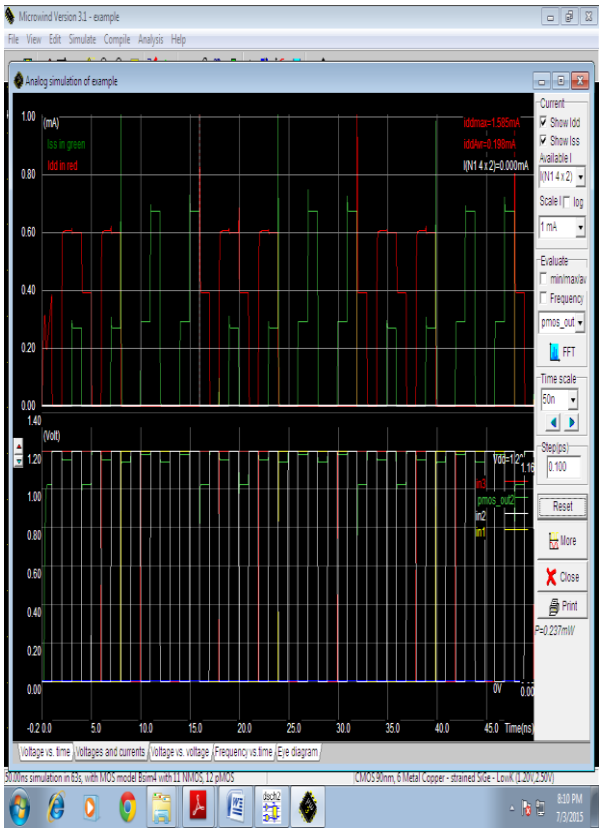

Fig 16.Voltage vs current simulation result

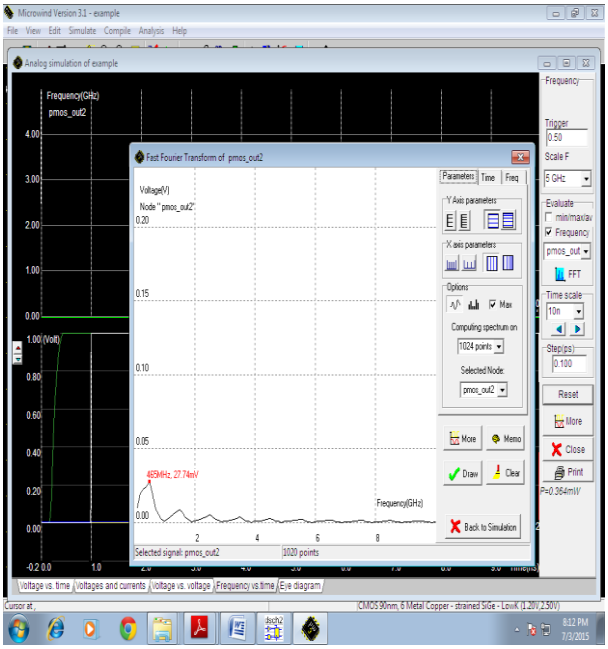

Fig 17.Frequency vs time related fft simulation result

VI CONCLUSTION

The result of optimal low power adaptive PCE technique we find the maximum range of frequency is 100 MHZ, and the voltage is 158.9mv and the total current is 1.585mA the optimal power is calculated 0.251wis required in our prose system we design new structure that has an extended optimal PCE range .Using a three-stage conventional differential-type rectifier as the sub rectifier,\an adaptive rectifier that can switch between parallel and series modes is proposed.

VII References

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