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Speed Control of VSI Fed PMBLDC Motor with Power Factor Correction Control Technique

Marla Mahesh
M.Tech (Power Electronics),
Department of Electrical Engineering,
Swami RamanandaTirtha Institute of Science & Technology, Nalgonda, T.S, India.

Bhukya John Wesley
Assistant professor,
Department of Electrical Engineering,
Swami RamanandaTirtha Institute of Science & Technology, Nalgonda, T.S, India.

Abstract:

BLDC motoris better choice for low-power applications. Power factor correction control technique used in bridgeless (BL) buck-boost converter. The voltage source inverter fed with DC-link capacitor, the speed control of motor is done by controlling the dc link voltage. The proposed system was designed with filter circuit, DC-DC buck-boost converter, voltage source inverter and BLDC motor. Bridge-less buck-boost converter is designed with power factor correction technique. The converter designed with reduced number of switches, which reduces switching losses. The performance characteristics are observed with MATLAB/ simulink software.

Key words:

power factor correction (PFC), BLDC motor, discontinuous mode, BL-BU-BO converter.

I.INTRODUCTION:

Efficiency and cost are the major concerns in the development of low-power motor drives targeting household applications such as fans, water pumps, blowers, mixers, etc. [1]. The use of the brushless direct current (BLDC) motor in these applications is becoming very common due to features of high efficiency, high flux density per unit volume, low maintenance requirements, and low electromagnetic-interference problems. These BLDC motors are not limited to household applications, but these are suitable for other applications such as medical equipment, transportation, HVAC, motion control, and many industrial tools [2],[3].

A BLDC motor has three phase windings on the stator and permanent magnets on the rotor [4]. The BLDC motor is also known as an electronically commutated motor because an electronic commutation based on rotor position is used rather than a mechanical commutation which has disadvantages like sparking and wear and tear of brushes and commutatorassembly [5].Power quality problems have become important issues to be considered due to the recommended limits of harmonics in supply current. A BLDC motor when fed by a diode bridge rectifier (DBR) with a high value of dc link capacitor draws peaky current which can lead to a THD of supply current of the order of 65% and power factor as low as 0.8 [6]. For improving power quality at ac mains supply, a DBR with pfc converter is used.

The choice of mode of operation of a PFC converter is a critical issue because it directly affects the cost and rating of the components used in the PFC converter. The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are the two modes of operation in which a PFC converter is designed to operate [7]. In CCM, the current in the inductor or the voltage across the intermediate capacitor remains continuous, but it requires the sensing of two voltages (dc link voltage and supply voltage) and input side current for PFC operation, which is not cost-effective. On the other hand, DCM requires a single voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains, but at the cost of higher stresses on the PFC converter switch; hence, DCM is preferred for low-power applications [8]. The conventional PFC scheme of the BLDC motor drive utilizes a pulsewidth-modulated voltage source inverter (PWM-VSI) for speed control with a constant dc link voltage.

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This offers higher switching losses in VSI as the switching losses increase as a square function of switching frequency. As the speed of the BLDC motor is directly proportional to the applied dc link voltage, hence, the speed control is achieved by the variable dc link voltage of VSI. This allows the fundamental frequency switching of VSI (i.e., electronic commutation) and offers reduced switching losses.

PROPOSED CONVERTER:

Fig. 1 shows the proposed BL buck–boost converter-based VSI-fed BLDC motor drives. The parameters of the BL buck–boost converter are designed such that it operates in discontinuous inductor current mode (DICM) to achieve an inherent power factor correction at ac mains. The speed control of BLDC motor is achieved by the dc link voltage control of VSI using a BL buck–boost converter.

This reduces the switching losses in VSI due to the low frequency operation of VSI for the electronic commutation of the BLDC motor. The performance of the proposed drive is evaluated for a wide range of speed control with improved power quality at ac mains. Moreover, the effect of supply voltage variation at universal ac mains is also studied to demonstrate the performance of the drive in practical supply conditions. Voltage and current stresses on the PFC converter switch are also evaluated for determining the switch rating and heat sink design. Finally, a hardware implementation of the proposed BLDC motor drive is carried out to demonstrate the feasibility of the proposed drive over a wide range of speed control with improved power quality at ac mains.The proposed configuration of the BL buck–boost converter has the minimum number of components and least number of conduction devices during each half cycle of supply voltage which governs the choice of the BL buck–boost converter for this application.

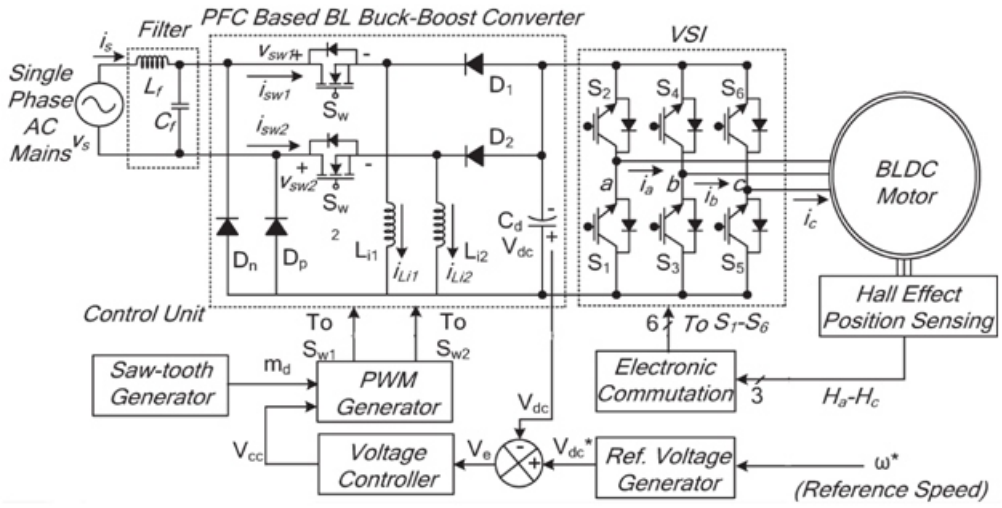

Fig. 1: Proposed BLDC motor drive with front-end BL buck–boost converter.

PRINCIPLE OF OPERATION OF PROPOSED CONVERTER:

The operation of the PFC BL buck–boost converter is classified into two parts which include the operation during the positive and negative half cycles of supply voltage and during the complete switching cycle.

Operation during Positive and Negative Half Cycles of Supply Voltage:

In the proposed scheme of the BL buck–boost converter, switches Sw1 and Sw2 operate for the positive and negative half cycles of the supply voltage, respectively. During the positive half cycle of the supply voltage, switch Sw1, inductor Li1, and diodes D1 and Dp are operated to transfer energy to dc link capacitor Cd as shown in Fig. 2(a)–(c). Similarly, for the negative half cycle of the supply voltage, switch Sw2, inductor Li2, and diodes D2 and Dn conduct as shown in Fig. 3(a)–(c). In the DICM operation of the BL buck–boost converter, the current in inductor Li becomes discontinuous for certain duration in a switching period. Fig. 2(d) shows the waveforms of different parameters during the positive and negative half cycles of supply voltage.

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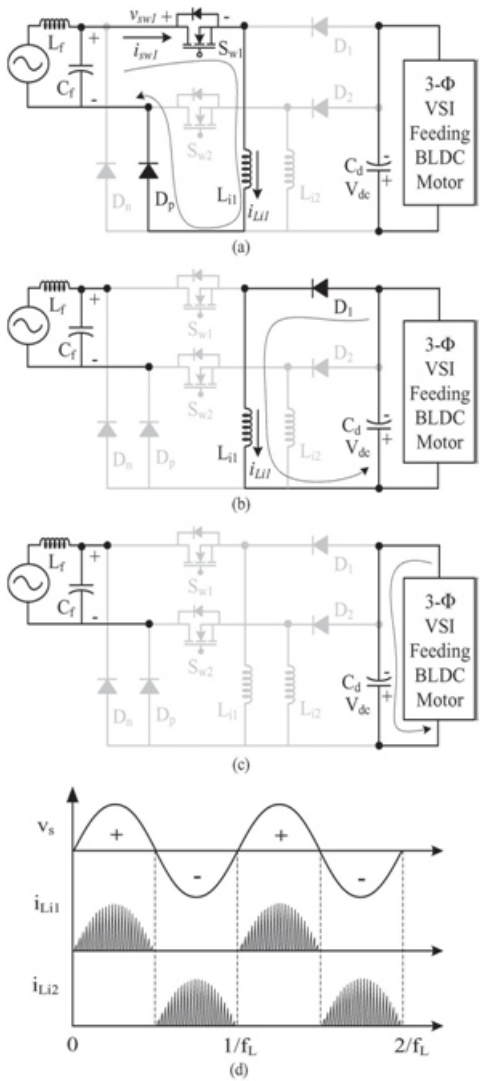


Fig. 2: Operation of the proposed converter in different modes. (a) Mode I. (b) Mode II. (c) Mode III. (d) Waveforms for positive and negative half cycles of supply voltage.

Operation during Complete Switching Cycle:

Three modes of operation during a complete switching cycle are discussed for the positive half cycle of supply voltage as shown hereinafter. Mode I: In this mode, switch Sw1 conducts to charge the inductor Li1; hence, an inductor current iLi1 increases in this mode as shown in Fig. 2(a). Diode Dp completes the input side circuitry, whereas the dc link capacitor Cd is discharged by the VSI-fed BLDC motor as shown in Fig. 3(d). Mode II: As shown in Fig. 2(b), in this mode of operation, switch Sw1 is turned off, and the stored energy in inductor Li1 is transferred to dc link capacitor Cd until the inductor is completely discharged.

The current in inductor Li1 reduces and reaches zero as shown in Fig. 3(d).Mode III: In this mode, inductor Li1 enters discontinuous conduction, i.e., no energy is left in the inductor; hence, current iLi1 becomes zero for the rest of the switching period. As shown in Fig. 2(c), none of the switch or diode is conducting in this mode, and dc link capacitor Cd supplies energy to the load; hence, voltage Vdc across dc link capacitor Cd starts decreasing.The operation is repeated when switch Sw1 is turned on again after a complete switching cycle. Similarly, for the negative half cycle of the supply voltage, switch Sw2, inductor Li2, and diodes Dn and D2 operate for voltage control and PFC operation.

IV. DESIGN OF PFC BL BUCK–BOOST CONVERTER:

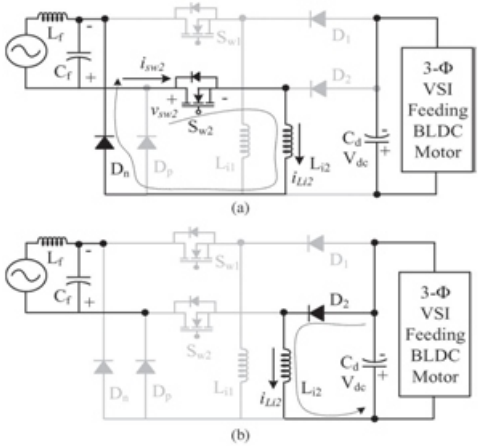
A PFC BL buck–boost converter is designed to operate in DICM such that the current in inductors Li1 and Li2 becomes discontinuous in a switching period. For a BLDC of power rating 251 W, a power converter of 350 W (Po) is designed. For a supply voltage with an rms value of 220 V, the average voltage appearing at the input side is given as

Vin = [2√2Vs]/π = [2√2×220]/π ≈ 198 V.

The relation governing the voltage conversion ratio for a buck–boost converter is given as

d = Vdc/[Vdc + Vin]

The proposed converter is designed for dc link voltage control from 50 V (Vdc min) to 200 V (Vdcmax) with a nominal value (Vdc des) of 100 V; hence, the minimum and the maximum duty ratio (dmin and dmax) corresponding to Vdc min and Vdcmax are calculated as 0.2016 and 0.5025, respectively.



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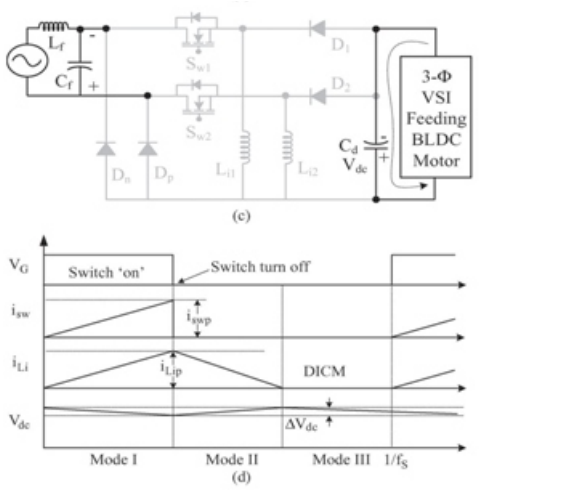

Fig 3: Operation of the proposed converter in different modes. (a) Mode I. (b) Mode II. (c) Mode III. (d) Waveforms during complete switching cycle.

Inductor parameters (Li1 and Li2)

The value of inductance Lic1, to operate in critical conduction mode in the buck–boost converter, is given as
Lic1 = R(1 – d)2/2fs
Where R is the equivalent load resistance, d is the duty ratio, and fs is the switching frequency.
Now, the value of Lic1 is calculated at the worst duty ratio of dmin such that the converter operates in DICM even at very low duty ratio. At minimum duty ratio, i.e., the BLDC motor operating at 50 V (Vdc min), the power (Pmin) is given as 90 W (i.e., for constant torque, the load power is proportional to speed).
The value of inductance Lic min corresponding to Vdc min is calculated as

Lic min = 442.67 µH.
The values of inductances Li1 and Li2 are taken less than 1/10th of the minimum critical value of inductance to ensure a deep DICM condition [9]. The analysis of supply current at minimum duty ratio (i.e., supply voltage as 220 V and dc link voltage as 50 V) is carried out for different values of the inductor (Li1 and Li2). The supply current at higher values of the input side inductor is highly distorted due to the inability of the converter to operate in DICM at peak values of supply voltages.

Hence, the values of inductors Li1 and Li2 are selected around 1/10th of the critical inductance and are taken as 35 µH.

DC Link Capacitor (Cd)

The design of the dc link capacitor is governed by the amount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows.
Cd = Id/2ωΔVdc
Now, the value of the dc link capacitor is calculated for the designed value Vdc des with permitted ripple in the dc link voltage (ΔVdc) taken as 3% as
Cd= Id/2ωΔVdc = [Po/Vdcdes]/2ωΔVdc
Input Filter (Lf and Cf)
A second-order low-pass LC filter is used at the input side to absorb the higher order harmonics such that it is not reflected in the supply current. The maximum value of filter capacitance is given as
Cmax = [Ipeak/ωLVpeak]tan(θ)
The value of the filter inductor is designed by considering the source impedance (Ls) of 4%–5% of the base impedance.
Lf =Lreq + Ls 1/4π2f2cCf

CONTROL STRATEGY

The control of the PFC BL buck–boost converter-fed BLDC motor drive is classified into two parts as follows.
Voltage Follower Approach
The control of the front-end PFC converter generates the PWM pulses for the PFC converter switches (Sw1 and Sw2) for dc link voltage control with PFC operation at ac mains. A single voltage control loop (voltage follower approach) is utilized for the PFC BL buck–boost converter operating in DICM. A reference dc link voltage (V*dc) is generated as
V*dc = kvω*
Where kv and ω* are the motor's voltage constant and the reference speed, respectively.
The voltage error signal (Ve) is generated by comparing the reference dc link voltage (V*dc) with the sensed dc link voltage (Vdc) as
Ve(k) = V*dc(k) – Vdc(k)
Where k represents the kth sampling instant.

Control of BLDC Motor: Electronic Commutation:

An electronic commutation of the BLDC motor includes the proper switching of VSI in such a way that a symmetrical dc current is drawn from the dc link capacitor for 120 and placed symmetrically at the center of each

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phase. A Hall-effect position sensor is used to sense the rotor position on a span of 60, which is required for the electronic commutation of the BLDC motor.

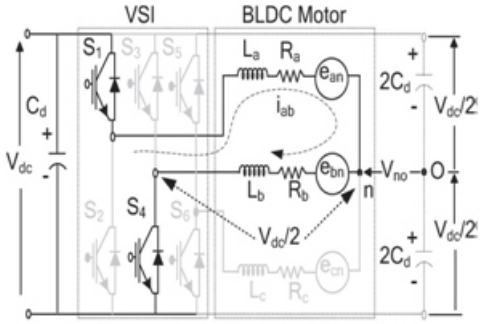

Fig 4: Operation of a VSI-fed BLDC motor when switches S1 and S4 are conducting.

SIMULATION RESULTS:

The performance of the proposed BLDC motor drive is simulated in MATLAB/Simulink environment using the SimPower-System toolbox. The performance evaluation of the proposed drive is categorized in terms of the performance of the BLDC motor and BL buck–boost converter and the achieved power quality indices obtained at ac mains. The parameters associated with the BLDC motor such as speed (N), electromagnetic torque (Te), and stator current (ia) are analyzed for the proper functioning of the BLDC motor. Parameters such as supply voltage (Vs), supply current (is), dc link voltage (Vdc), inductor's currents (iLi1, iLi2), switch voltages (Vsw1, Vsw2), and switch currents (isw1, isw2) of the PFC BL buck–boost converter are evaluated to demonstrate its proper functioning.

Moreover, power quality indices such as power factor (PF), displacement power factor (DPF), crest factor (CF), and THD of supply current are analyzed for determining power quality at ac mains.The dynamic behavior of the proposed drive system during a starting at 50 V, step change in dc link voltage from 100 to 150 V, and supply voltage change from 270 to 170 V is shown in Fig. 8. A smooth transition of speed and dc link voltage is achieved with a small overshoot in supply current under the acceptable limit of the maximum allowable stator winding current of the BLDC motor.

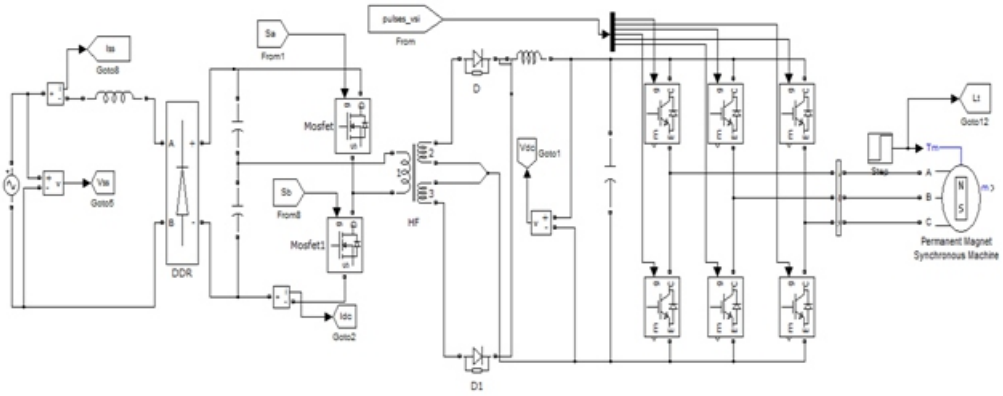

Fig 5: Simulation circuit of Proposed BLDC motor drive with front-end BL buck–boost converter

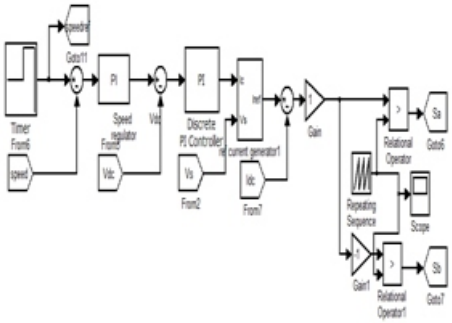

Fig 6: control circuit

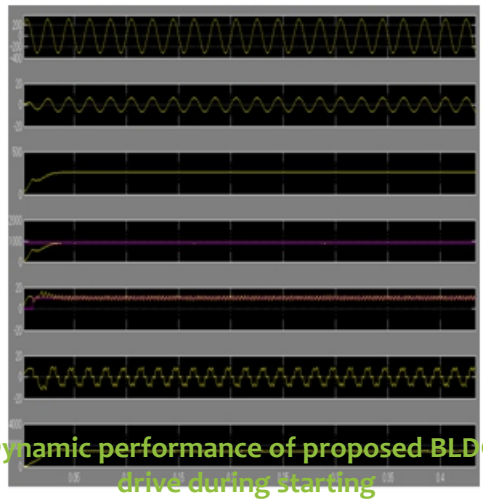

Fig 7: Dynamic performance of proposed BLDC motor drive during starting

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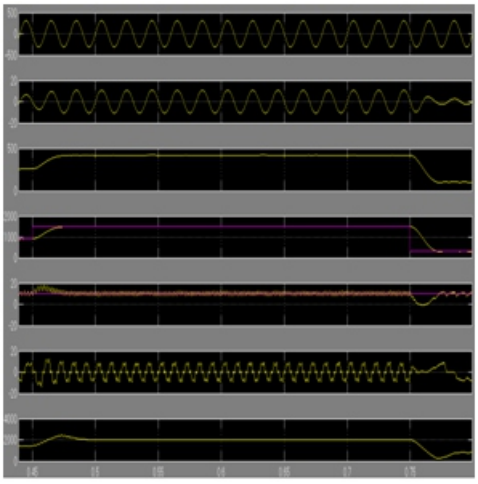

Fig 8: Dynamic performance of proposed BLDC motor drive duringspeed control

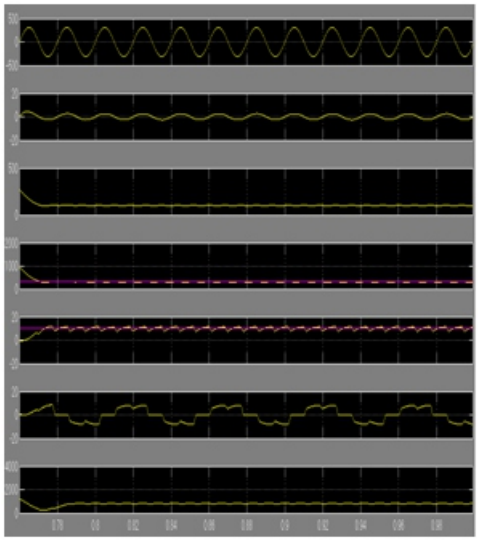

Fig 9: Dynamic performance of proposed BLDC motor drive duringsupply voltage variation at ratedconditions.

CONCLUSION:

A PFC BL buck–boost converter-based VSI-fed BLDC motordrive has been proposed targeting low-power applications.A new method of speed control has been utilized by controllingthe voltage at dc bus and operating the VSI at fundamentalfrequency for the electronic commutation of the BLDC motorfor reducing the switching losses in VSI. The front-end BLbuck–boost converter has been operated in DICM for achievingan inherent power factor correction at ac mains.

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