ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A New Hybrid Multilevel Converter with DC-Fault Blocking Capability: AAC

Md.Asmath Tharunnam
MTech Student
Department of EEE
AnuBose Institute of Technology(ABIT)
Paloncha, Khammam, India

C.Ch Mohan Rao
Associate Professor & HoD
Department of EEE
AnuBose Institute of Technology(ABIT)
Paloncha, Khammam, India

Abstract: ***This paper explains the working principles, supported by simulation results, of a new converter topology intended for HVDC applications, called the alternate arm converter (AAC). It is a hybrid between the modular multilevel converter, because of the presence of H-bridge cells, and the two-level converter, in the form of director switches in each arm. This converter is able to generate a multilevel ac voltage and since its stacks of cells consist of H-bridge cells instead of half-bridge cells, they are able to generate higher ac voltage than the dc terminal voltage. This allows the AAC to operate at an optimal point, called the "sweet spot," where the ac and dc energy flows equal. The director switches in the AAC are responsible for alternating the conduction period of each arm, leading to a significant reduction in the number of cells in the stacks. Furthermore, the AAC can keep control of the current in the phase reactor even in case of a dc-side fault and support the ac grid, through a STATCOM mode. Simulation results and loss calculations are presented in this paper in order to support the claimed features of the AAC.***

Index Terms—AC–DC power converters, emerging topologies, fault tolerance, HVDC transmission, multilevel converters, power system faults, STATCOM.

INTRODUCTION:

Increasing attention is being paid to HVDC transmission systems, especially because most of the new schemes are intended to connect remote renewable sources to the grid and The most effective way to do it is to transmit the generated power using HVDC instead of HVAC [1]. For offshore HVDC applications, voltage-source converters (VSCs) are more suitable than current-source converters (CSCs) [2] due to to their black-start capability and ability to operate in weak ac grids, such as a network of wind turbine generators.

However, compared to CSCs, their power ratings are limited and their efficiency is somewhat poorer although recent developments in semiconductor devices are closing the gap in both cases so that VSCs are becoming economically viable as technological solutions in large HVDC schemes; some of them to be commissioned in the next couple of years. Since the 1990s, a great deal of research effort has been directed to improving converters primarily to make them more power efficient than the first generation of VSCs.

The modular multilevel converter (MMC), published in 1998 for STATCOM applications [9], published in 2003 for HVDC Power Transmission [10], and followed up in brought several new features to VSC. It replaced the series-connected insulated-gate biploar transistor (IGBT) in each arm of the two-level converter by a stack of half-bridge cells which consist of a charged capacitor and a set of IGBTs. Sincet the voltage of each cell is small compared to the ac and dc voltages, a large number of cells are placed in series in each stack, resulting in the creation of a voltage waveform with numerous steps. This characteristic has two main consequences: 1) the generated ac current is very close to a sine wave and no longer requires any filtering, thus saving the implementation of bulky and costly ac filters and 2) the converter does not rely on high-frequency PWM to syntheses voltage waveforms,

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thus greatly reducing the switching loss and thereby improving the overall efficiency.

Existing System:

Briefly presented in [20], the alternate arm converter (AAC) is a hybrid topology which combines features of the two-level and multilevel converter topologies. As illustrated in Fig. 2, each phase of the converter consists of two arms, each with a stack of H-bridge cells, a director switch, and a small arm inductor. The stack of cells is responsible for the multistep voltage generation, as in a multilevel converter.

Since H-bridge cells are used, the voltage produced by the stack can be either positive or negative; thus, the converter is able to push its ac voltage higher than the dc terminal voltage if required. The director switch is composed of IGBTs connected in series in order to withstand the maximum voltage which could be applied across the director switch when it is in the open state. The main role of this director switch is to determine which arm is used to conduct the ac current.

Indeed, the key feature of this topology is to use essentially one arm per half cycle to produce the ac voltage. By using the upper arm to construct the positive half-cycle of the ac sine wave and the lower arm for the negative part, the maximum voltage that each stack of cells has to produce is equal to half of the dc bus voltage, which is approximately half the rating of the arm of the MMC.

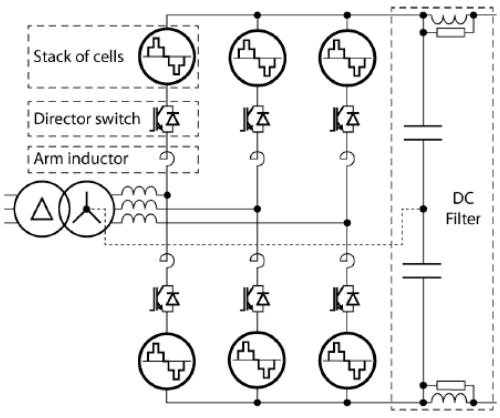

Fig. 2. Schematic of the alternate arm converter, with the optional middle-point connection shown in a dashed line.

Proposed System:

In order to confirm the operation of this new topology, a simulation model has been realised in Matlab/Simulink using the SimPowerSystems toolbox. The characteristics of this model have been chosen in order to reflect a realistic power system, albeit at medium voltage (MV), and key parameters are summarized in Table II. The transformer interfacing the ac grid and the converter has its turns ratio defined such that the converter operates close to the sweet-spot ac voltage, as defined in Section II-C. The number of cells chosen for each stack follows the second case from Table II so that dc-side fault blocking is available. A small additional allowance was made so that the converter can still operate and block faults with an ac voltage of 1.05 p.u. The choice is therefore for nine cells charged at 1.5 kV each per stack. The minimum number of cells for operation without overlap (sweet spot operation only) and without fault blocking would be seven cells. The choice of nine cells per stack allows the AAC to operate with 1-ms overlap period which is sufficient to internally manage the energy storagewithin the current rating of the IGBTs (1.2 kA). Finally, a dc filter has been fitted to the AAC model, as illustrated in Fig. 2, and tuned to have critical damping and a cutoff frequency at 50 Hz; well below the first frequency component expected on the dc side which is a six-pulse ripple (i.e., 300 Hz in this model).

Performance Under Normal Conditions

Based on this model, the behavior of the AAC was simulated under normal conditions in order to test its performance. In this section, the converter is running in rectifier mode, converting 20 MW and providing 5-MVAr capacitive reactive power. Fig. 5 shows the waveforms generated by the AAC in this simulation. First, the converter is very responsive. Second, the waveform of the phase current in the ac grid connection is high quality with only very low amplitude harmonics, as shown by the Fourier analysis in Fig. 6. Third, the dc current exhibits the characteristic six-pulse ripple inherent in the rectification method of this converter, but attenuated

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by an inductor placed between the converter and the dc grid. Fourth, this rectification action of the current is particularly observable in the fourth graph which shows the arm currents in phase A, indicating when an arm is conducting. Finally, the fifth graph presents the average voltage of the cells in both stacks of phase A, with their offstate voltage being controlled to stay at the reference value of 1.5 kV.

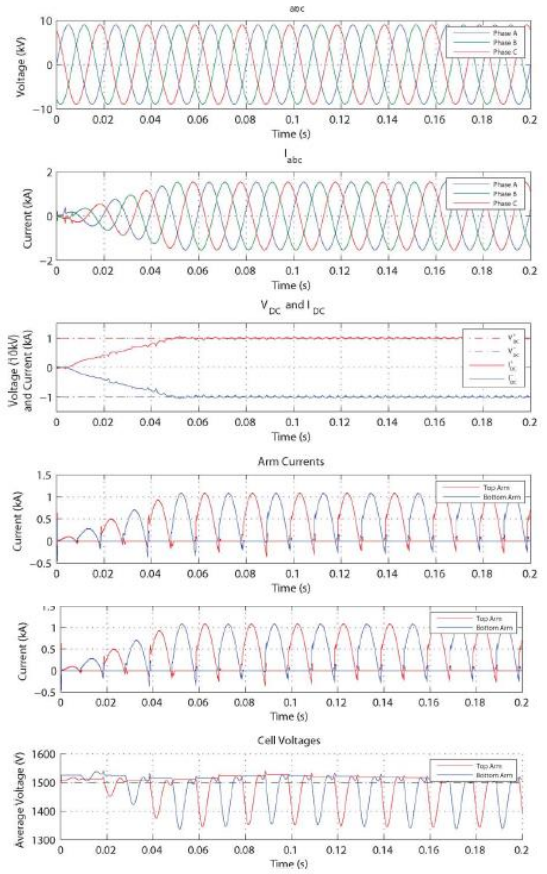

Fig. 5. Simulation results of a 20-MW AAC model running in rectifier mode under normal conditions.

However, the conduction loss is kept small despite the use of H-bridge cells by the fact that the stacks do not have to be rated for the full dc bus voltage because of the presence of the director switches;

Simulations of a small-scalemodel show that this converter is able to deliver performance under normal conditions, in terms of efficiency and current waveform quality, and provide rapid responses in the case of ac- or dc-side faults. Its ability to keep control of the current even during dc faults is a significant advantage, especially in multiterminal HVDC applications, and can be extended into STATCOM operation in order to support the ac grid during the outage, by providing potentially up to 2.0-p.u. reactive.

CONCLUSION

The AAC is a hybrid topology between the two-level converter and the modular multilevel converter. By combining stacks of H-bridge cells with director switches, it is able to generate almost harmonic-free ac current, as does the modular multilevel approach. And by activating only one arm per half cycle, like the two-level converter, it can be built with fewer cells than the MMC. Since this topology includes cells with capacitors which are switched into the current path, special attention needs to be paid to keeping their stored energy (equivalently, the cell capacitor voltage) from drifting away from their nominal value. By examining the equations, which govern the exchange of energy between the ac and dc sides, an ideal operating condition has been identified, called the "sweet spot." When the converter is running at this condition, the energy levels of the stacks return to their initial values at the end of each cycle without any additional action. In cases where this equilibrium is not attained, an overlap period can be used to run a small dc current in order to balance the stacks by sending the excess energy back to the dc capacitors.

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Author's Biographies

Miss. Md.Asmath Tharunnam, PG Scholar and Completed B.TECH degree in Electrical & Electronics Engineering in 2013 from JNTU,hyderabad. She is presently pursuing M.Tech in "Power Electronics" in **Anubose Institute of Technology, paloncha ,India.**

Mr.Chettumala Ch Mohan Rao was born in 1980. He graduated from kakatiya University, warangal in the year 2002. He received M.Tech degree from Jawaharlal Nehre Technological University, Hyderabad in the year 2012. He is presently working as Associate. Professor in the Department of Electrical and Electronics Engineering at **Anubose Institute Of Technology,Paloncha, India.** His research area includes DTC and Drives.