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Design of Area and Power Efficient 5:2 Compressor for High Speed Multipliers

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Abstract- ***The paper proposes architectures of 5:3 compressor designs for low power multiplication purposes. The architecture explores the essence of two transistor multiplexer design and novel two transistor XOR gates for the proposed topology with least number of transistors for logic level implementation. The modified and proposed compressor designs reduce the stage delays, transistor count, PDP (power delay product), EDP (energy delay product) and area by utilizing the combinations of XORXNOR gates, MUX circuits and transistor level implementation contrasted with the conventional designs. Simulation studies have been carried out in 65nm, 90nm, 130nm technologies in Cadence Spectre.***

Index Terms - ***Compressor, Low Power, Layout, Multiplexer, Multiplier, XOR-XNOR***

INTRODUCTION

With the commencement of semiconductor industry, the profound growth is seen in the integration of diversified circuit components in limited silicon area [1]-[13]. The continuous urge for integration of more and more components on minimum area of silicon has galvanized the scientists to employ new trends and techniques. This is to notify the challenging criteria without incurring any overhead and still achieving low power and high speed. Moore's law clearly demonstrated the need of transistors in VLSI design. [1]. Speed, area and power are three thrust areas scrutinized in the literature and endless researches are still going on [2]. Multipliers are the primitive ziggurat block and multiplication is imperative for many DSPs, general purpose processors, and digital filters etc. [3], [4]. With the era of technological advancement, potential for power saving and area is acknowledged from prevailing logic styles to actualize new logic styles at the circuit level. Multiplication is a complex operation and has three stages imbibed with it [5], [6] i.e. 1.) Partial product generation 2.)Partial product reductions 3.)Final carry propagating addition. Second phase being imperative for overall performance of processors, reducing the critical path and minimizing time and power deserves ultimate attention for power proficient design. Compressors being one of the PEs (processing element) are the fundamental building block for accumulation of partial product in multiplication. Compressors dictates the overall critical path of the circuit owing which high speed and reduced power demand is progressively increasing [7]-[9]. This paper constitutes novel compressor architecture replacing XOR gates in critical path with MUX to competently exploit prior output and ameliorate overall performance [10]-[12]. A contemporary study of literature acknowledges the primitive design of 5:3 compressor using full adders and half adder shown in figure 1(a). Further optimization of 5:3 compressor is exhibited in S. Chowdhury, A. Banerjee and H. Sahatopology in figure 1(b) [13].

The current work presents two architectures of 5:3 compressor suitably mutated to minimize the stage delay, power dissipation and area in two ways. Firstly, employing two transistor 2x1 multiplexer in lieu of XOR gates diminishing the critical path delay. Secondly, proposing a novel design of two transistor

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XOR gates for minimum silicon area epitomizing global enrichment of performance.

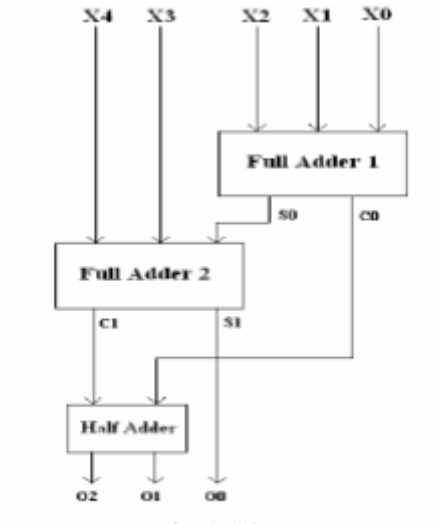

Fig. 1. (a)

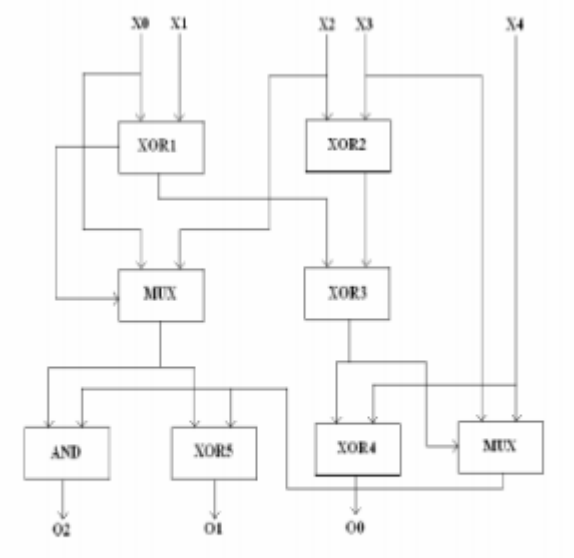

Fig. 1. (b)

Fig 1. Architecture of conventional designs of 5:3 compressor

In order to gain independence of design, they have been implemented in three technologies viz. 65nm, 90nm and 130nm. The power delay and energy delay product simulations are also carried out which is found to be less than its peer designs. The paper is organized as follows: Section 2 represents the topologies of 2x1 multiplexers and novel two transistor XOR gates. Section 3 exhibits the architecture of 5:3 compressors. Section 4 is entitled with the schematic view of the logic style in Cadence Spectre. The performance evaluation is done in section 5 carried forward with layout view in section 6. The conclusion has been enumerated in section 7 followed by acknowledgement in section 8.

II. MUX vs XOR-XNOR

The prevalent topology of MUX and XOR-XNOR circuits over the decade are shown in figure 2(a) and 2(b) [10]

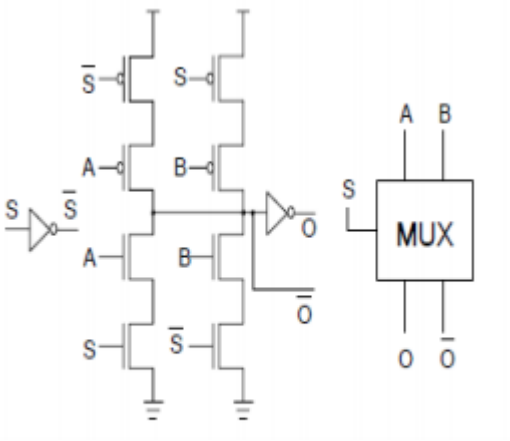

Fig. 2. (a)

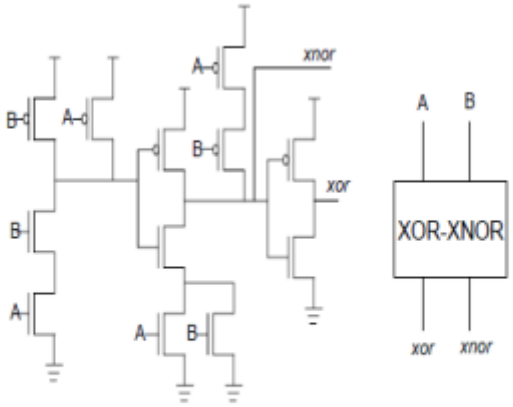

Fig. 2. (b)

Fig 2. CMOS Implementations of (a) MUX (b) XOR-XNOR

In figure 2(a), it is evident that transistor switching is formerly attained if both select bit and complement bit alight before the input, advancing towards reduction of global delay of the circuit [10]. Thus, eliminating

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additional inverter stage giving way to low power consumption and area [14]. The alternative topology for 2x1 multiplexer valued in the paper is shown in figure 3 with A, B as inputs and S as select line which is faster and consumes lesser power than other CMOS design [10].

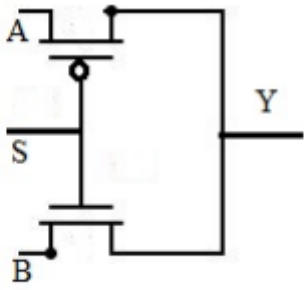

Fig 3. Two transistor 2x1 multiplexer design

The paper formalizes a novel design of two transistor XOR gate which obtain logic values by modifying the value of bulk terminal i.e. V_{sb} [15] which changes V_{th} of the circuit as shown in figure 4 in 65nm technology. For A=0, B=1 and A=1, B=0 we elicit logic high values from the circuit. The governing equation for V_{th} exhibiting relation between channel length, V_{th} and V_{sb} is shown in equation 1 below:

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + \phi_0} - \sqrt{\phi_0}\right) - \alpha_v \frac{t_{ox}}{L} V_{DS} + \alpha_w \frac{t_{ox}}{W}(V_{SB+}\phi_0) \quad ..1$$

Where,

V_{T0}: zero bias threshold voltage

γ : Bulk threshold coefficient,

V: Bulk Potential,

ϕ_0: Fermi potential,

t: The thickness of the oxide layer

α_v: process dependent parameters.

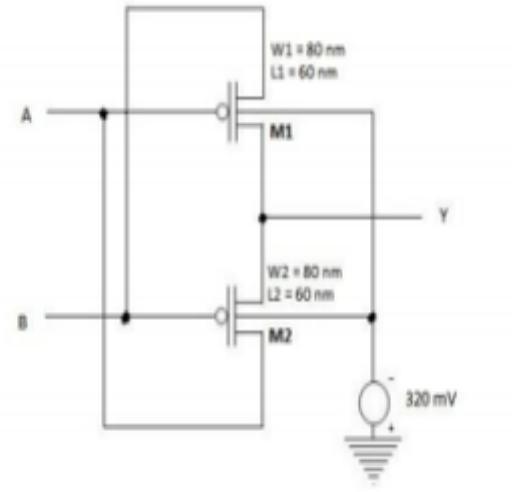

Fig 4. Novel design of two transistor XOR gate in 65nm technology

For A=1 and B=1, both PMOS are off and the circuit goes to high impedance state. So, from equation (1), it is evident that changing values of W, L and V_{sb} varies the logic levels of XOR gate. A 320mV reverse bias supply is thus employed to bring down the logic value to logic low. Figure 5, shows the simulation results of 2T XOR gates in Cadence. The waveform shows how logic values varies at different reverse bias voltages i.e. 270mV and 320mV with the change in V_{th} .With increase in reverse bias voltage value, Vth is increased and V_{dd}-V_{th} at A=1 and B=1 goes to logic low values

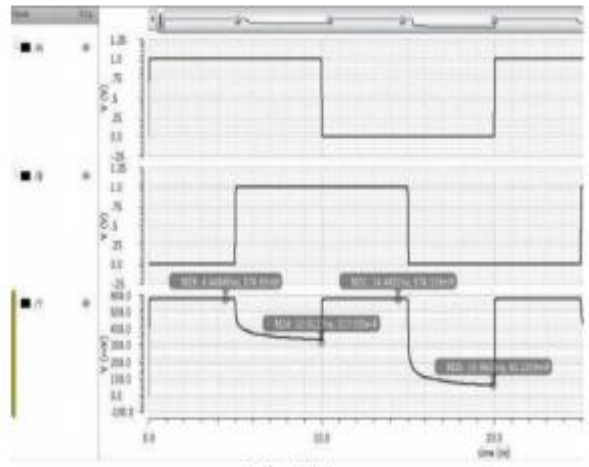

Fig 5(a)

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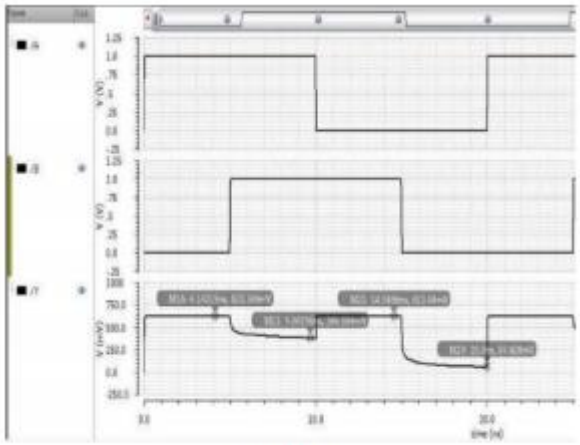

Fig 5(b)

The simulations for two transistor XOR gate is carried out at 50MHz frequency and 50ps rise and fall times.

III. ARCHITECTURE OF 5:3 COMPRESSOR

A combinational logic circuit of 5:3 compressor is a topology accepting five inputs and generating three outputs. The five input bits are summed up to produce the three bit output. The conventional design of 5:3 compressor is an enhanced version of 4:2 compressor [16], [17], [18] and can have maximum value of 101 when all the three bits are 1. The conventional blueprint of 5:3 compressors are shown in figure 1. Figure 1(a) is a straightforward approach which leads to five stage delays and the up-gradation in figure 1(b) [13] entails three stage delays. The current work encounters the involvement of 2x1 multiplexer substituting XOR gates at second and third stages producing output proportionally decreasing critical path delay. Moreover, the architecture has profound role in decreasing the PDP, EDP and area. The design of 5:3 compressor has been derived by suitably altering the Boolean equations as follows:

$$O_o = x_0 \oplus x_1 \oplus x_2 \oplus x_3 \oplus x_4$$
$$= (x_0 \oplus x_1 \oplus x_2 \oplus x_3).\overline{x_4} + \overline{(x_0 \oplus x_1 \oplus x_2 \oplus x_3)}.\, x_4$$
$$= [(x_0 \oplus x_1).\overline{(x_2 \oplus x_3)} + \overline{(x_0 \oplus x_1)}.(x_2 \oplus x_3)].\overline{x_4} + [\overline{(x_0 \oplus x_1).\overline{(x_2 \oplus x_3)} + \overline{(x_0 \oplus x_1)}.(x_2 \oplus x_3)}].x_4$$

……2

$$O_1 = ((x_0 \oplus x_1 \oplus x_2 \oplus x_3).x_4 + \overline{(x_0 \oplus x_1 \oplus x_2 \oplus x_3)}.x_3) \oplus ((x_0 \oplus x_1).x_2 + \overline{(x_0 \oplus x_1)}.x_0)$$

……3

$$O_2 = ((x_0 \oplus x_1 \oplus x_2 \oplus x_3).x_4 + \overline{x_0 \oplus x_1 \oplus x_2 \oplus x_3}).x_3) \oplus ((x_0 \oplus x_1).x_2 + \overline{(x_0 \oplus x_1)}.x_0)$$

……4

The proposed architectures are based on equations (2), (3) and (4).

Figure 6, is the modified version of 5:3 compressor encountered in figure 1(b) reducing the critical path delay by incorporating two transistor 2x1 multiplexers substituting the XOR gates. Additionally, there is reduction in transistor count, PDP and EDP. It also shows a unique representation of 5:3 compressor blending novel 2T XOR gate and two transistor 2x1 MUX presenting pioneer state-of-art in the design. Experimentally, the radical changes portrays an optimized design with high speed and low power. The W/L ratiosare minimum for XOR gates and 5/1 for multiplexer. The reverse-biased voltages are adjusted according to desired logic levels in the design in different technologies. MUX* is the block incorporating the inverter stage.

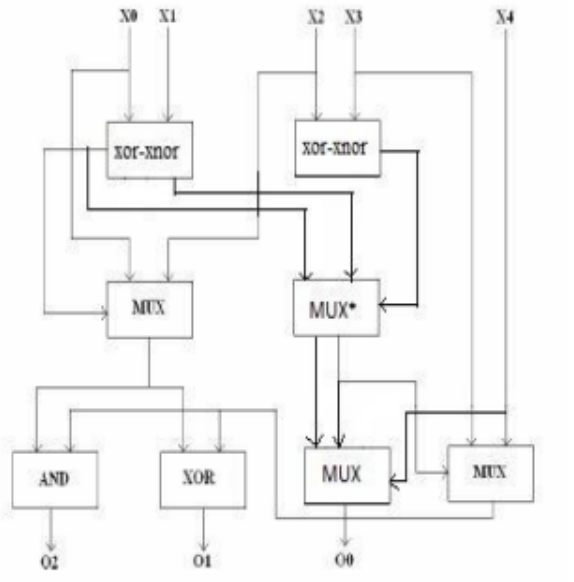

Fig 6. Architecture of proposed 5:3 compressor

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IV. CIRCUIT DESIGN OF 5:3 COMPRESSORS

The architectures have been designed and simulated in Cadence Spectre in 65nm, 90nm and 130nm technologies. The schematic blueprint of modified and proposed design is as shown in figure 7.

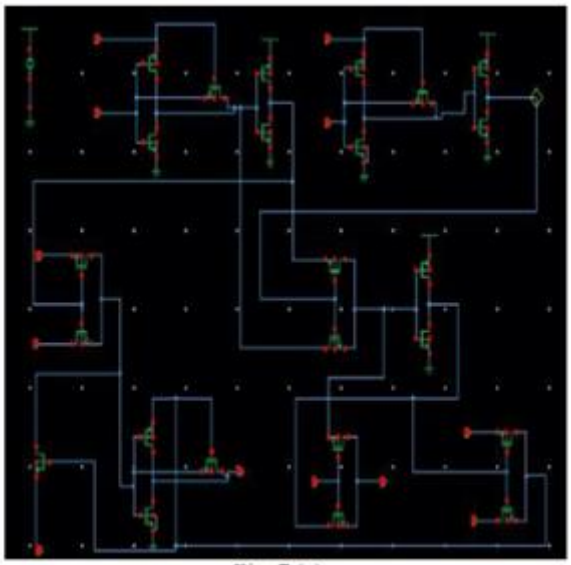

Fig. 7 (a)

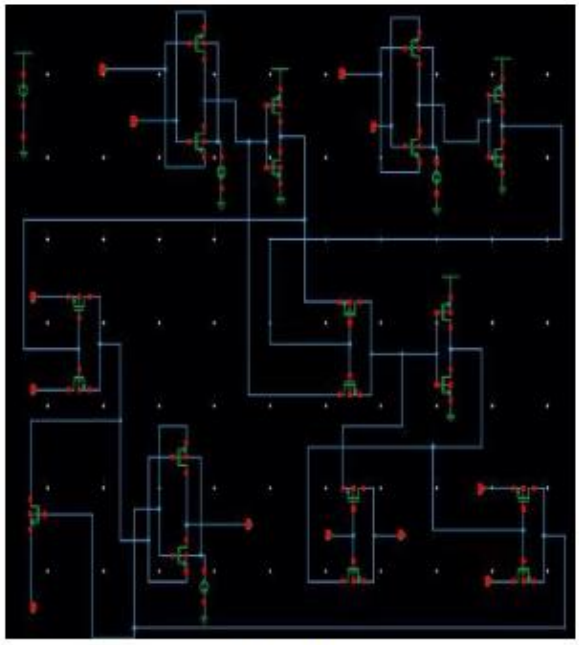

Fig. 7 (b)

Fig 7. Schematic view of 5:3 compressors

(a) 3T XOR and 2T 2x1 MUX compressor

(b) 2T XOR and 2T 2x1 MUX compressor

V. SIMULATION AND PERFORMANCE ANALYSIS OF 5:3 COMPRESSOR DESIGNS

With the view of evaluating and comparing the performance of proposed designs with previously reported 5:3 compressor in fig 1(b)(3 transistor XOR and 6 transistor MUX compressor) [13], exhaustive simulation studies has been carried out with respect to number of transistors, delay, power dissipation, PDP, EDP and area. The circuits are simulated under same testing conditions and the response of outputs at four different input patterns is studied. All the assessment and estimation has been executed in 65nm, 90nm and 130nm technologies. The simulations are carried out at 2.5 MHz frequency with rise and fall times of 50 ps. The power delay product is the product of average power and average delay. Computation of energy delay product is multiplication of PDP by average delay [19]. The simulated outcome is exhibited in TableI.

TABLE I - SIMULATION RESULTS OF DIFFERENT 5:3 COMPRESSORS

Technology	Type of Compressor Circuit	No of transistors	Delay (ns)	Power (nW)	PDP(10^{-18}) (J)	EDP(10^{-27}) (Js)
130nm	Conventional(fig.1(b))[13]	28	1.371	2070	2837.97	3890.857
130nm	3T XOR-2T 2x1 MUX	24	0.811	463.710	376.0688	304.991
130nm	2T XOR-2T 2x1 MUX	21	1.207	154.460	186.433	225.024
90nm	Conventional(fig.1(b))[13]	28	0.870	1305	1135.350	987.754
90nm	3T XOR-2T 2x1 MUX	24	0.578	227.800	131.668	76.104
90nm	2T XOR-2T 2x1 MUX	21	0.721	128.170	92.414	66.630
65nm	Conventional(fig.1(b))[13]	28	0.604	1220	736.880	445.075
65nm	3T XOR-2T 2x1 MUX	24	0.477	155.706	74.271	35.427
65nm	2T XOR-2T 2x1 MUX	21	0.553	92.840	51.340	26.984

The table indicates that the delay of 3T XOR and 2T 2x1 MUX 5:3 compressor is less as contrasted with 2T XOR and 2T 2x1 MUX 5:3 compressor, but the

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power dissipation is approximately half, giving way to reduced PDP and EDP. The trade-off of power and delay has been found in other peer designs of literature. [20]. A contrastive study of silicon area is done for proposed designs and conventional design. The result obtained is assimilated in Table II.

TABLE II - COMPARATIVE STUDY OF THE AREA OF THE DIFFERENT COMPRESSORS

Type of design	Technology	Area (μm^2)
Conventional(fig.1(b))[13]	130nm	278.141
3T XOR-2T 2x1 MUX	130nm	204.491
2T XOR-2T 2x1 MUX	130nm	181.249
Conventional(fig.1(b))[13]	90nm	220.065
3T XOR-2T 2x1 MUX	90nm	153.960
2T XOR-2T 2x1 MUX	90nm	131.953
Conventional(fig.1(b))[13]	65nm	76.497
3T XOR-2T 2x1 MUX	65nm	61.425
2T XOR-2T 2x1 MUX	65nm	45.578

VI. LAYOUT DESIGN OF PROPOSED 5:3 COMPRESSOR ARCHITECTURES

The layout of 5:3 compressor architectures in two configuration is designed and simulated. Figure 8 shows the layout view of the two designs in 90nm technology in Cadence Virtuoso Spectre. The layout is designed with lowest interconnect density leading to low power consumption [21]. The layout is built symmetric by placing n-wells appropriately with big sized PMOS transistors with proper orientation of substrates.

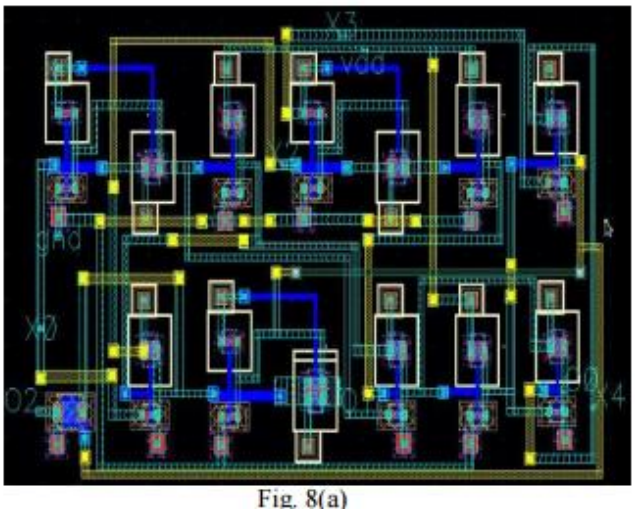

Fig. 8(a)

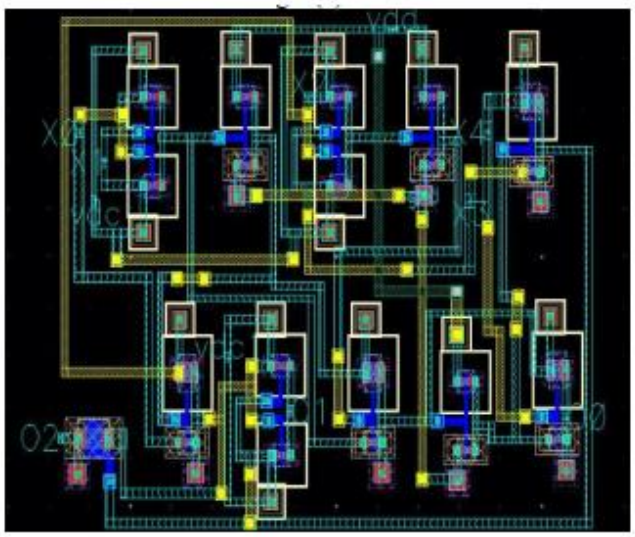

Fig. 8(b)

Fig 8. Layout view of proposed 5:3 compressors in 90nm technology

(a) 3T XOR and 2T 2x1 MUX
(b) 2T XOR and 2T 2x1 MUX

VII. CONCLUSION

The current work the design, simulation and layout view of novel 5:3 compressors. The work encompasses in implementation of compressors by engaging multiplexers superseding the XOR gates. Thus, governing the reduction of critical path delay and reducing transistor count by employing novel 2T XOR gates. The design utilizes least number of transistors for the logic level implementation of compressors in different technologies and comparison is done at all levels- delay, power, PDP, EDP and area. The layout has also been designed and simulated.

VIII. Acknowledgement

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