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Design and Implementation of Current-Mode Multiplier/Divider Circuits in Analog Processing

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***Abstract*—**This project presents two original implementations of improved accuracy current-mode multiplier and divider circuits. Besides the advantage of their simplicity, these original multiplier and divider structures present the advantage of very small linearity errors that can be obtained as a result of the proposed design techniques (0.9% and 0.75%, respectively, for an extended range of the input currents). The original current mode multiplier and divider circuits permit a facile reconfiguration, the presented structures representing the functional basis for implementing complex function synthesizer circuits. The proposed computational structures are designed for implementing in 0.18-μm Complex Metal Oxide Semi-conductor technology (i.e., CMOS Technology), with a low-voltage operation (a supply voltage of 1.2 V). The circuits' power consumptions are 60 and 75 μW, respectively, while their frequency bandwidths are 59.7 and 79.6 MHz, respectively.

I. INTRODUCTION

Signal processing circuits find a multitude of applications in many domains such as telecommunications, hearing devices, medical equipment, and disk drives etc., the preference for an analog approach of signal processing systems being mainly motivated by their high speed and low-power operation that allows a real-time signal processing. Multiplier circuits represent intensively used blocks in analog signal processing structures. The motivation for designing these computational structures is related to their extremely wide range of applications in analog signal processing, such as frequency translation, adaptive equalization, curve-fitting generators and waveform generation, automatic gain control, squaring and square rooting, amplitude modulation, rms-dc conversion, neural networks, and Very Large Scale Integrated adaptive filters, or measurement equipment. Based on sub-threshold operated Metal Oxide Semi-conducter transistors, the realization of current mode multiplier and dividers requires simple architectures. In order to improve the frequency response of the computational structures and to increase their −3 dB bandwidth, many analog signal processing functions can be achieved by exploiting the squaring characteristic of Metal Oxide Semi-conductor transistors biased in saturation. In, current mode multiplier the structures were presented with single-ended input voltages, the linearization of their characteristics being obtained using proper squaring relations between the input potentials. To implement the multiplication of two differential-input voltages, in current mode multiplier circuits were described using mathematical principles, similar to the methods used for current mode multipliers with single input voltages. The biasing of the multiplier differential core at a current equal to the sum of a constant component and a current proportional to the square of the differential input voltage was presented in multipliers and dividers and allows us to obtain a linear behavior of the implemented multiplier circuits. In another class of multipliers and dividers, currents are used as input variables. In this case, the designed circuits present the advantage of an independence of the circuit performances on technological errors. These circuits can implement, based on the same configuration, both

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dividing and multiplying functions. Multiplier structures were also reported with increased linearity, designed using different mathematical principles.

II. THEORETICAL ANALYSIS

Two original implementations of current-mode multiplier and current-mode divider structures will be presented. The main aim of the proposed designs is related to the accuracy of implemented functions in both multiplier and divider structers. The current-mode approach of the multiplier and divider circuits strongly increases their frequency response. A further advantage is independence of the computational circuits, output currents on technological parameters is that it contributes to an important increase in the accuracy of the multipliers and dividers. Additionally, the operation of the proposed circuits is not affected by the temperature variations.

A. First Multiplier/Divider Circuit

The first original proposed implementation of a current-mode multiplier and divider circuit is presented in below figure.

The equations of the functional loops containing M1, M2, M3, and M4 gate-source voltages and, respectively, M1, M2, M6, and M7 gate-source voltages can be expressed as follows:

$$2V_{GS}(I_2) = V_{GS}(I_{D1,2}) + V_{GS}\left[I_{D1,2} + 2(I_1 \mp I_O)\right]$$

Considering the squaring characteristics of Metal Oxide Semi-conductor transistors biased in the saturation region

$$I_{D1,2} = I_2 - (I_1 \mp I_O) + \frac{(I_1 \mp I_O)^2}{4I_2}.$$

The expression of the output current will be

$I_{OUT} = I_{D2} - I_{D1} + 2I_O$, resulting in $I_{OUT} = I_O I_1 / I_2$. So, the circuit implements the multiplying and dividing function, having the advantage of an independence of the output current expression on technological parameters and of a circuit operation that is not affected by temperature variations. The aspect ratios of Metal Oxide Semi-conducter transistors . The chip area of the multiplier and divider implemented in 0.18-μm Complex Metal Oxide Semi-conductor technology, shown in below figure, equals approximately 600 μm2 (including pads).

B. Second Multiplier/Divider Circuit

The second original realization of the multiplier and divider circuit is presented in below Figure. The equation of the functional loop containing M1, M2, M4, and M5 gate-source voltages can be expressed as follows:

$$2V_{GS}(I_2) = V_{GS}(I_{OUT1}) + V_{GS}\left[I_{OUT1} + 2(I_1 + I_O)\right]$$

From above equation we get,

$$I_{OUT1} = I_2 - \frac{2(I_1 + I_O)}{2} + \frac{4(I_1 + I_O)^2}{16I_2}.$$

A similar expression can be obtained for the *I* OUT2 current, replacing in (4) the *(I*1 + *IO)* current with *(I*1 − *IO)* current. The expression of the output current of the multiplier/divider circuit from is

$I_{OUT} = I_{OUT1} - I_{OUT2} + 2I_O$, resulting

$I_{OUT} = (I_O I_1)/I_2$.

The chip area of the multiplier and divider implemented in 0.18-μm Complex Metal Oxide Semi-conductor technology, shown in below Figure equals approximately 800 μm2 (including pads). The negative feedback loops that enforce M8 and M18 transistors and, respectively, M4 and M15 transistors to have the same current are stable, since their speed is suitable for obtaining designed circuits the for the requested frequency response.

C. Errors Introduced by Second-Order Effects

The most important errors introduced in the multiplier and divider circuit operations are represented by the channel effect modulation, mismatches, mobility degradation, and body effect. As a result of these undesired effects, the proper functionality of previous circuits will be affected by additional errors.

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Additionally, a multitude of specific design techniques exist that are able to compensate the errors introduced by the second-order effects. The practical realization of trans-linear loops using common-centroid Metal Oxide Semi-conductor transistors strongly reduces the errors introduced by the mismatches between the corresponding devices. The design of current mirrors using configurations which are cascade allows an important reduction of the errors caused by the channel length modulation. In this situation, a trade-off between the impact of the second-order effects and the minimal value of the supply voltage must be performed. Because the bulks of an important number of Metal Oxide Semi-conductor transistors can be connected to their source, the errors introduced by the bulk effect can be cancelled out for these devices.

D. Small-Signal Frequency Response of Multiplier/Dividers

The multiplier and divider circuit proposed is designed for allowing a high bandwidth. In order to achieve this aim, there exists a single high-impedance node, noted as A, which will impose the maximal frequency of operation. The frequency response of the multiplier and divider circuit presented is poorer than the frequency response of the circuit, because there exists three high-impedance nodes (A, B, and C). As most of the nodes in a circuit represent low-impedance nodes, it is expected that the proposed circuits to have relatively high maximal frequencies of operation.

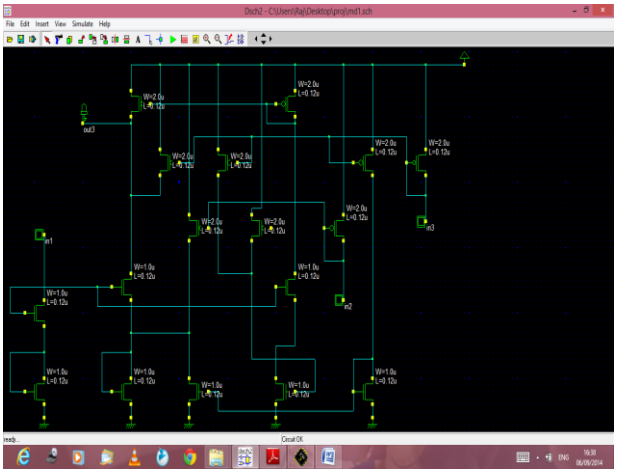

Fig: First implementation of the multiplier and divider circuit.

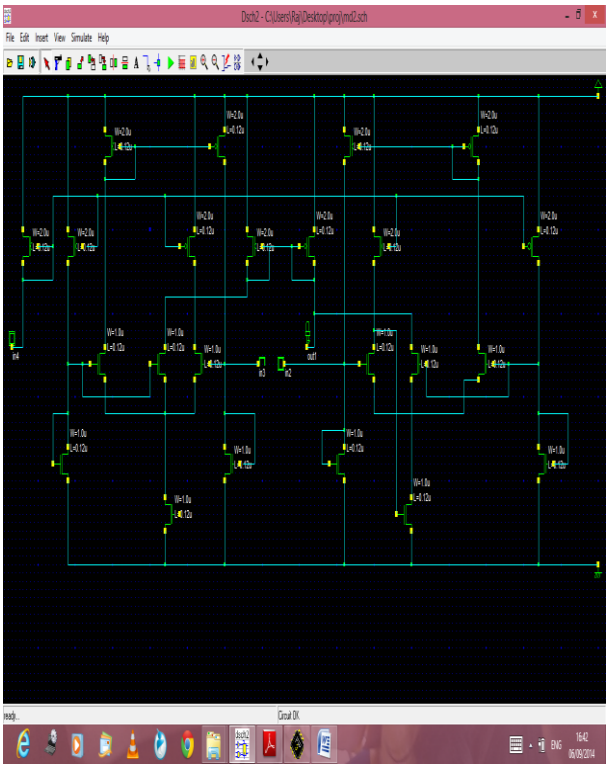

Fig: Second implementation of the multiplier and divider circuit.

III. SIMULATED RESULTS

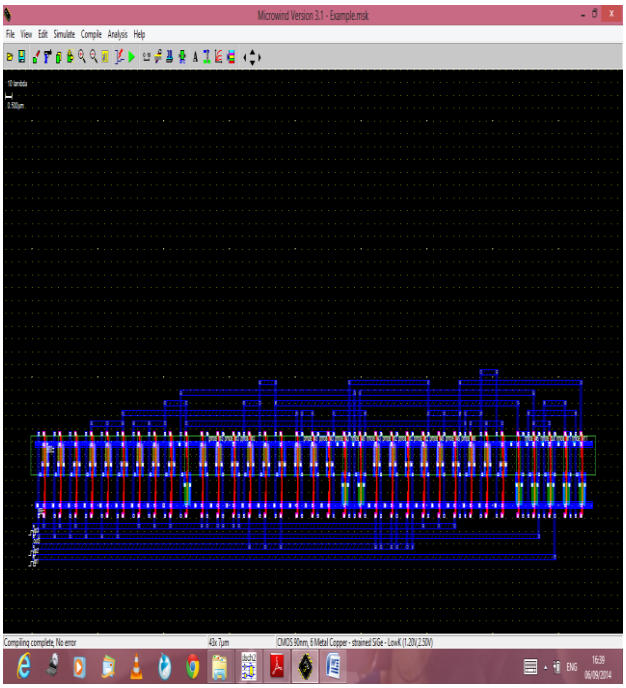

Fig: First implementation lay out diagram of the multiplier and divider circuit.

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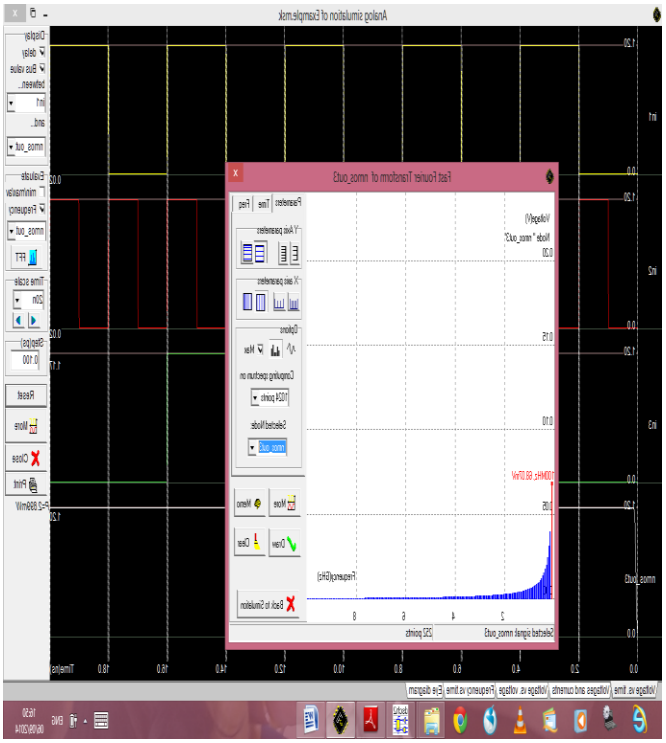

Fig: First implementation V vs I of the multiplier and divider circuit with FFT

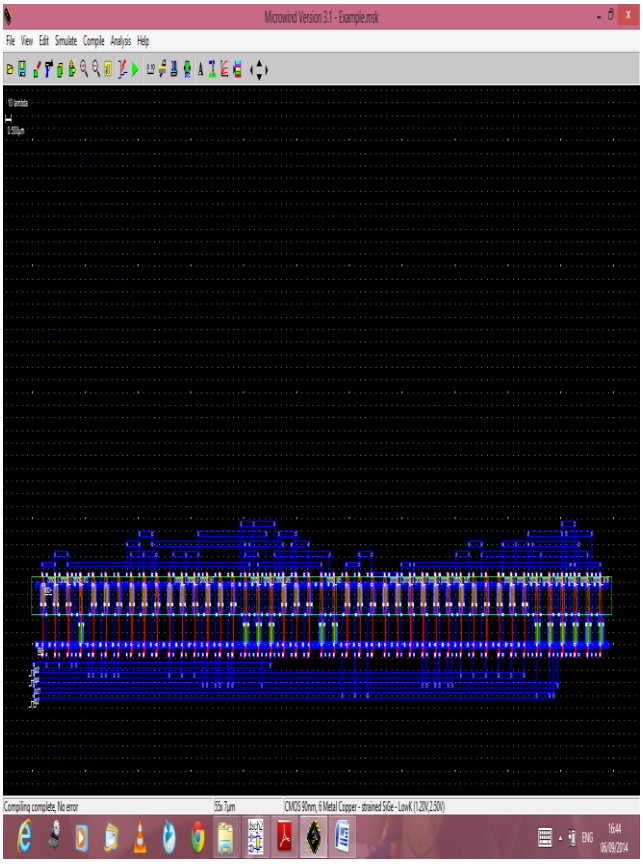

Fig: Second implementation lay out diagram of the multiplier and divider circuit

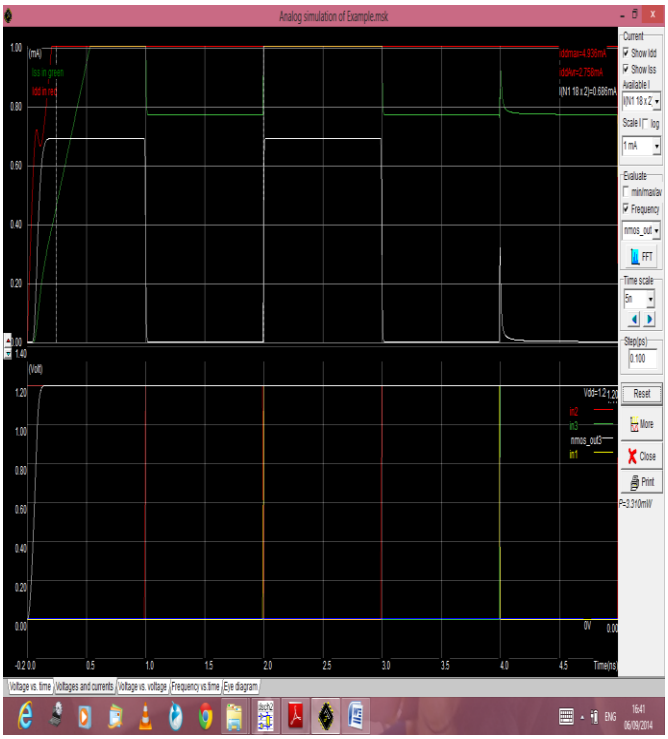

Fig: First implementation V vs I of the multiplier and divider circuit

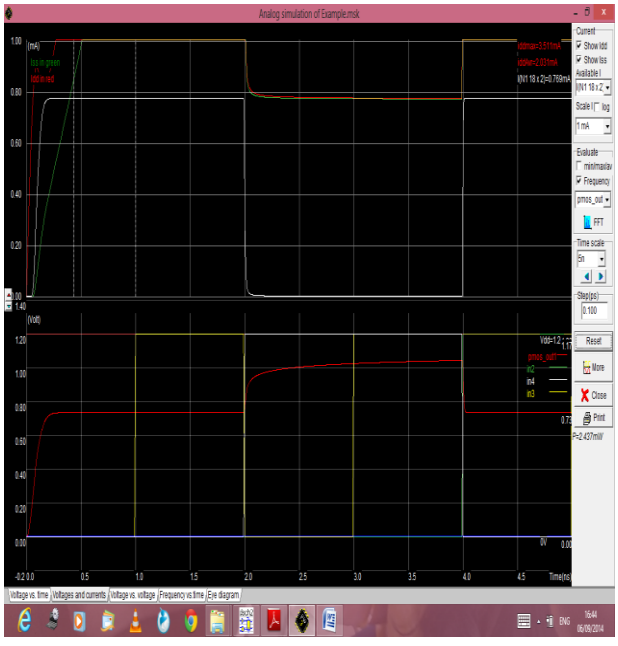

Fig: Second implementation V vs I of the multiplier and divider circuit

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IV. CONCLUSION

Here we are implementing original accuracy improved the two multiplier and divider circuits. The current mode operation of the multiplier and divider circuits improves the accuracy of the circuits and the proposed designs improve the performance of the module. The proposed multiplier and divider circuits have the less linearity errors. The proposed system designed in the 0.18um technology and it takes the minimal voltage 1.2v. The most important factor that contributes to the small value of the minimal supply voltage is represented by the proposed designs of the multiplier/divider circuits, works with low-voltage operation.

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