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32 BIT×32 Bit Razor-Based Dynamic Voltage Scaled Multi Precision Multiplier

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ABSTRACT

In this paper, we present a multi precision (MP) reconfigurable multiplier that incorporates variable precision, parallel processing (PP), razor-based dynamic voltage scaling (DVS), and dedicated MP operands scheduling to provide optimum performance for a variety of operating conditions. All of the building blocks of the proposed reconfigurable multiplier can either work as independent smaller-precision multipliers or work in parallel to perform higher-precision multiplications. Given the user's requirements (e.g., throughput), a dynamic voltage/ frequency scaling management unit configures the multiplier to operate at the proper precision and frequency. Adapting to the run-time workload of the targeted application, razor flip-flops together with a dithering voltage unit then configure the multiplier to achieve the lowest power consumption. The single-switch dithering voltage unit and razor flip-flops help to reduce the voltage safety margins and overhead typically associated to DVS to the lowest level. The large silicon area and power overhead typically associated to re configurability features are removed. Finally, the proposed novel MP multiplier can further benefit from an operands scheduler that rearranges the input data, hence to determine the optimum voltage and frequency operating conditions for minimum power consumption

Index Terms—Computer arithmetic, dynamic voltage scaling, low power design, multi-precision multiplier.

I.INTRODUCTION

Consumers demand for increasingly portable yet high performance multimedia and communication products imposes stringent constraints on the power consumption of individual internal components Of these, multipliers perform one of the most frequently arithmetic This spurious switching activity can be mitigated by balancing internal paths through combination of architectural and transistor-level optimization techniques . In addition to internal path delays, dynamic power reduction can also be achieved by monitoring the effective dynamic range of the input operands .so as to disable unused sections of the multiplier truncate the output product at the cost of reduced precision. This is possible because, in most sensor applications, the actual inputs do not always occupy the entire magnitude of its word-length.

II.EXISTING SYSTEM

Today's full-custom DSPs and application specific integrated circuits (ASICs) are designed for a fixed maximum word-length so as to accommodate the worst case scenario. Therefore, an 8-bit multiplication computed on a 32-bit Booth multiplier would result in unnecessary switching activity and power loss. Several works investigated this word length optimization. Each pair of incoming operands is routed to the smallest multiplier that can compute the result to take advantage of the lower energy consumption of the smaller circuit. This ensemble of point systems is reported to consume the least power but this came at the cost of increased chip area given the used ensemble structure. Combining multi precision (MP) with dynamic voltage scaling (DVS) can provide a dramatic reduction in power consumption by adjusting the supply voltage according to circuit's run-time workload rather than fixing it to cater for the worst case scenario. When adjusting the voltage, the actual performance of the multiplier running under scaled

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voltage has to be characterized to guarantee a fail-safe operation.

III. SYSTEM OVERVIEW AND OPERATION

The proposed MP multiplier system comprises five different modules that are as follows:

1) The MP multiplier;

2) The input operands scheduler (IOS) whose function is to reorder the input data stream into a buffer, hence to reduce the required power supply voltage transitions;

3) The frequency scaling unit implemented using a voltage controlled oscillator (VCO). Its function is to generate the required operating frequency of the multiplier;

4) The voltage scaling unit (VSU) implemented using a voltage dithering technique to limit silicon area overhead. Its function is to dynamically consumption generate the supply voltage so as to minimize power

5) The dynamic voltage/frequency management unit (VFMU) that receives the user requirements (e.g., throughput).

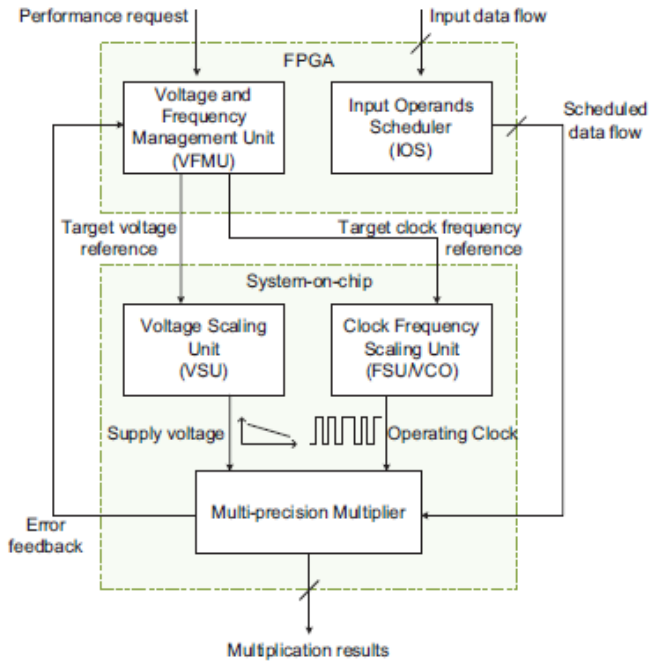

Fig. 1. Overall multiplier system architecture.

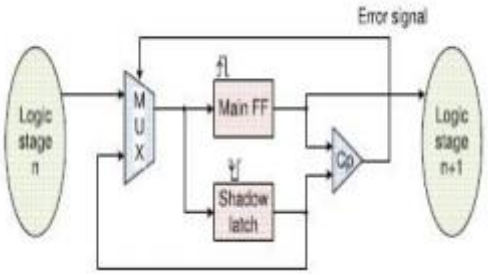

Fig. 2 Conceptual view of razor flip-flop.

The razor technology is a breakthrough work, which largely eliminates the safety margins by achieving variable tolerance through in-situ timing error detection and correction ability .This approach is based on a razor flip-flop, which detects and corrects delay errors by double sampling. The razor flip-flop operates as a standard positive edge triggered flip-flops coupled with a shadow latch, which samples at the negative edge. Therefore, the input data is given in the duration of the positive clock phase to settle down to its correct state before being by the shadow latch. The minimum allowable supply voltage needs to be set, hence the shadow latch always clocks the correct data even for the worst case conditions. This requirement is usually satisfied given that the shadow latch is clocked later than the main flip-flop.

IV.PROPOSED SYSTEM

Selected Bit Of Operation Use. Whatever input are given that multiplier bits only operating. Remaining Bits are OFF Condition

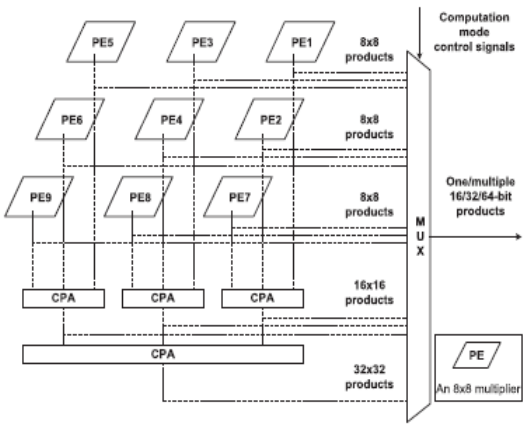

Fig.3: Possible configuration modes of proposed MP multiplier.

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The proposed multiplier (Fig. 3) not only combines MP and DVS but also parallel processing (PP). Our multiplier comprises 8 × 8 bit reconfigurable multipliers. These building blocks can either work as nine independent multipliers or work in parallel to perform one, two or three 16 × 16 bit multiplications or a single-32 × 32 bit operation. PP can be used to increase the throughput or reduce the supply voltage level for low power operation. Fig. 3 shows the benefits of the different approaches being considered. Power consumption is a linear function of the workload, which is normally represented by the input operands precision.

V.DYNAMIC VOLTAGE AND FREQUENCY SCALING MANAGEMENT

Dynamic voltage scaling

Is a power management technique in computer architecture, where the voltage used in a component is increased or decreased, depending upon circumstances. Dynamic voltage scaling to increase voltage is known as overvolting; dynamic voltage scaling to decrease voltage is known as under volting. Under volting is done in order to conserve power, particularly in laptops and other mobile devices,[1] where energy comes from a battery and thus is limited. Over volting is done in order to increase computer performance, or in rare cases, to increase reliability

Dynamic frequency scaling

(also known as CPU throttling) is a technique in computer architecture whereby the frequency of a microprocessor can be automatically adjusted "on the fly," either to conserve power or to reduce the amount of heat generated by the chip. Dynamic frequency scaling is commonly used in laptops and other mobile devices, where energy comes from a battery and thus is limited. It is also used in quiet computing settings and to decrease energy and cooling costs for lightly loaded machines. Less heat output, in turn, allows the system cooling fans to be throttled down or turned off, reducing noise levels and further decreasing power consumption. It is also used for reducing heat in insufficiently cooled systems when the temperature reaches a certain threshold, such as in poorly cooled over clocked systems.

V. RESULTS

Existing system: The below figure.4 shows the simulation results for existing system and the proposed system simulation output results is shown in fig.5

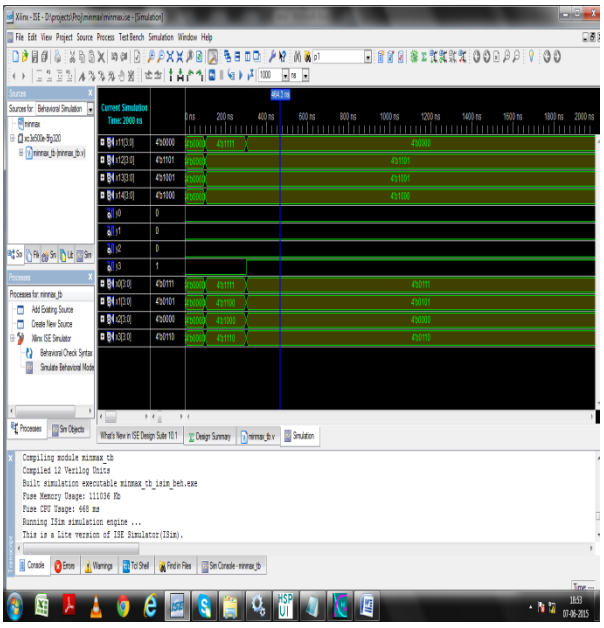

Fig: 4 Existing System output results

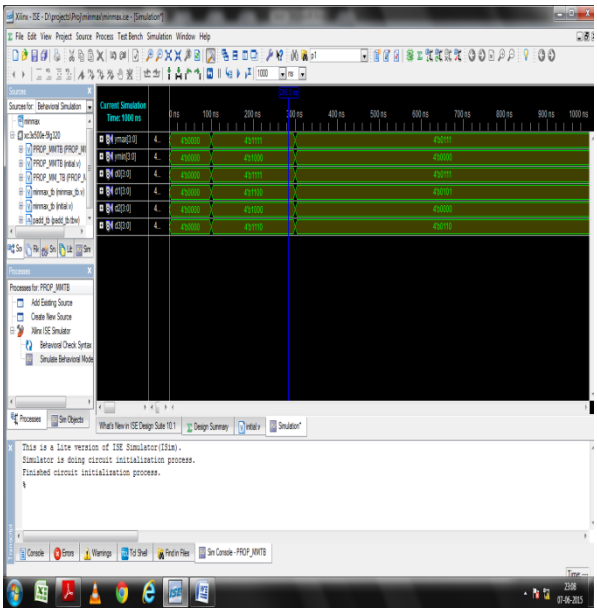

Fig:5 proposed system output results

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Table:1 Comparison Results for existing and proposed system

Design	Slices	4-input LUTs	Delay (nS)	Area Delay Product (nm^2.nSec)
Existing System	28	49	15.321	428.988
Proposed System	11	22	7.458	82.038

VI.CONCLUSION

We proposed a novel MP multiplier architecture featuring, respectively, 28.2% and 15.8% reduction in silicon area and power consumption compared with its 32 × 32 bit conventional fixed-width multiplier counterpart.When integrating this MP multiplier architecture with an error-tolerant razor-based DVS approach and the proposed novel operands scheduler, 77.7%–86.3% total power reduction was achieved with a total silicon area overhead as low as 11.1%. The fabricated chip demonstrated run-time adaptation to the actual workload by operating at the minimum supply voltage level and minimum clock frequency while meeting throughput requirements. The proposed novel dedicated operand scheduler rearranges operations on input operands, hence to reduce the number of transitions of the supply voltage and, in turn, minimized the overall power consumption of the multiplier. The proposed MP razor-based DVS multiplier provided a solution toward achieving full computational flexibility and low power consumption for various general purpose low-power applications.

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