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Power-Quality Improvement with a Voltage-Controlled DSTATCOM

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ABSTRACT:

This paper proposes a new algorithm to generate reference voltage for a distribution static compensator (DSTATCOM) operating in voltage-control mode. The proposed scheme exhibit several advantages compared to traditional voltage-controlled DSTATCOM where the reference voltage is arbitrarily taken as 1.0 p.u. The proposed scheme ensures that unity power factor (UPF) is achieved at the load terminal during nominal operation, which is not possible in the traditional method. Also, the compensator injects lower currents and, therefore, reduces losses in the feeder and voltage-source inverter. Further, a saving in the rating of DSTATCOM is achieved which increases its capacity to mitigate voltage sag. Nearly UPF is maintained, while regulating voltage at the load terminal, during load change. The state-space model of DSTATCOM is incorporated with the deadbeat predictive controller for fast load voltage regulation during voltage disturbances. With these features, this scheme allows DSTATCOM to tackle power-quality issues by providing power factor correction, harmonic elimination, load balancing, and voltage regulation based on the load requirement. Simulation and experimental results are presented to demonstrate the efficacy of the proposed algorithm.

Index Terms—Current control mode, power quality (PQ), voltage-control mode, voltage-source inverter.

INTRODUCTION:

A distribution system suffers from current as well as voltage-related power-quality (PQ) problems, which include poor power factor, distorted source current, and voltage disturbances. A DSTATCOM, connected at the point of common coupling (PCC), has been utilized to mitigate both types of PQ problems. When operating in current control mode (CCM), it injects reactive and harmonic components of load currents to make source currents balanced, sinusoidal, and in phase with the PCC voltages. In voltage-control mode (VCM) , the DSTATCOM regulates PCC voltage at a reference value to protect critical loads from voltage disturbances, such as sag, swell, and unbalances. However, the advantages of CCM and VCM cannot be achieved simultaneously with one active filter device, since two modes are independent of each other. In CCM operation, the DSTATCOM cannot compensate for voltage disturbances.

Hence, CCM operation of DSTATCOM is not useful under voltage disturbances, which is a major disadvantage of this mode of operation. This paper considers the operation of DSTATCOM in VCM and proposes a control algorithm to obtain the reference load terminal voltage. This algorithm provides the combined advantages of CCM and VCM. The UPF operation at the PCC is achieved at nominal load, whereas fast voltage regulation is provided during voltage disturbances. Also, the reactive and harmonic component of load current is supplied by the compensator at any time of operation. The deadbeat predictive controller is used to generate switching pulses. The control strategy is tested with a three-phase four-wire distribution system. The effectiveness of the proposed algorithm is validated through detailed simulation and experimental results.

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Existing System:

Circuit diagram of a DSTATCOM-compensated distribution system is shown in Fig. 1. It uses a three-phase, four-wire, two-level, neutral-point-clamped VSI. This structure allows independent control to each leg of the VSI [7]. Fig. 2 shows the single-phase equivalent representation of Fig. 1. Variable is a switching function, and can be either or depending upon switching state. Filter inductance and resistance are and , respectively. Shunt capacitor eliminates high-switching frequency components. First, discrete modeling of the system is presented to obtain a discrete voltage control law, and it is shown that the PCC voltage can be regulated to the desired value with properly chosen parameters of the VSI. Then, a procedure to design VSI parameters is presented. A proportional-integral (PI) controller is used to regulate the dc capacitor voltage at a reference value.

Proposed System:

The control scheme is implemented using PSCAD software. Simulation parameters are given in Table I. Terminal voltages and source currents before compensation are plotted in Fig. 4. Distorted and unbalanced source currents flowing through the feeder make terminal voltages unbalanced and distorted. Three conditions, namely, nominal operation, operation during sag, and operation during load change are compared between the traditional and proposed method. In the traditional method, the reference voltage is 1.0 p.u., whereas in the proposed method, (32) is used to find the reference voltage.

Nominal Operation

Initially, the traditional method is considered. Fig. 5(a)–(c) shows the regulated terminal voltages and corresponding source currents in phases, and, respectively. These waveforms are balanced and sinusoidal. However, source currents lead respective terminal voltages which show that the compensator supplies reactive current to the source to overcome feeder drop, in addition to supplying load reactive and harmonic currents.

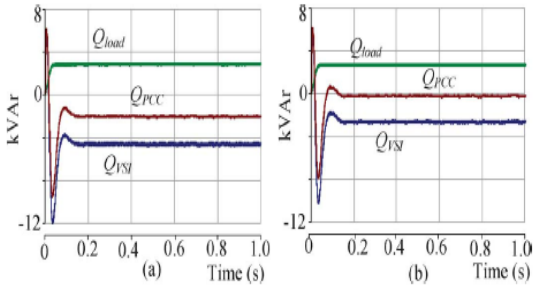

Fig. 8. Load reactive power (Q_{load}), compensator reactive power (Q_{VSI}), and reactive power at PCC (Q_{PCC}). (a) Traditional method. (b) Proposed method.

Operation During Sag

To create sag, source voltage is lowered by 20% from its nominal value at 0.6 s as shown in Fig. 11(a). Sag is removed at 1.0 s as shown in Fig. 11(b). Since voltage regulation capability does not depend upon reference voltage, it is not shown separately for the traditional method. Fig. 11(c) and (d) shows terminal voltages regulated at their reference value. The controller provides a fast voltage regulation at the load terminal. Fig. 11(e) and (f) shows the total dc bus voltage and the load angle, respectively. During the transient period, capacitors supply real power to maintain load power which results in discharging of capacitors.

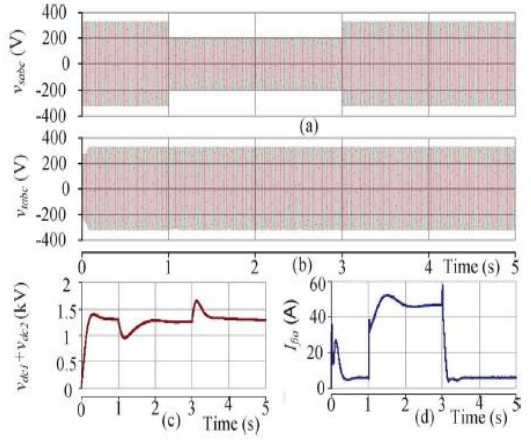

Fig. 12. (a) Source voltages. (b) Terminal voltages. (c) Voltage at the dc bus. (d) Compensator rms current in the proposed method.

Operation During Load Change

To show the impact of load changes on system performance, load is increased to 140%of its nominal value. Under this condition, the traditional method

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gives less power factor as the compensator will supply more reactive current to maintain the reference voltage. The voltage and current waveforms, as shown in Fig. 13(a), confirm this. In proposed method, a load change will result in small deviation in terminal voltage from its reference voltage. Compensator just needs to supply extra reactive current to overcome this small extra feeder drop, hence, nearly UPF is maintained while regulating the terminal voltage at its reference voltage.

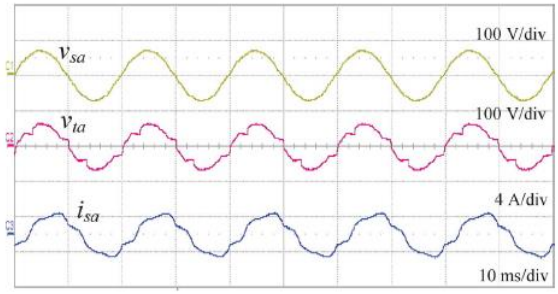

Fig. 14. Experimental results without the compensator.

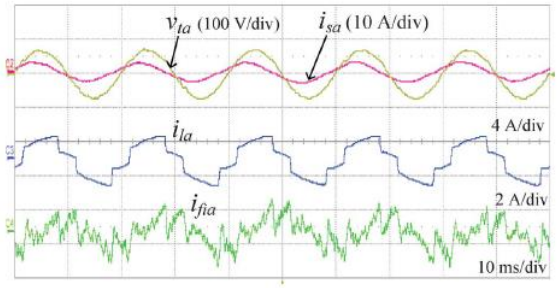

Fig. 15. Experimental results with the traditional scheme.

EXPERIMENTAL RESULTS

The proposed idea and control strategy are experimentally verified on a reduced scale setup. To implement the algorithm, the digital signal processor (DSP) TMS320F2812 interfaced with the host computer is used. Fig. 14 shows the uncompensated waveforms which include source voltage ( ), terminal voltage ( ), and source current ( ). It is seen that the distorted source current flowing through the feeder makes the terminal voltage distorted. First, the DSTATCOM operates with the traditional method and the obtained results are shown in Fig. 15. It shows terminal voltage ( ), source current ( ), load current ( ), and injected current ( ). Here, is sinusoidal even though is distorted, implying that the compensator supplies reactive and harmonic component of. However, it can be noticed that the leads, indicating that the ompensator supplies additional reactive current to overcome feeder drop as well.

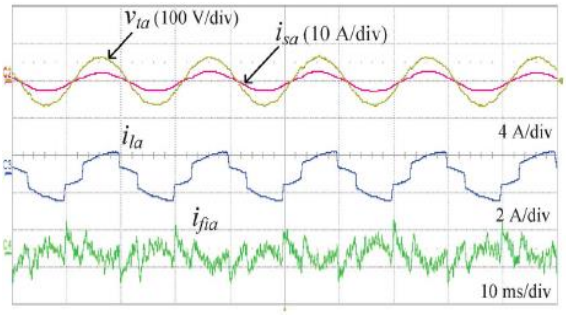

Fig. 16. Experimental results with the proposed scheme.

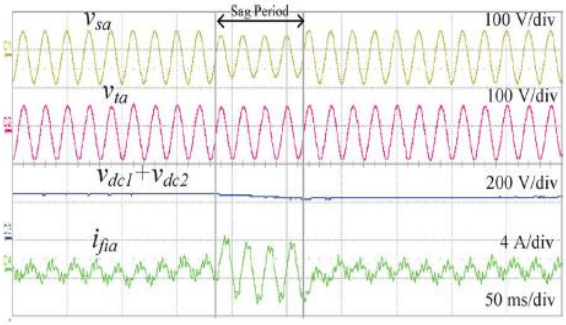

Fig. 17. Experimental results before, during, and after sag.

A voltage sag of 20% is created by using a programmable ac power source. Fig. 17 shows the source voltage, terminal voltage, dc-link voltage, and injected filter current waveforms before, during, and after the sag. It is seen that the terminal voltage is sinusoidal and maintained at the reference voltage before, during, and after the sag without any significant transient. Hence, the proposed scheme is able to provide fast voltage regulation. During voltage sag, the dc link supplies real power to the load which results in discharging of the capacitor; hence, voltage decreases. However, the PI controller acts to bring back voltage at the reference value. Once sag gets cleared, voltage is slowly brought back to its reference by controlling the load angle. Injected filter current ( ) increases rapidly to support the terminal voltage during the sag period, as shown in Fig.17. Injected and source currents will be more when the reference voltage is set

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to 1.0 p.u. It will result in more losses; however, they are not shown here.

CONCLUSION

In this paper, a control algorithm has been proposed for the generation of reference load voltage for a voltage-controlled DSTATCOM. The performance of the proposed scheme is compared with the traditional voltage-controlled DSTATCOM. The proposed method provides the following advantages: 1) at nominal load, the compensator injects reactive and harmonic components of load currents, resulting in UPF; 2) nearly UPF is maintained for a load change; 3) fast voltage regulation has been achieved during voltage disturbances; and 4) losses in the VSI and feeder are reduced considerably, and have higher sag supporting capability with the same VSI rating compared to the traditional scheme. The simulation and experimental results show that the proposed scheme provides DSTATCOM, a capability to improve several PQ problems (related to voltage and current).

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