An Efficient Digital Signal Processing With Razor Based Programmable Truncated Multiplier for Accumulate and Energy reduction

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ABSTRACT

Fault tolerant methods can extend the power savings achievable by dynamic voltage scaling(DVS) by exchanging exactness and/or timing execution against power. Such energy upgrades have a strong dependency on the delay distribution of the circuit and the measurable attributes of the data signal. independently, programmable truncated multipliers likewise accomplish power advantages to the expense of degradation of the output sign to-noise ratio. In this brief, a mix of programmable truncated multiplication is utilized inside of a fault tolerant computerized sign handling (DSP) structure in which the supply voltage is decreased beyond the basic timing level. Timing modulation properties of truncated multiplications are analyzed and exhibited to enhance the execution of fault tolerant designs, reducing error correction burdens, and extending the system operating voltage range. Joining both power techniques brings about lower energy utilization levels, which enhance the vitality savings beyond that normal when applying a mix of both methods with the first DSP.

Keywords—Digital signal processing (DSP), fault tolerant, low power, razor, reconfigurable multiplier, truncated multiplication.

I.INTRODUCTION

Dynamic voltage scaling is widely used as part of strategies to manage switching power consumption in battery powered devices such as cell phones and laptop computers. Low voltage modes are used in conjunction with lowered clock frequencies to minimize power consumption associated with components such as CPUs and DSPs; only when significant computational power is needed will the voltage and frequency be raised.

Voltage scaling provides an effective means to lower power consumption in VLSI circuits, because scaling the supply voltage by a factor of K results in reductions in the dominating dynamic power consumption by a factor of $K2$ and yields static power benefits. However, advances in CMOS technology scaling contributed to an exponential growth of design issues derived from process voltage temperature (PVT) variations, often resulting in conservative designs that lead to a high power consumption.

Some of the classic design timing constraints can be relaxed in digital signal processing (DSP) systems by applying unconventional voltage over scaling (VOS) levels to further improve energy consumption levels while maintaining signal processing performance.

Two of the main streams for providing error-resiliency against timing violations are:

1. Techniques that introduce an estimation or prediction subsystem that monitors the system output and provides an approximation if a fault is detected.
2. Techniques that modify the data capture by augmenting the latches or flip-flops on the critical path and allotting extra execution time for operations that need a long execution time.

Such techniques allow implementation of low power systems with acceptable circuit performance at the

expense of either signal degradation [1], [2], [5], or execution time penalties [3], [4]. Power savings obtained by fault tolerant techniques are dependent on both PVT variations and the circuit physical design, but are also influenced by the data input to the circuit, as the statistical timing distribution defines the percentage of samples estimated and/or corrected, thus conditioning the maximum power savings obtainable using such techniques.

Truncated multiplication has been widely studied as a means of achieving both power and area improvements in the field of arithmetic circuit design, at the expense of signal degradation [6]–[12]. As the truncated multipliers are smaller than full-precision ones, they not only achieve improvements in power consumption and area, but result in different timing distributions. The existence of synergic benefits derived from the combination of truncated multiplication and VOS using a fault tolerance strategy is presented in this brief where both techniques are applied to a custom-designed fixed point multiply and accumulate (MAC) structure.

II.EXISTING SYSTEM

A. *Voltage Scaling Beyond Vdd−crit*

Dynamic power consumption is the dominating component in many arithmetic unit circuits because of the high toggling profile of such structures. The switching component of the energy consumed by a digital gate is defined as Pavg $= \alpha_{0 \to 1} C_L V^2$dd $f$clk, where $\alpha_{0 \to 1}$ is defined as the average number of times in each clock cycle (at a frequency $f$clk) that a node with capacitance C_L makes a power consuming transition. Reducing the supply voltage by a factor of K results in a quadratic improvement in the power consumption rate of CMOS logic.

Scaling of Vdd results in timing penalties which increase as Vdd approaches the threshold voltages of the devices. The relationship between the circuit delay (τ_d) and the supply voltage Vdd is given by $\tau_d = C_L V$dd$/\beta(V$dd $- V_t)\alpha$, where C_L is the load capacitance, β is the gate transconductance, V_t is the

device threshold voltage, and α is the velocity saturation index. We refer to the critical supply voltage of a given architecture Vdd−crit, as the minimum supply voltage where timing on the critical path is met for any expected PVT variations.

Scaling the supply voltage to Vdd $= K \cdot V$dd−crit, where $0 < K < 1$ is referred to as VOS; although this technique results in further energy reductions almost proportional to $K2$, scaling Vdd below the critical supply voltage results in critical timing failures for certain input combinations under certain PVT conditions. This is impractical for use with designs that do not apply fault tolerant schemes.

B. *Razor and Fault Tolerance for Timing*

The Razor technique is an approach to apply dynamic voltage scaling by dynamic detection and correction of circuit timing errors. By measuring the error rate in the circuit, the supply voltage can be tuned while the circuit is in operation, easing the requirements imposed by conservative timing analysis.

Implementation issues of Razor along with its required hardware overhead, where Razor II and Bubble Razor were introduced and tested within a full system with reduced area and timing overheads, and Razor is applied to a high-speed real-time finite-impulse response (FIR) filter. The efficiency of Razor, and the limits regarding Vdd scaling depend on the circuit timing distribution. Therefore, for any circuit implementing Razor, reducing the amount of time required to perform the average and slowest operation will significantly improve Razor merits. This is the motivation for considering the truncated multiplier which exhibits a timing profile different from the standard multiplier.

C. *Truncated Multiplication*

In systems where it is not necessary to compute the exact least significant part of the product, truncated multipliers allow power, area, and timing improvements by skipping the implementation of

sections of the least significant part of the partial product matrix.

Instead of computing the full-precision output, the output is that from the sum of the first $(N + h)$ columns (where $0 \leq h \leq N$), where N is the operand width, plus an estimation of the erased bits. In many applications, product values generated by fixed width $N \times N$ bit multipliers are truncated or rounded back to the original bitwidth in latter stages of the algorithm flow. Truncation allows a way of reducing the complexity of the multiplier unit by replacing the lower parts of the partial product matrix by a smaller compensation circuit, and its variants range from very aggressively truncated applications to faithfully rounded truncated multipliers.

Programmable and configurable approaches to truncated multiplication use fixed-width structures that can be operated at reduced resolutions by disabling parts of the partial product generation. The introduction of programmable truncation in a fixed-point multiplier facilitates modifying not only he multiplier power, but also the timing of the system where the multiplier is embedded. This also alters the original critical path (OCP) of such arithmetic block, making the architecture virtually faster where the active critical path (ACP) $\tau ACP < \tau OCP$. This characteristic of the PTM over the overall and maximum delay is exploited with fault-tolerant schemes to achieve lower minimum energy consumption limits

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III.PROPOSED SYSTEM
PTMAC—A FLEXIBLE LOW-POWER DSP WITH PTM

To extend the usage of PTM to general DSP architectures, the PTMAC was introduced and analyzed. PTMAC, designed as a vehicle to exercise PTM in low-power biomedical applications with a need for modest DSP such as ECG filtering or fall detection, will be utilized in this brief as a platform to

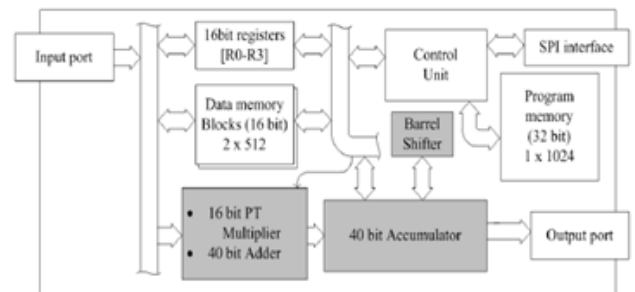combine the benefits of programmable truncation and fault tolerance.

Figure 1: PTMAC top level diagram.

The proposed DSP, as depicted in Figure 1, includes a control unit operating in a five-stage pipeline, program and memory blocks in a multi bus Harvard configuration, some I/O connectivity and an arithmetic unit consisting of a MAC structure with a 16-bit PTM,a 40-bit accumulator, and a 40-bit barrel shifter for scaling and rotating the accumulated value. The total gate count of the original PTMAC chip is 48 k, and it is estimated (post synthesis) to have a maximum power consumption of 79.46 μW/MHz.

Timing analysis of the proposed PTMAC architecture indicates that the critical path is located within the MAC structure of the arithmetic unit; therefore, energy savings derived from the application of voltage scaling approaches will be constrained by the signal propagation time through the arithmetic unit. An experimental approach to combine the delay-modulation capabilities of programmable truncation and the benefits of fault tolerance is explored in the following sections as a way to achieve a flexible unit that trades energy for signal and performance degradation.

IV.RAZOR-BASED PTMAC, LOW-POWER DSP VIA DELAY MODULATION

The combination of a PTM and a fault tolerant system allows such a system to modulate the average and maximum delay times in the MAC unit at run time. Therefore, the number of errors that need correction at any *V*dd level can be trimmed down by reducing the multiplier accuracy. This technique also enables lower

functional *Vdd* values that can be applied before nonrecoverable failures appear in the system, delivering lower optimum operation voltages which result in lower energy expenditure levels.

To explore the independent benefits and interactions between fault tolerance and truncated multiplication, Razor PTMAC was designed as an evolution of PTMAC. To that end, a Razor-enabled version of the original DSP was designed and implemented using Cadence RTL Compiler and TSMC 90 nm technology.

Razor Implementation

To achieve the fault tolerance, the accumulator unit of the PTMAC was replaced by a fault tolerant version named Razor Accumulator where the original flip-flops were substituted by a version of the Razor registers.

The proposed augmented cells were designed and stored as library cells for postsynthesis insertion. Such a cell follows the original implementation Razor implementation, replacing the shadow latch within the Razor registers with a shadow-flip-flop to avoid synthesis issues. The metastability detector required in Razor implementations was modeled as the delay of an inverter added as a constraint to the hold time of the Razor accumulator. In this way, all timing violations potentially causing metastability are then detected as timing errors, providing a lower bound for the performance of Razor.
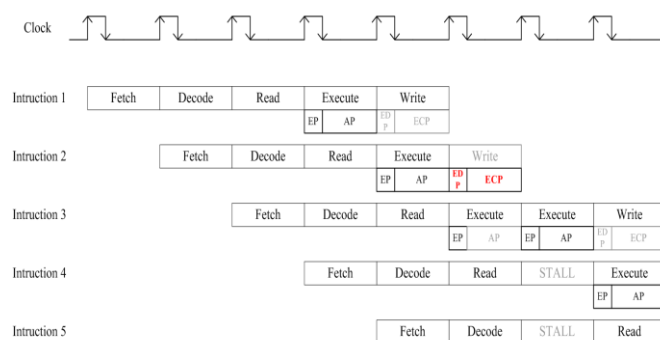
Static timing analysis of PTMAC demonstrated that the only registers situated at potentially critical paths within PTMAC were located in the accumulator, as the multiplication and accumulation of the input data is performed within a clock cycle. Therefore, flipflops capturing the 10 most significant bits of the accumulator were replaced by Razor flip-flops. Insertion of the Razor flip-flops and the associated control logic resulted in an increase of 18% of the core area.

Since the hold constraint only limits the maximum duration of the positive clock phase and does not affect the clock frequency, a single clock was utilized to drive both main and razor flip-flops with both transition edges providing flexibility to configure the extra time allowed by the shadow registers by configuring the duty cycle of the clock. A delay of 25% of the overall clock cycle was selected, which results in an asymmetrical clock signal.

The selection of a short error detection phase, enabled a strategy whereby a barrier formed by transparent latches was situated between the compression tree of the multiplier and adder blocks. During the high phase of the clock, the partial products generation begins, but the signals provided by the multiplier are blocked at the latch barrier input, while during the low cycle of the clock, the latches become transparent and signals are free to pass to the adder.

V.RESULTS ANALYSIS:
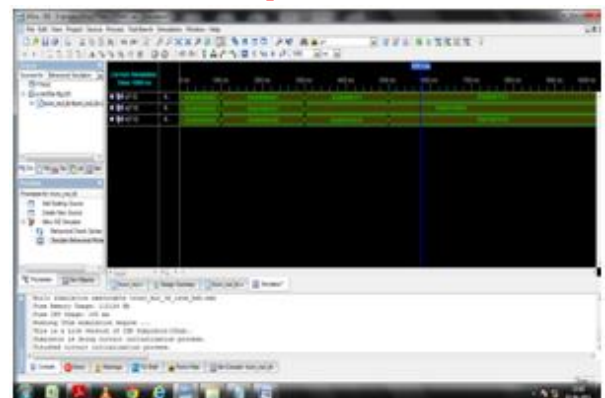
Results Truncated Multiplier

Fig 3 :Truncated Multiplier

Figure 2: Execution of five instructions in the Razor PTMAC pipeline. With the four stages of the Razor error detection-correction cycle indicated.
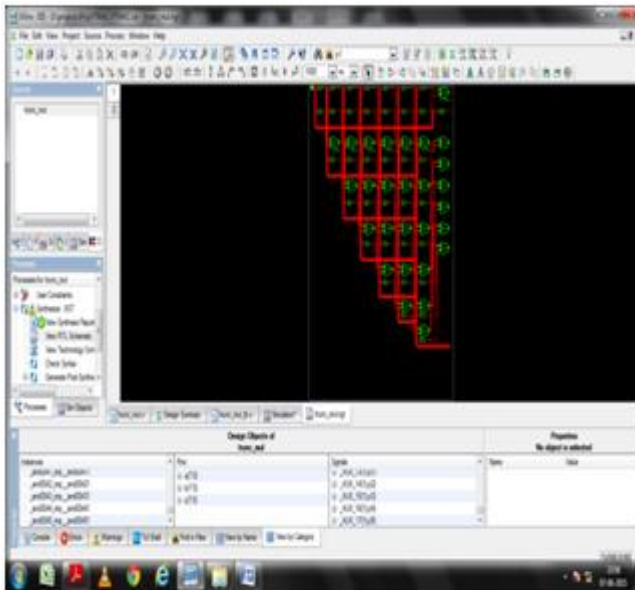
Fig 4 :RTL Schematic
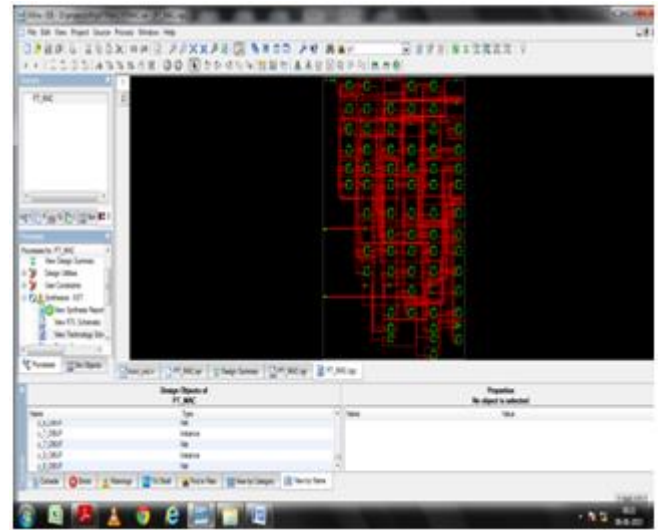

Fig 7 :Technology Schematic
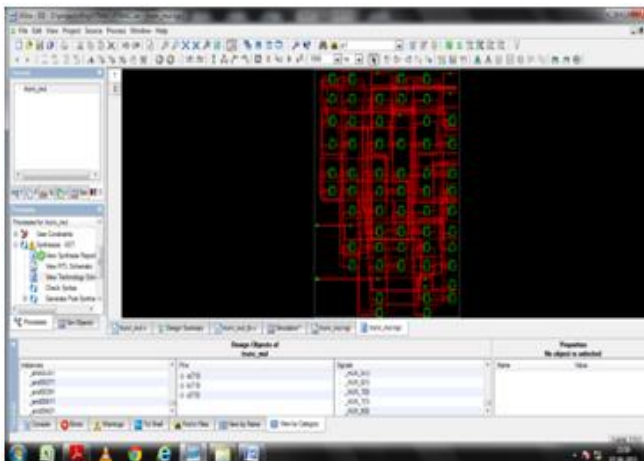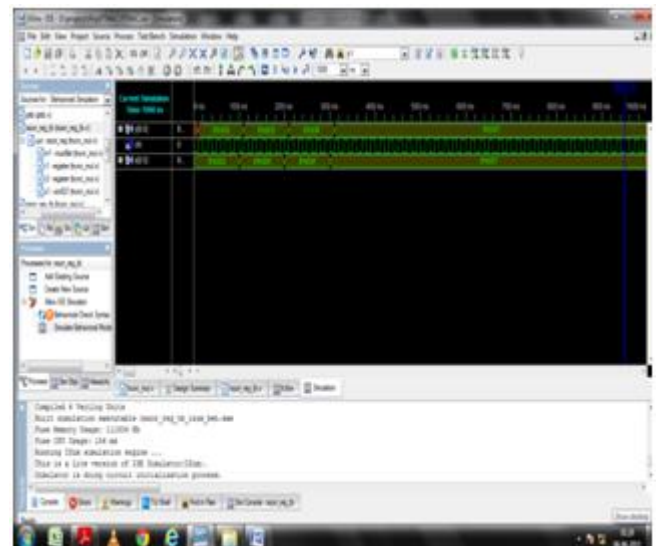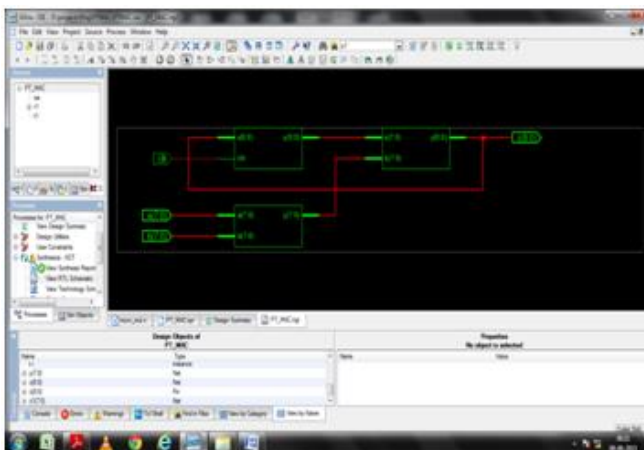

Fig 5 :Technology Schematic
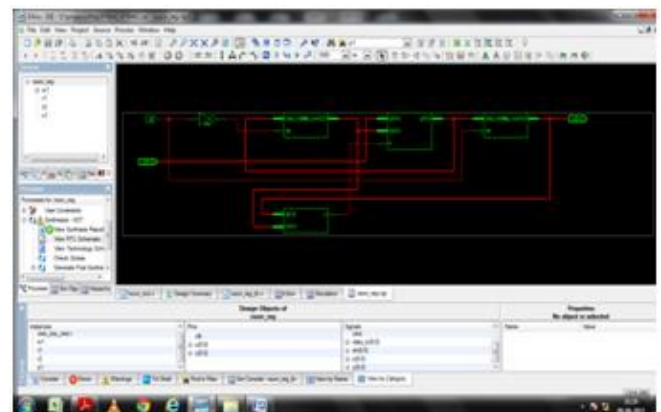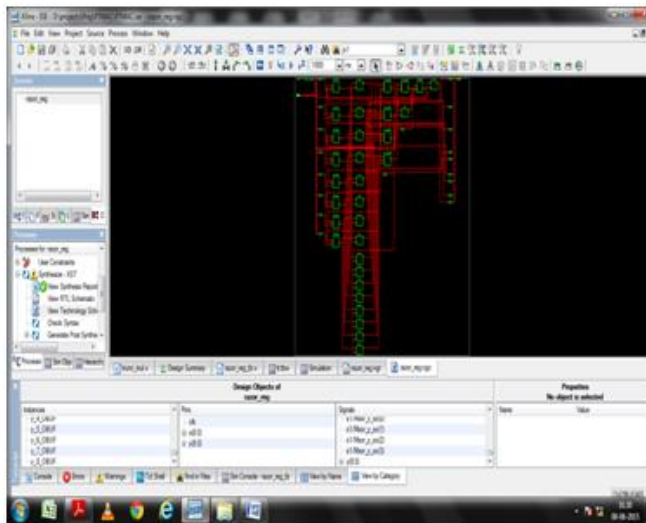

Fig 8:Razor reg

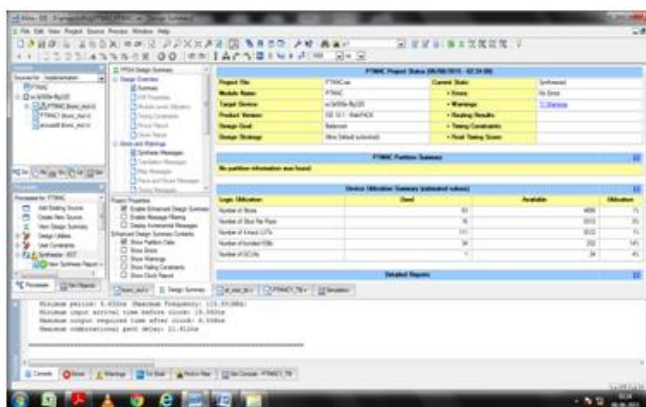
Fig 6 :RTL Schematic

Fig 9 : RTL

Fig 10 : Technology Schematic
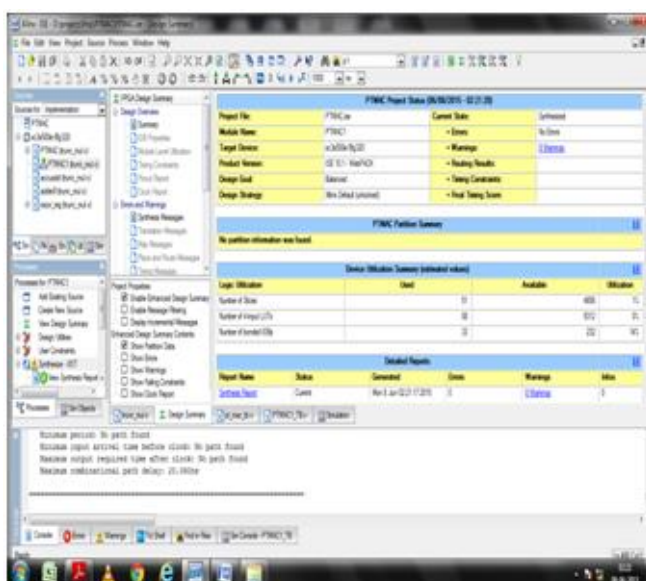

Fig 11 : PTMAC

Fig 12 : PTMAC1

VI. CONCLUSION

The use of Razor on a PTMAC structure has been tested at a post synthesis simulation level to study the effect and interactions of both energy reducing techniques on a previously tested DSP design. The timing and power effects of VOS with error correction and the application of programmable truncated multiplication resulted in significant power reductions. Fault tolerance was provided by implementing a conservative approach to the Razor I technique, and achieved energy reductions of 17.7% over the original DSP implementation by enabling the reduction of Vdd beyond the original critical supply level. Truncated multiplication was achieved by implementing a PTM, and resulted in energy savings of 8.1% of the full design.

Energy reductions achieved by fault tolerant techniques are limited by the overheads required to provide error resilience and the amount of operations that need correction, therefore, they are highly influenced by the delay distribution and maximum value of the system critical paths. The introduction of the truncated multipliers achieve two goals in this scenario: 1) it reduces power on the multiplier by cancelling the switching activity within its least significant sections and 2) disables the multiplier critical path, thus reducing the error recovery overheads of Razor, and extending the applicable Vdd range.

Results show that the application of both techniques to the proposed DSP unit allow maximum energy savings of 24.8%, improving the results obtained by independently implementing programmable truncation, fault tolerance via Razor, and the most optimistic prediction for the combination of both techniques (24.4%). This indicates that the delay-modulation properties of truncated multiplication can be exploited to improve the energy consumption of fault tolerant DSP architectures where multipliers are involved in the critical path of the circuit.

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