ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Implementation of Power Optimization Technique for Mixed Launch of Capture (LOC)andLaunch of Shift (LOS)

T.Divya
MTech Student
Department of ECE
Prasad Engineering College,
VikasNagar,Siddipet Road
Jangaon,Warangal District.

A.Akhila
Assistant Professor
Department of ECE
Prasad Engineering College,
VikasNagar,Siddipet Road
Jangaon,Warangal District.

Nihar
HoD
Department of ECE
Prasad Engineering College,
VikasNagar,Siddipet Road
Jangaon,Warangal District.

Abstract: ***The speed testing of Very Large Scale Integrated (VLSI) circuit aim for increasing high - quality screening of the digital circuits and reducing testing faults. On one hand, a compact test set with highly effective patterns, and detecting number of multiple faults, is desirable for lower test costs. On the other hand, this process increase signal activity during launch and capture operations. This process control for quality and cost may thus end up violating peak-power constraints, the output in yield loss, while the test pattern generation under low switching involvement constraints may lead to loss in test quality or pattern count inflation. This paper, we propose design for testability (DFT) support for enabling the use of a set of patterns optimized for cost and signal quality as is, less power manner; in this project we are developed three different ty6pes of Design For Testability (DFT) techniques, one is launch-off capture by using scanning operation , second one launch-off shifting , and last one for mixed technique this method used for increasing the speed testing . The proposed Design For Testability (DFT) technique used for enables a design partitioning operation, where given set of test patterns, created in a less power manner, this technique can be utilized to test the design circuits and decreasing both launch and capture power in a electronic design circuits-flow compatible manner. This method, the test pattern generation counts and quality of the optimized test set can be preserved, while lowering the launch of capture(LOC) and launch of shifting (LOS) power.***

Keywords: ***LOC, LOS, Low Power, BIST***

I. INTRODUCTION

The speed testing of Very Large Scale Integrated (VLSI) circuits main aims for a increases quality screening of Very Large Scale Integrated (VLSI) circuits, and correcting related faults. Based on scanning operation at speed testing possibilities on load, launch, capture, shift operations for each and every test pattern generation signals. Load technique is used for scan, shift related operations, filling up all the scan based signal chains with the pattern. The main aim for defects are timing-related, these test patterns need to check whether transitions launched from scan cells can arrive at their destinations within a functional clock period. There are mainly two different operations for launch transitions off the serially based loaded pattern. In the launch-off capture (LOC) test operation technique used as a functional capture operation launches transitions from the locations where the serially loaded pattern (V1) differs from the response of the combinational logic to V1, i.e., the launch pattern (V2). In launch-off-shift test operation it shifts single cycle operation launches transitions from the locations where the serially loaded pattern (V1) differs from its one-bit shifted version, i.e., the launch pattern (V2). In this two schemes ,a subsequent fast testing functional capture operation is performed, Which is of a functional clock period apart fromthe launch event, sets as Dead line for the transitions to reach their destination .a time based faults that slows down the chip delay its rated clock speed is in increased . Yet the loss problems are solved by using

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

speed testing techniques during switching activity the launch cycle provides in elevated peak supply currents, leading to IR drop and increase the signal path delays in the combinational circuits. The final effect cannot be find out from that of a timing-related defect, at the functional chip is failed at test pattern generation. Peak power during the launch cycle of at-speed testing should therefore be reduced in order to avoid the yield loss induced by IR drop. Significant research efforts have been expended in reducing power dissipation during the launch and capture of at speed testing.

Test pattern generation while accounting for the functional clock gating logic in order to produce patterns that disable parts of the design during launch and capture has been proposed in and to reduce peak power at the expense of pattern count inflation. Another approach that elevates pattern count while reducing peak launch power has been in the form of generating patterns under the constraint that only one chain launches transitions while all chains capture them Another similar scan-segmented solution partitions the scan cells into three regions where only two out of three regions launch and capture any test pattern. A partitioning approach has been proposed in where power wise costly patterns are further analyzed via fault simulation to identify the location of the care bits, which dictate the partitioning of the design during capture; with few problems at icpatterns, such an approach can deliver power savings. X-fill approaches have also been proposed where pattern count inflation is the side effect. Partitioning the design and testing one partition at a time has been proposed to reduce launch and capture power in built-in self-test (BIST) in LOS and in LOC testing schemes; in all these schemes, newly generated patterns targeting one partition at a time end up loading the interface registers of other partitions as well, incurring test time and data volume penalty. Similarly, pattern count increase has been experienced and minimizes capture violations.

II EXISTING SYSTEM

In this existing system we are using launch of capture and launch of shifting operation are used for speed testing in electronic circuits. Launch of capture based schematic diagram

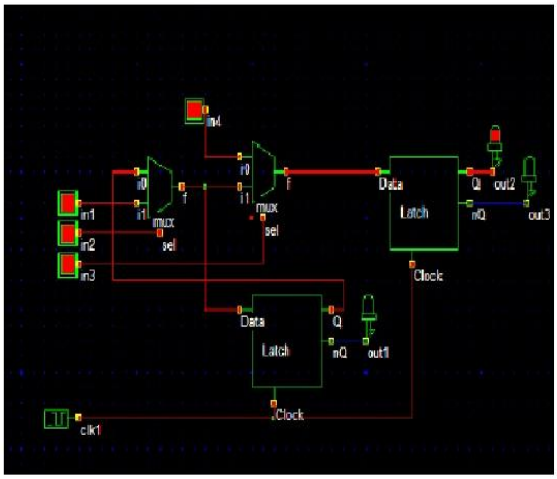

FIG: SCEMATIC DIAGRAM OF LOC

A. Launch of capture

At-speed scan test based applications for which static testing is not sufficient to the speed testing. The basic technique of speed scan testing involves loading the scan signals at a low clock speed rate and then applied two clock pulses at the functional frequency as shown in above figure. The first pulse effects a transition to start propagating path from a scan based cell. The second pulse captures the scan cell value at the end of the path being tested. Speed scan test involve loading scan chains signals at a low clock rate and then applied two clock pulses at the functional frequency. If the circuit is functional, then the transition will propagate to the end of the path in time and the correct value will be captured. Otherwise, if a delay causes a low propagation, the transition from launch to capture cell will be low, fault value will be captured, and the error will be detected. The most popular the speed scan pattern is the transition based test pattern. A potential fault of low to high (0 to 1) and low level to fall (1 to 0) is modeled at every gate terminal within the test pattern generation design. Automatic Test-Program Generation (ATPG) tools target these fault sites and cause a transition using any launch scan cell and capture results using any downstream scan cell.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

B. Using PLLs for accurate clocks

The basic problem with speed based scan testing how to apply accurate clock signal for the speed launch and capture pulse wave forms. The basic stuck-at scan patterns are static. Stuck-at clocking for loading the scan chain and capturing fault results is often performed at frequencies between 10MHz and 40MHz. At-speed scan testing can load the scan chains with a clock frequency that is similar to the one used for stuck-at tests, but the launch and capture pulses must be applied at the functional frequency.

C. Launch of Shift Operation

In this launch of shifting operation we are using Automated Test Pattern Generation(ATPG) are used to perfectly matches the test pattern generation With LOS patterns, the launch occurs during the last shift while loading the scaned signal. Next, the circuit is placed into were the capture mode very quickly so speed functional clock can be pulsed. Automated Test Pattern Generation (ATPG) technique is much easier technique with Launch OfShift (LOS) compared to broadside patterns.

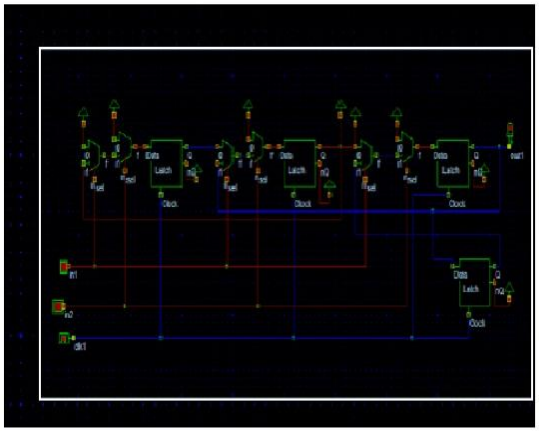

FIG: SCEMATIC DIAGRAM OF LAUNCH OF SHIFT

It is a simple Automated Test Pattern Generator (ATPG) activity to load the starting value for a transition directly to the scan cell one shift before the last and then load the transition value in the last shift. Broadside patterns requires Automated Test Pattern Generator (ATPG) to calculate the transition value through the combinational logic values, since it is in functional mode during the launch pulse. In addition, Launch Of Shift (LOS) patterns usually report higher coverage than broadside patterns .launch of capture and launch shift it takes more power to detecting the faults in test pattern generation,it takes less speed to testing the signal generation and it takes more clock pulse signals compared other techniques so to overcome this problems we design combinational of both launch of capture (LOC) and launch of shift (LOS).

III PROPOSED SYSTEM

This proposed system we are using combinational of both the techniques, like Launch Of Shift (LOS), LaunchOf Capture (LOC) like that mixed operation. the schematic diagram for mixed technique is the only additional constraint imposed on scan stitching by the proposed partitioning system is interface with the registers of each path region should be placed in consecutive positions on the scan based signal chain and that they must be stitched in a bidirectional method. Such a special stitching method is associated with the Design ForTestability (DFT) support it is need only for the interface registers.

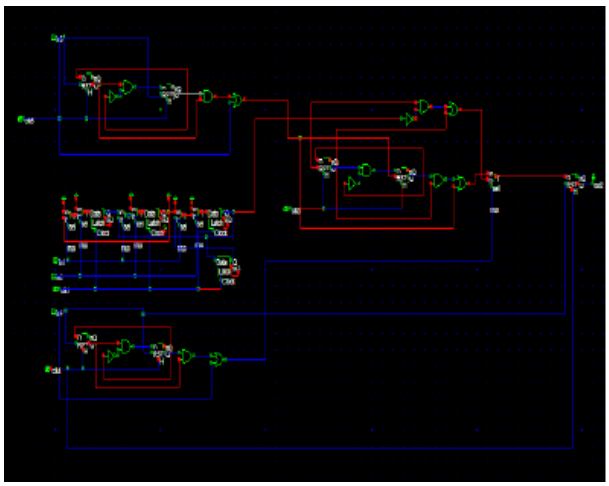

FIG:SCEMATIC DIAGRAM FOR

PROPOSED SYSTEM

In order to enable a proper scanned based means Launch ofCapture (LOC) technique. This method to

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

minimize the number of interface registers this registers helps to minimize the efficient area and cost incurred. Finally, re capturing the value of the right most bit of a group of interfacing registers subsequent to the launching operation necessitates an extra flip-flop, this flip flop holds the value of the rightmost interface bit upon Launch Of Shifting (LOS) operation. a subsequent re win operation restores the value of the rightmost interface register bit in the form of the value in this extra flip-flop which is used. Bidirectional stitching of the interface registers in this region needs one extra multiplexers for each interface register devices this multiplexers can be replaced on the scan path , imposing no impact on the functional timing of the design whatsoever.

The proposed scan architecture that supports design partitioning into two regions is it provided inabove figure.As the Launch Of Shift (LOS) and Launch Of Capture (LOC) testing may uniquely detect faults in a bidirectional manner, a mixed test with both Launch Of Shift (LOS) and Launch Of Capture (LOC) patterns typically yields a higher fault coverage level compared to either testing scheme applied alone .in this pattern , we outline the Design For Testability (DFT) support required to support low power mixed testing with both Launch Of Shift (LOS) and Launch Of Capture (LOC) patterns. While the bidirectional stitching of interface registers fails to enable the proposed low-power Launch Of Capture (LOC) testing, the shadow register support can be utilized to enable the proposed low power Launch Of Shift (LOS) testing the shadow registers can replace the bidirectional stitching for the restoration of the load state in Launch Of Shift (LOS) testing. Therefore, to support both low power Launch Of Shift (LOS) and Launch Of Capture (LOC) testing, the architecture in above figure can be utilized, but with a couple of changes the shadow registers should be clocked only during the shift cycles, and a unified Restore signal should be generated to support both Launch Of Shift (LOS) and Launch Of Capture (LOC) operations. The simple circuitry that generates this unified Restore signal is provided in the Launch Of Shift/Launch Of Capture signal, which denotes the type of test for the current pattern being applied and can be controlled.

IV CONCLUSION:

Here we proposed DFT support that can recollect the load state in interface registers in between the launch/capture operations in the design regions, enabling low-power Launch Of Capture, Launch Of shifting, and mixed at-speed testing. This way, a set of patterns optimized for low Cost and High Quality can be used as is, yet in a low power manner.

V REFERENCES

[1] O. Sinanoglu, "Rewind-support for peak capture power reduction in launch-off-shift testing," in *Proc. 20th Asian Test Symp.*, Nov. 2011, pp. 78–83.

[2] S. M. Saeed and O. Sinanoglu, "DfT support for launch and capture power reduction in launch-off-capture testing," in *Proc. 17th IEEE Eur.Test Symp.*, May 2012, pp. 1–6.

[3] J. Savir and S. Patil, "On broad-side delay test," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 2, no. 3, pp. 368–372, Sep. 1994.

[4] J. Savir and S. Patil, "Scan-based transition test," *IEEE Trans. Comput.Aided Design Integr. Circuits Syst.*, vol. 12, no. 8, pp. 1232–1241,Aug. 1993.

[5] P. Girard, "Survey of low-power testing of VLSI circuits," *IEEE Design Test*, vol. 19, no. 3, pp. 82–92, May–Jun. 2002.