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Low-Power and High Performance Charging/Discharging Flip-Flop Design Using Pulse Generator

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ABSTRACT:
In all digital designs we are using the storage elements. Basic storage elements are the flip-flops, in this paper we focus on the low power flip-flop using pulse triggered structure based on signal feed through scheme. The proposed pulse triggered flip-flop solves the long discharging path in conventional designs and this design works with the low power and it shows the high performance. The proposed pulse triggered flip-flop simulation results testing in CMOS 90nm technology. The power and power delay product metrics in the performance edges are 22.7% and 29.7% respectively.

INTRODUCTION:
In Electronic designs, flip flops or latches are circuits which are used to store state information. The Flip flop circuit have the two stable states the circuit controls the two or more inputs and it's have the two or more outputs. In digital electronics the flip flops are used in computers, communications, and in portable devices. In present Technology most of flip-flops are working with the pipelining technique those are shift register, register file, first-in first-out. When estimating the total power consumption in clock system is high as 50% when the total power dividing and it goes to storage elements and clock distribution systems. In the overall system designs the flip-flops plays a virtual role in chip design and power consumption.

Pulse triggered flip-flops are more popular than the conventional transmission gate flip-flops because P-FF have the single latch structure. The pulse triggered flip-flop is working with the low power and the performance of this P-FF is more when compare with the other master slave flip-flops. Pulse triggered flip-flop (P-FF) have the pulse generator for generating the signals and it's have the latch for store the data. When pulse generator provides sufficient triggering pulses on that same time the latch behaves like an edge triggered Flip-flop. Pulse triggered flip-flop circuit complexity is less, In the master slave configuration which is need to oppose one latch with another one to provide the accuracy results. In high speed applications Pulse triggered flip-flop based on signal feed through scheme have the high speed toggle rate. The pulse triggered flip-flops also enables the appropriate time clock pulses and attribute a zero or even negative concern time. The pulse generator circuit wants the exquisite pulse width control to attribute with number of variations in present process technology and signal distribution network. When we are designing the any module in digital electronics we are considering the three factors those are power, area and performance. The proposed pulse triggered flip-flop satisfies the three factors its works with the low power, high performance and it takes less area.

In this brief, we present a high performance low power pulse triggered flip-flop based on signal feed through scheme. To speed up the data transmission, the latching data in dispensary delay is '1' and '0' the design undertaken the shorten and long delay for signal feed through scheme in the input signal is directly connected to the internal node of latch design. The design is implemented by instigating a simple pass

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transistor design for extra driving signal. When any flip-flop is combined with the pulse generator it forms the new pulse triggered flip flop design with increased speed and power delay product interpretations.

PROPOSED PULSE TRIGGERED FLIP-FLOP:

Here we are designing the two types of pulse triggered designs based on signal feed through scheme, those are

1. Conventional Pulse Triggered Flip-Flop
2. Pulse Triggered Flip-Flop

1. Conventional Pulse Triggered Flip-Flop:

Here we are discussing about the Conventional P-FF Designs. It can be classified in to two types one is implicit and another one is explicit type. In implicit design, no explicit pulses signals are generated only implicit pulse signals are generated which is the part of latch design. In explicit pulse triggered design, latch and the pulse generator are separate. The implicit and explicit designs take the more power when we are working with without generating the pulse signals. However, the explicit and implicit designs are not working properly with the long discharging path and those are taken more power. The explicit design pulse triggered flip-flop design working with the more power consumption but in the latch design the logic separation gives the unique speed in flip-flop design. The power consumption and circuit complexity can be reduces the one pulse generator in N number of pulse generators. Mainly here we are focusing on the one type of pulse triggered design only i.e. Explicit P-FF Design.

For comparison, here we are designing the Data close to output (ep-DCO) design. The design is designed by based on explicit P-FF Design. The design has the NAND logic gate based pulse generator and True Single Phase Clock (TSPC) latch design. In this NAND gate based Pulse generator Flip-Flop Design, For providing the latch data we are using the I3 and I4 inverters, to hold the internal node X we are using the I1, I2 inverters. The design pulse width is determined by the delay of 3 inverters. Figure 1 shows the Data Close to Output (DCO) Design.

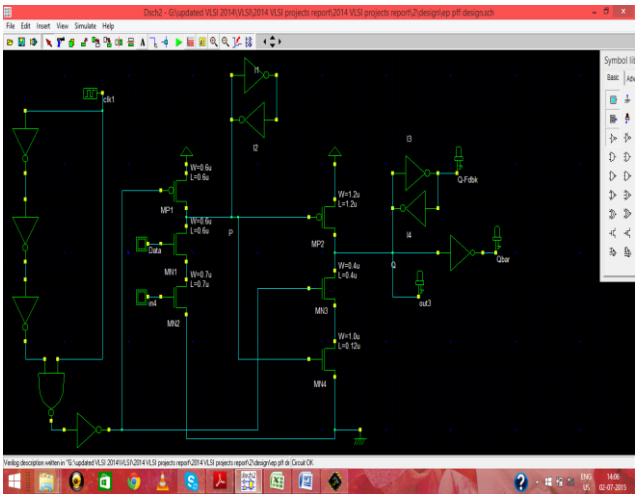

Figure 1: Design of Data Closed to Output (ep-DCO)

The Data Close to Output based on Explicit P-FF design have some drawbacks those are when the rising edge on pulse generator the internal node X will be discharged. Pulse generator provides the pulses high and low, when the pulse will be high automatically the 'X' will be discharged. To solve the problem, we are proposing the conditional precharge, conditional capture, conditional enhancement and conditional discharge. The figure 2 shows the conditional discharge design. An extra transistor is connected to previous design that is MN3 it controls the output Q-fdbk so here no discharge will be occurred when pulse generator provides the positive peak.

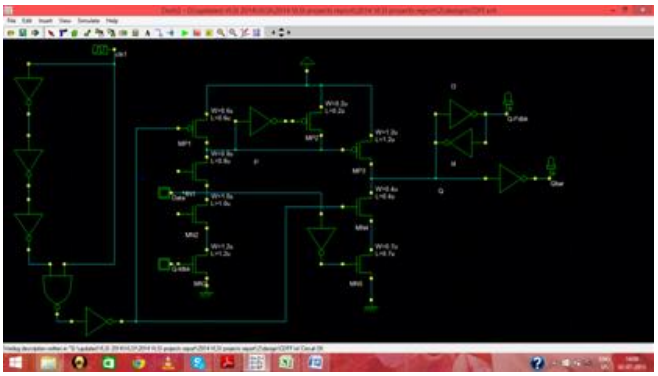

Figure 2: CDFF Design

Figure 3 shows the Static conditional Discharged Flip-flop (Static CDFF). It different when we are comparing with CDFF technique. Static CDFF design provides accurate results. The static CDFF design

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provides the longer data to Q delay. Both Designs are providing the longer delay in M1, M2, M3 Transistors.

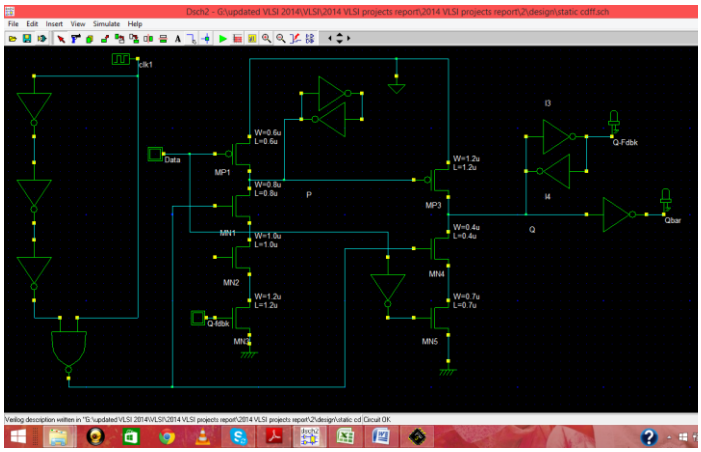

Figure 3. Static CDFF Design

The CDFF and Static CDFF pulse triggered Flip-Flops are providing the longer delay in M1, M2, M3 Transistors so to reduce that problem we are implementing the new design i.e. Modified Hybrid Latch Flip-Flop and it's have the static latch. In this design the internal node 'X' will be removed. In this MHLFF design the weak signal m1 transistor controlled by the output Q when the internal node X will be zero. The design circuit complexity is high when compare with the other techniques. The figure 4 shows the MHLFF design

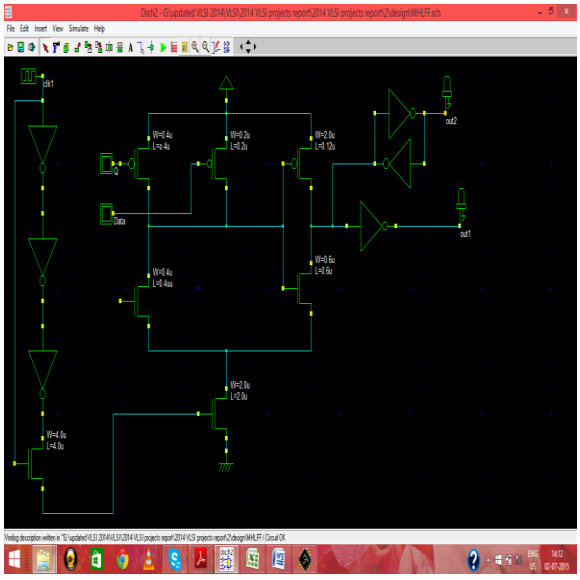

Figure 4: MHLFF Design

2. Pulse Triggered Flip-Flop:

The DCO, CDFF, Static CDFF and MHLFF have their own draw backs because of this reason we are proposing the Pulse Triggered Flip-Flop. To improve the delay we are implementing the design based on signal feed through scheme. The static CDFF and Proposed pulse triggered Flip-Flop both are having the static latch. However, we have the 3 major differences in proposed pulse triggered flip-flop design in a unique TSPC latch structure. First, in the first stage of TSPC latch pull up PMOS transistor MP1 gate will be connected to the ground. When the signal rising edge on that time no discharge path will be occurred in the Pulse Triggered Design. This design also reduces the capacitance node of 'X'. Second one, the simple pass transistor is controlled by the pulse clock signal which is included so that the given input data can be divided in to the latch directly. The pull up transistor MP2 that is second stage of inverter is directly connected the input Source node to Q. The level of node can be speedily pulled up to the transmission time delay. Third one, the second stage of inverter network completely removed in the pulse triggered Flip-Flop Design. Here we are connecting a new pass transistor that provides a new discharging path in the design.

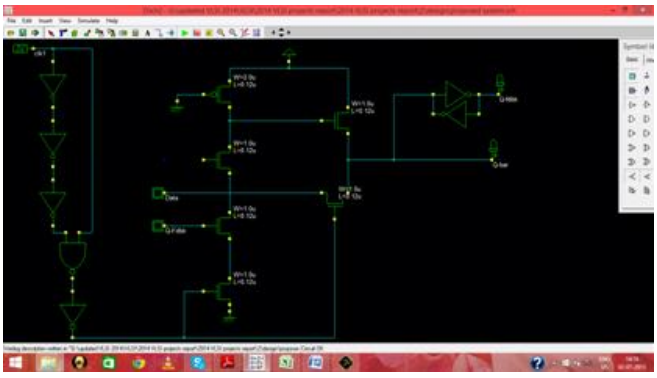

Figure: Proposed Pulse Triggered Design

SIMULATION RESULTS:

Here we are designing the Schematics in Low Power design Circuits on Digital Schematic (DSCH). The Proposed system is designed based on the 90nm Technology. Here we are generating the different factors in Micro wind Tool. The factors are Voltage vs Time, Voltage vs Current, Voltage vs Voltage and

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Frequency vs Time. The below figures shows the simulation results of proposed system.

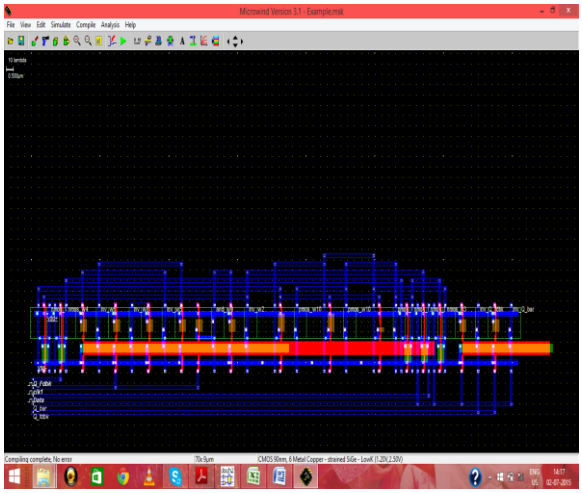

Figure 5: Layout Diagram of P-FF

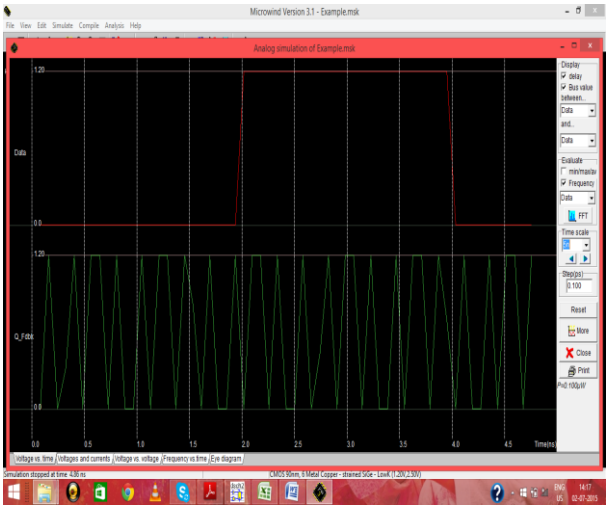

Figure 6: Voltage vs Time

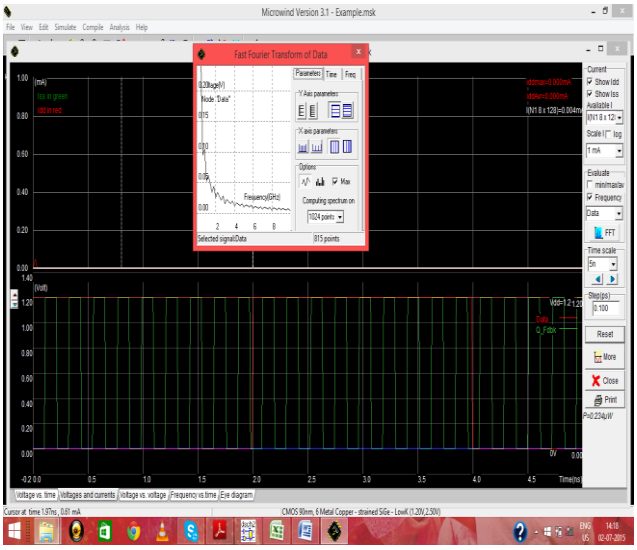

Figure 7: Voltage vs Voltage with FFT

CONCLUSION:

Here we are designing the low power pulse triggered flip-flop based on signal feed through scheme in 90nm Technology. In modified TSPC structure mixed design style consists of a pass transistor and pseudo-nmos logic. It provides the signal feed through scheme from input source to internal source of the latch. The proposed Pulse triggered Flip-Flop design is working with the low power and it provides the high speed results.

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