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Implementation of Low power All-Digital PLL Architecture for Advanced Nanometer Technologies

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Abstract:
In this paper, we are proposing a which can produce oscillating-clock signals with the certain frequency used a total designated range. However, we are proposing the all-digital phase-locked loop optimization process as a search problem, during that problem we can find a good configuration that not only achieves the user defined requirement but it achieves a lower power and smaller area utilization than a manual design. The silicon design measurement parameters shows that it's a new alternative approach for Analog phase-locked loops (APLL), especially it will be developed for advanced nanometer technologies. The proposed design is working with the low power and high performance. The proposed system will be designed in Xilinx 14.2 the RTL design and all simulation results are shown in the Modelsim.
Keywords: All-Digital PLL (All Digital Phase Locked Loop), (Digitally Controlled Oscillator), Analog PLL (APLL), Xilinx, Low Power, Nanometer Technologies.

I INTRODUCTION:

In Electronics Phase Locked Loops are used in different types of applications. Phase Locked Loop is a control system; the signal output phase is related to the input signal phase. Every electronic circuit have the phase detector and variable frequency oscillator. The oscillator generates the certain frequency periodic signals. A phase detector is the logic circuit that provides the voltage signal which represents the phase difference between the input and output signal. The phase detector compares the both input signal phase and adjusts the oscillator to provide the certain periodic signals to match the phase of input signal and output signal. If u are taking the any clock pulsed base circuit it is mandatory to use high speed clock pulse generator to provide the pulses for circuit same like that here Phase Locked loop have the some Analog Blocks those are charge pump and voltage control oscillator. The analog signals in these analog blocks swing to be persuadable to the noise caused by the constantly switching of the digital signals. Present days, in CMOS process the power and performance are became serious problems. The Compilation and the less Complexity of designing an analogue Phase Locked Loop (PLL) increases as the advanced technology. Because of this reason, there is most number of researches aiming on the All-Digital Phase Locked Loop (All Digital Phase Locked Loop), considering that have better higher stability and noise immunity thus could be a alternative way to improve accuracy in migrating modules.

The main component for an All-Digital Phase Locked Loop (All Digital Phase Locked Loop) is the (Digitally Controlled Oscillator), which provides the maximum frequency, frequency range, and the better resolution. For different applications we are having the Clock Synchronization and the Clock and Data Recovery (CDR), these benefits of Digitally Controlled Oscillator are the most important considerations for designers. The All Digital Phase Locked Loop portability has been effectively enhanced by realizing a with only the standard cells are proposed. The most Digitally controlled oscillators are proposed in 0.18um

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technology with the frequency of 700MHZ. If we are implanting the any design we are consider three things those are power, area and performance. Here our proposed design is working with the low power and it takes less area when we are going to the fabricate and it shows the high performance with the certain frequency of 700MHZ.

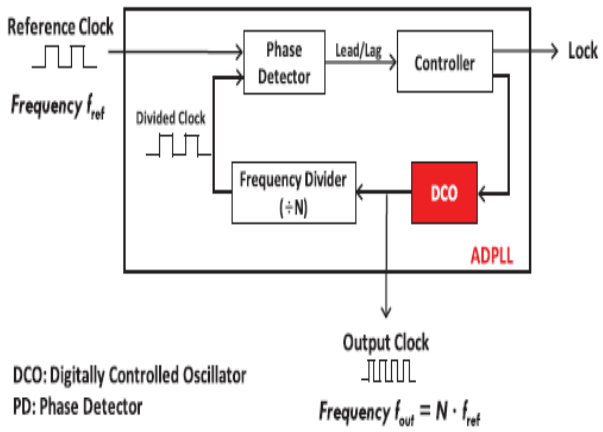

Fig. Overall architecture of the proposed All Digital Phase Locked Loop.

In this brief, we have two major considerations, here we are proposing the (Digitally Controlled Oscillator) it provides the maximum 1MHZ output frequency in the operating frequency range. Using different standard cells we are implementing the (Digitally Controlled Oscillator) design. Using we are implementing the design that is the All-Digital PLL (All Digital Phase Locked Loop). The automation of power design, we are taking a easy way to migrate the Digitally Controlled Oscillator in All Digital Phase Locked Loop. In our simulation results the design takes the less compatibility with low power. According to our All Digital Phase Locked Loop design implementation, we are finding the important factors those are Low power and less cost and the Digitally Controlled Oscillator design have the user friendly specifications with number of configurations. Parameters of fabricated test chips are shown that quality compatibility of the All Digital Phase Locked Loop implemented by our compiler is highly effective as compared to the most recent previous works on full-custom and/or analog Phase Locked Loops.

In this brief, in section II we are discussing about the All-Digital PLL (All Digital Phase Locked Loop) and proposed design (Digitally Controlled Oscillator). In section III we are discussing about the All-Digital PLL (All Digital Phase Locked Loop) Compiler. In section IV we are discussing about the simulation results of our proposed design.

II All Digital Phase Locked Loop and Digitally Controlled Oscillator :

The All Digital Phase Locked Loop architecture have the 4 major blocks:

1. Phase detector
2. All Digital Phase Locked Loop Compiler
3. Frequency Divider
4. Digitally Controlled Oscillator

In N Integer All Digital Phase Locked Loop, the generates the certain frequency of output clock signals are divided by N times to produce a less speed divider clock signal. Here N is the Frequency Multiplicative Factor. The phase detector is to compare the phase polarity between the divided-clock signal and the reference-clock signal. It generates two mutually exclusive signals: one is lead and the other is lag, to show whose edge is leading. Once the frequency of has been tuned as close as possible to the target frequency and the phase of the divided clock is in line with that of the reference clock, signal lock is then asserted, and the output clock frequency will be exactly '*N*' times the reference clock frequency. This is often regarded as the most critical part among these components because it dictates the frequency range and the resolution of an All-Digital Phase Locked Loop.

A. Architecture of the Proposed Digtally Controlled Oscillator

A parameterized to achieve the goal of improving maximum output frequency and resolution of the simultaneously is shown in Fig.

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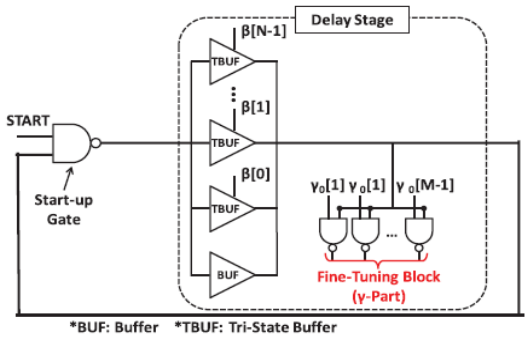

Fig. Architecture of the proposed Digitally Conrolled Oscillator.

It is formed with a loop including two parts, namely the coarse-tuning block (β-part) and the fine-tuning block (γ -part). In some sense, one coarse-tuning block and one fine-tuning block jointly form a tunable delay stage. Each part of the can respectively contribute to the overall Digitally Controlled Oscillator's performance one way or another, as to be described below.

1) Coarse-Tuning Block (β-Part): In the coarse-tuning block, we adopt the controllable driving strength method, which increases the driving strength gradually to achieve the goal of increasing the maximum output frequency of the Digitally Controlled Oscillator. As shown in Fig.

N tri-state buffers are connected in parallel to one buffer in each tunable delay-stage. When the numbers of enable tri-state buffers is increasing, some additional driving current is added to the tunable delay-stage so that the overall delay of the delay chain will decrease. These tri-state buffers connected in parallel are called driving-strength-tuning block in the sequel. The benefit of using tri-state buffers for coarse-tuning includes a finer resolution as compared to the general path selector.

2) Fine-Tuning Block (γ -Part): The resolution of the used in this paper is determined by some two-input NAND Fig. Clock period profile spanned by β-code and

γ –code the gates that are called loading gates in the sequel. In γ -part, as shown in Fig, a two-input NAND gate array is attached to the output node of β-part in each tunable delay-stage, which can slightly adjust the output frequency of by controlling the number of turned-on NAND gates as proposed . This is due to the fact that different numbers of turned-on NAND gates will cause the changes on the loading effect at the output node of β-part. This fig shows a segment of the period profile (over different tuning codes) of the proposed Digitally Controlled Oscillator. A β-range is the range of the Digitally Controlled Oscillator 's clock periods spanned by varying the γ -code under a specific coarse-tuning β-code. During the Digitally Controlled Oscillator 's frequency locking step, we only need to decide the best initial β-code (which harbors the desired target clock period). As for the fine tuning of γ -code within the selected β-code, we then decide it in the phase-locking step. It is notable that the maximum Digitally Controlled Oscillator 's clock period that can be offered by each β-code is dictated by the maximum output capacitance induced by the side input of each of the two-input NAND gates when every bit of the γ -code is assigned to logic-1, i.e., γ -code = 11. . .1. On the other hand, the minimum Digitally Controlled Oscillator 's clock period that can be offered by each β-code is dictated by the minimum output capacitance induced by the side input of each two-input NAND gates when every bit of the γ -code is assigned to logic-0, i.e., γ -code = "00. . .0". It is notable that the architecture of the Digitally Controlled Oscillator is very flexible and easy to change to meet various specifications due to its large configuration space.

Definition 1 (Configuration of the Digitally Controlled Oscillator): one configuration of Digitally Controlled Oscillator is decided by the combination of the following five parameters:

1) The type of the buffer
2) All sorts of combination of the driving-strength-tuning
3) The number of loading gates used in the fine-tuning block

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4) The number of delay stages

5) The number of startup gates to meet the application and specification.

III. All Digital Phase Locked Loop Compiler

Based on the proposed Digitally Controlled Oscillator , we have developed the All Digital Phase Locked Loop compiler, which contains two major schemes:

1) a quick Digitally Controlled Oscillator -timing analyzer and

2) the Digitally Controlled Oscillator configuration finder to provide a quick search to find a Digitally Controlled Oscillator ,

which not only meets the user-defined specification but also does the optimization in terms of area and power consumption.

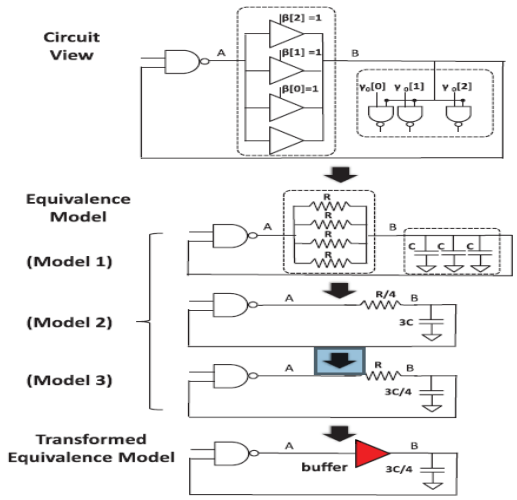

Fig. Derivation of the transformed equivalence model.

A. Quick Digitally Controlled Oscillator -Timing Analyzer

For a Digitally Controlled Oscillator , it always requires the transistor-level simulation to acquire its timing information, even for a standard cell-based architecture. However, the transistor-level simulation is so time-consuming that it is hard to explore all kinds of configurations in a short time. In light of this, we propose a quick Digitally Controlled Oscillator -timing analyzer that combines the timing information listed in the standard cell library file (i.e., the .lib file) only and some calibrated timing information from a few Digitally Controlled Oscillator samples. We attempt to explore the timing correlation between these two sets of timing information for those Digitally Controlled Oscillator samples and then we extrapolate the results to all the other configurations for quick Digitally Controlled Oscillator -timing estimation.

1) Transformed Equivalence Model Of Digitally Controlled Oscillator :

In the standard cell library, the delay information of each gate could be obtained from the 2-D look-up table by specifying the input transition time and output capacitance. However, the approach will run into trouble when we would like to calculate the delay time of one node that is driven by multiple gates simultaneously, and this is the case in our proposed coarse tuning block. Therefore, a transformed equivalence model is required to solve the issue. The concept of the transformed equivalence model is to use a single driving gate to represent the effect of the multiple driving gates by using a series of transforming processes, as described in Example 1.

Example 1: as shown in Fig, in order to estimate the delay time from node A to node B (where node B is driven by one buffer and three tri-state buffers simultaneously, and loaded by three two-input NAND gates), the first step it to build the primitive equivalence model named Model 1 in the Fig. Model 1 adopts the resistors and capacitances to represent the driving-strength variation and the loading effect, respectively. Without the loss of generality, we assume that the buffer and the three tri-state buffers have the same driving strength. For Models 2 and 3, resistances and capacitances are combined and normalized, which lead to a transformed equivalence model as shown in Model 4. Model 4 has 1 driving gate and 3/4th loading gate, which mimics the behavior of the original case (with 4 driving gates and 3 loading gates). By this simple transformation, we can use the library's information directly by referring to the 2-D look-up table of the buffer to estimate the delay time from node A to node B with the transformed equivalence model.

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The equivalence model could also be extended to support the combination of tri-state buffers with various driving strengths. For example, if the driving strength of a tri-state buffer TBUF*y* is twice as large as the basic tri-state buffer TBUF*x* of resistance *R*, then its representative resistance would be estimated as *R*/2.

2) Sample Digitally Controlled Oscillator Generation:

To minimize the estimation error, a few Digitally Controlled Oscillator s are generated as samples and simulated with a transistor-level simulator in advance. To determine how many Digitally Controlled Oscillator samples need to be generated is based on the type number of buffers used in the coarse-tuning block (β-part) and this is automatically selected in our All Digital Phase Locked Loop compiler. In general, six samples are required.

3) Timing Correlation Between Simulation and Estimation: For each major type of Digitally Controlled Oscillator , we would select an appropriate but small number of Digitally Controlled Oscillator samples to perform the timing correlation. In this process, the first step is to derive the maximum clock period offered by each β-code and the second step is to build up the clock-period range corresponding to each β-code.

Definition 2 (Digitally Controlled Oscillator Instance): A Digitally Controlled Oscillator instance (which is not like a Digitally Controlled Oscillator sample generated for only process calibration) is particularly referred to a target Digitally Controlled Oscillator that a user expects to generate by our All Digital Phase Locked Loop compiler. For each of such Digitally Controlled Oscillator instances our compiler supports, we need to provide the entire Digitally Controlled Oscillator period profile not only quickly but also accurately by a procedure as detailed below.

a) Step 1—Max-period calibration using Digitally Controlled Oscillator sample: For a Digitally Controlled Oscillator sample, by using the transformed equivalence model, we can quickly estimate the maximum clock period of each β-code. On the other hand, by postlayout (transistorlevel) simulation, we can derive a so-called max-period mapping ratio to correlate our estimation results to that of the postlayout simulation. For a particular β-code, if Pestimation and Psimulation denote the maximum clock periods within that β-code derived by our estimation and postlayout simulation,respectively, then the β-code-dependent max-period mapping ratio, denoted as Ratiomax-period (β), can be expressed as follows:

$$\text{Ratio}_{\text{max-period}}(\beta) = (P_{\text{simulation}} - P_{\text{estimation}})/P_{\text{simulation}} \times 100\%$$

For example, Pestimation = 1332 ps and Psimulation = 1536 ps when β-code equals 0 Thus, Ratiomax-period for this β-code is $(1536 - 1332)/1332 = 15.32\%$. Similarly, we can derive the Ratiomax-period as 18.14%, 20.64%, 23.15%, and 25.31% when β-code is 1, 2, 3, and 4, respectively.

b) Step 2—Max-period extrapolation to a Digitally Controlled Oscillator instance: Once we have the above max-period mapping ratio information for each β-code, we can apply it to a user-defined Digitally Controlled Oscillator instance by an extrapolation procedure: We estimate the maximum clock period of each β-code by our transformed equivalence model and then multiply the estimated results by the (1 + Ratiomax-period) to compensate for the estimation error between the our initial estimation and the postlayout simulation, as shown in Fig. The compensated equation is

$$P_{\text{compensated}} = P_{\text{initial-estimation}} \times (1 + \text{Ratio}_{\text{max-period}})$$

Based on our experimental results to be shown later, the average estimation error after the compensation as compared to the post layout simulation results is only about 2%. It is notable that the error could be some value in the range in the example shown in Fig, if the compensation scheme is not used.

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c) Step 3—β-Range estimation: Recall that the *β*-range refers to the Digitally Controlled Oscillator period range of a particular *β*-code in the Digitally Controlled Oscillator profile. Up to this point, we only derive the accurate estimation of the maximum Digitally Controlled Oscillator period for each *β*-code (i.e., the top point of each *β*-segment). To complete the entire Digitally Controlled Oscillator period profile, we need to further decide the *β*-range calibrated by the post layout simulation results. In the standard cell library, the input capacitance of each gate is constant and independent of the input values. This implies that the library file is not delicate enough to provide the timing information in response to subtle capacitance change inducedby *β*-code change when the side input of a two-input gate is switched from logic-1 to logic-0 or vice versa. To overcome this difficulty, new tactic needs to be developed.

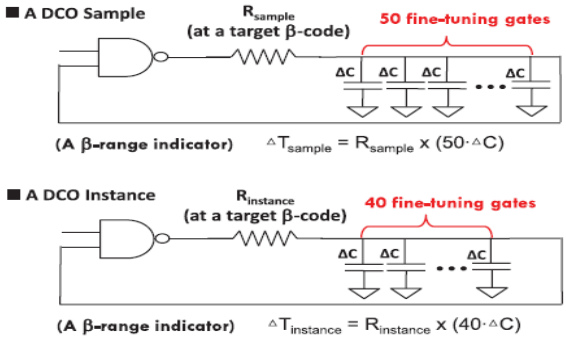

Fig. Illustration of the *β*-range ratio between a Digitally Controled Oscillator sample and a Digitally Controlled Oscillator instance

Each *β*-range of the Digitally Controlled Oscillator sample has been accurately known. For a specified *β*-code in a given user-defined Digitally Controlled Oscillator instance, we can derive a quick and accurate estimation of its range by the following procedure.

1) First, we derive the ratio of the target *β*-ranges between the Digitally Controlled Oscillator sample and Digitally Controlled Oscillator instance.
2) Second, we multiple the *β*-range of the Digitally Controlled Oscillator sample, and then use the result as the final estimated *β*-range for the Digitally Controlled Oscillator instance.

The second step is relatively easy, but the first step is more involved and deserves further explanation. In general, a target *β*-range is highly correlated to the RC time constant change associated with a delay stage due to the *β*-code change, and thus can be expressed as

$$\Delta T_{instance} = R_{instance} \times (40 \cdot \Delta C) \text{ /* for DCO instance */}$$
$$\Delta T_{sample} = R_{sample} \times (50 \cdot \Delta C) \text{ /* for DCO sample */.}$$

In the above expressions, △ Tsample and △ T instance are the *β*-range indicators for a target *β*-code of the Digitally Controlled Oscillator sample and the Digitally Controlled Oscillator instance, respectively. Rsample and Rinstanceare the equivalent resistance of △ the parallel tri-state buffers (estimated by our transformed equivalence model), and C is the minute capacitance change when one fine-tuning cell is turned from "0" to "1." We have assumed that there are 50 fine-tuning cells in the Digitally Controlled Oscillator sample and 40 fine-tuning cells in the Digitally Controlled Oscillator instance. Since we are only interested in calculating the ratio of Tinstance Tsample, in which C is canceled out and thus there is no need to know its exact value. Now we have arrived at the following expression for *β*-range mapping ratio, denoted as Ratio*β*-range*(β)*, and the expression for the estimated *β*-range of the Digitally Controlled Oscillator instance, denoted as

$$\text{Ratio}_{\beta\text{-range}}(\beta) = (R_{instance}/R_{sample}) \times (40/50)$$

$$\beta\text{-Range}_{instance}(\beta) = (\beta\text{-range of DCO-sample}) \times \text{Ratio}_{\beta\text{-range}}(\beta).$$

Fig. shows an example. The *β*-range-mapping ratio is calculated as 0.89, 0.86, 0.88, 0.86, and 0.86 when *β*-code is 0,1, 2, 3, and 4, respectively. After the mapping, we have derived the entire Digitally Controlled Oscillator period profile for a target Digitally Controlled Oscillator instance on the right-hand side. It is worthy to mention that it is easy to predict the characteristics of Digitally Controlled

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Oscillator in various operating conditions by simply repeating the timing correlation procedure. In our experience, the average estimation accuracy is less than 3% and the result is independent of the operating condition. More experiments on the estimation accuracy will be discussed in Section IV.

B. Digitally Controlled Oscillator Configuration Finder

The specification of a Digitally Controlled Oscillator in our compiler mainly includes the following two parameters:

1) the maximum/minimum clock periods and

2) the overlapping ratio between adjacent β-codes.

Digitally Controlled Oscillator with three clock-period voids (or called clock period gaps). These voids will result in potentially large jitter or frequency error when the desired target period happens to reside in the uncovered gaps. One valuable experience we have acquired during the development of an All Digital Phase Locked Loop is that such clock period voids could very likely occur during process migration, and potentially wasting a lot of efforts to solve if done by manual. An important advantage of our compiler is that we can not only solve this problem (i.e., by a robust Digitally Controlled Oscillator architecture free of clock period voids), but even better we can control the overlapping ratio of two adjacent β-codes to some extent. In our experience, 30% overlapping ratio is often adequate to avoid frequency gap completely even under various operating conditions in advanced process technology. Again, this is due to be of benefit for our quick and accurate Digitally Controlled Oscillator timing analyzer that allows the search of a very large configuration space to find out the best solution that our Digitally Controlled Oscillator can offer.

1) Configuration Space Analysis: First, we analyze the configuration number of the coarse-tuning block. As discussed previously, the coarse-tuning block is composed of one buffer and one driving-strength-tuning block formed by connecting several tri-state buffers in parallel. To compose a driving strength-tuning block, some rules (or restrictions) are adopted in our compiler.

Rule 1: The driving strength increases monotonically from bottom to top.

Rule 2: The number of the tri-state buffer types is restricted to three at most.

The number ending in a cell name (e.g., X1, X2, or X3, etc.) indicates the driving strength of the cell. The larger this number, the stronger the driving strength. Case 5 and 6 are the examples violating Rule 1 and case 7 is the one that violates Rule 2. The above two rules are mainly used to avoid the explosion of the search space. However, in our experience, the restricted configuration space is still large enough to contain some good enough Digitally Controlled Oscillator s with a high speed and a wide frequency range for most applications. The configuration space of the coarse-tuning block can be collectively expressed as follows:

$$\underbrace{(N_{\text{buf\_type}})}_{\text{term}_1} \times \Big[\underbrace{C_1^{N_{\text{tbuf\_type}}}}_{\text{term}_2} + \underbrace{C_2^{N_{\text{tbuf\_type}}} \times N_{\text{tbuf}}}_{\text{term}_3} + \underbrace{C_3^{N_{\text{tbuf\_type}}} \times C_2^{N_{\text{tbuf}}-1}}_{\text{term}_4}\Big]$$

Let *N*buf_type and *N*tbuf_type represent the numbers of types of the used buffers and the tri-state buffers, respectively. *N*tbuf is the number of tri-state buffers used in the driving-strength tuning block. Notations term2, term3, and term4 represent the number of the configurations for the three cases that contain only one type, two types, and three types of tri-state buffers in the driving-strength-tuning block, respectively. Then, the total number of the configurations of the coarse-tuning block can be calculated by multiplying the number of the types of the buffers (*N*buf_type) to the total number of the configurations of the driving-strength-tuning block (term2 + term3 + term4). In general, the total number of the configurations for the coarsetuning block (*N*coarse-tuning) is 22 096 (i.e., *N*buf_type = 4, *N*tbuf_type = 8, and *N*tbuf = 15). For the fine-tuning block, we increase the number of the two-input NAND gates gradually (e.g., 4 gates at a

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time). In general, the upper limit of the number of the two-input NAND gate is set to 100. Therefore, the number of configurations of the fine-tuning block (*N*fine-tuning) is 100/4 = 25. In addition, the numbers of the start-up gates (*N*start-up) and the delay stages (*N*stage) (consisting of one coarse-tuning block and one fine-tuning block) is also a tunable parameter. In our All Digital Phase Locked Loop compiler, both are set to 10. Therefore, the total number of the configurations of a Digitally Controlled Oscillator can be expressed as follows:

$$N_{\text{coarse - tuning}} \times N_{\text{fine - tuning}} \times N_{\text{stage}} \times N_{\text{start - up}}$$

2) Overall Flow of Digitally Controlled Oscillator Configuration Finder: The overall flow of the search process for the Digitally Controlled Oscillator is shown in Fig. 10. At first, a type of buffer contained in the coarse-tuning block is selected and the initial number of the delay stage is set to be 1. The initial configuration of the driving-strength-tuning block is composed of the tri-state buffers with the least driving strength (i.e., TBUFX1). The initial number of the two-input NAND gates (as the tunable capacitances) is set to 4 and the number would be increased gradually based on the estimated
results.

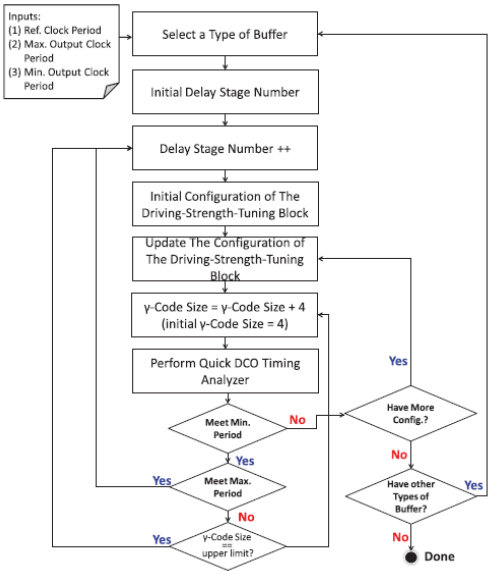

Fig. Overall flow of DCO search.

Then the proposed Digitally Controlled Oscillator timing analyzer is performed to do quick timing estimation. Based on the estimation results, the Digitally Controlled Oscillator configuration will be updated based on the following rules.

Rule 1: When the maximum clock period defined by the user is not satisfied, the number of two-input NAND gates will be increased until the upper limit is reached or to increase the number of the delay stages based on the difference between the user's target and the estimation result.

Rule 2: When the minimum clock period defined by the user is not satisfied, the tri-state buffers with higher driving strengths will be used in the driving-strength-tuning block. If the minimum clock period is still not met, then the buffer with even higher driving-strength will be adopted until there is no other buffer with higher driving strength. It is notable that the search process will not stop when the clock period range has met the user's target.

It will continue to perform minimum-area search, until it has concluded that the Digitally Controlled Oscillator with the smallest area while satisfying the user's. Specification has been found. It is mostly the case that such a configuration can also lead to lower power consumption since the number of gates that are actively switching in the Digitally Controlled Oscillator is smaller.

Simulation Results:

The design is implemented in Xilinx 14.2 and the simulation results are shown in Modelsim. The RTL design and implementation results are shown below. The top module of the design is ADPLL. Inbuilt its have the phase detector, controller, Digitally Controlled Oscillator. The design is working with the low power.

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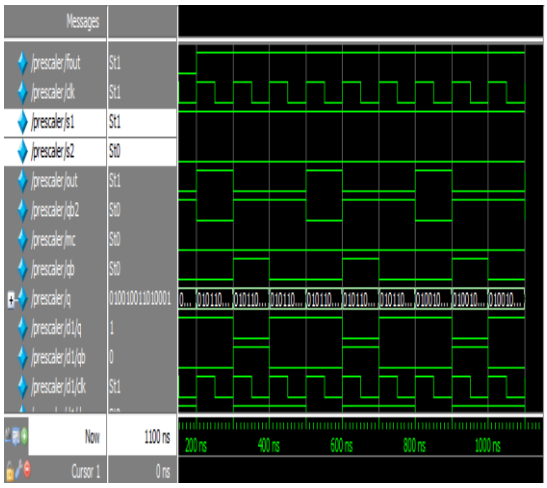

Figure: Phase detector simulation result

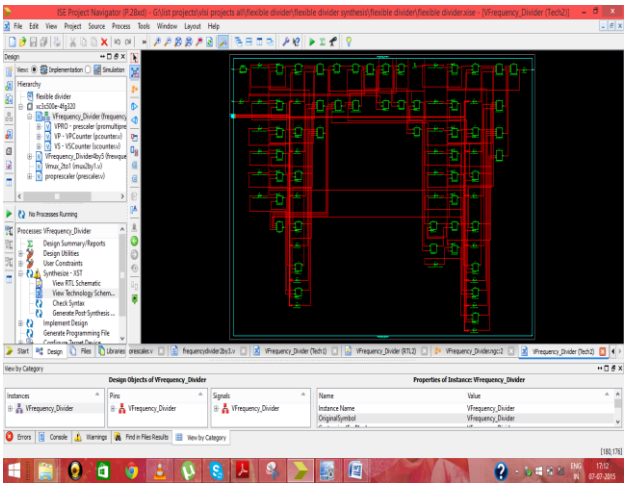

Figure: RTL Design for Proposed ADPLL

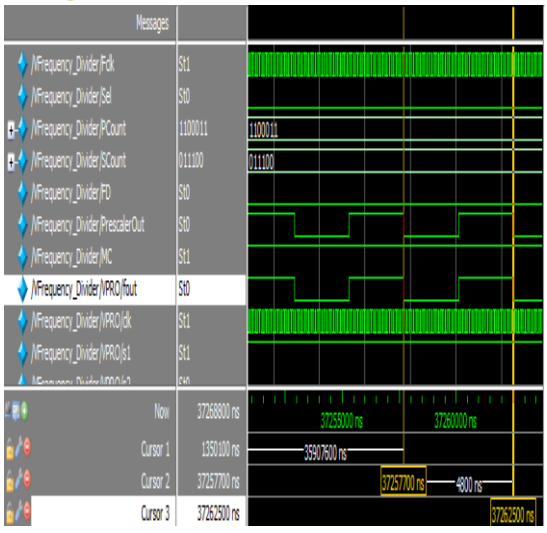

Figure: Frequency Divider

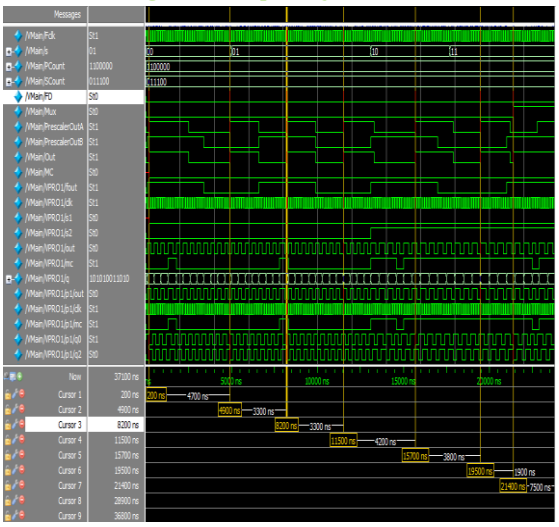

Figure: Proposed Design

Conclusion:

Here we are proposing a new design for oscillating-clock signals with the specified frequency used a total designated range. However, we are proposing the ADPLL optimization process as a search problem, during that problem we can find a good configuration that not only achieves the user defined requirement but it achieves a lower power and smaller area utilization than a manual design. The silicon design measurement parameters shows that it's a new alternative approach for Analog phase-locked loops (APLL), especially it will be developed for advanced nanometer technologies. The design is implemented in Xilinx 14.2 and its working with the low power.

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