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Impact of Sleep Transistor Channel Width on Threshold Voltage

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Abstract:

Most of the researcher said that threshold voltage is process dependant for long channel devices with respect to the different parameters such as channel length, Channel width, drain voltage VDD, and gate-source voltage. In this paper we mainly focus on the Sleep transistor Width. In this Paper, we mainly present behavior of a multi supply voltage interface circuit with respect to variation in width of the sleep transistor. most of the researchers are working on the conventional level shifter type-I .we mainly work on the Conventional level shifter Type-II. Level shifter use for effective interfacing between voltage domains supplied by different voltage level. We use Cadence Virtuoso Spectre simulator with gpdk180nm technology and doing DC and transient analysis along with timing and power analysis.

Keywords:

Level shifter, Threshold Voltage, Multi Supply Voltage.

1. Introduction:

An important value which characterizes the MOSFET transistors is the value of threshold voltage. According to the MOSFET type the value of threshold voltage can take positive and negative value. This value can be controlled during the fabrication process of MOSFET transistors. The value of the gate-to-source voltage VGS needed to create (induced) the conducting channel (to cause surface inversion) is called the threshold voltage and denoted with Vth or Vt [2],[3]. The value of the threshold voltage is dependent from some physical parameters which characterize the MOSFET structure such as Channel length, Channel width, drain voltage VDD and gate-source voltage (Vgs)[2],[3]. In CMOS circuits, the dynamic power is directly proportional to Square supply voltage.

Higher the supply voltage, the more is power consumption. Thus, the dynamic power consumption can be reduced by reducing the supply voltages, without other circuitry. However, when a low voltage circuit drives a high voltage circuit, the PMOS of the high voltage gate may not turn off completely by the low voltage "high logic" input[6],[7]. The requirement of level shifter arises here. The level-up shifters are used wherever low voltage gates drive high voltage gates. In present devices, more circuits can be designed on a single chip.

However, the major concern is related to the fact that different gates can use different voltage levels. The output from a low voltage gate can be connected to the input of a high voltage gate . Here the level shifter circuits have to be the major component of the CMOS devices[6]. In multi-voltage Voltage devices multiple blocks work on different voltages[7]. Therefore, level shifters are necessary when signal passes from one block to another block. In this Paper, we mainly present behavior of a multi supply voltage interface circuit with respect to variation in width of the sleep transistor. Optimization of level shifter for low power can lead to overall power reduction of the chip to greater extend.

2. Literature Review

2.1. Multi Supply Voltage Issues:

In multi-voltage Voltage devices multiple blocks work on different voltages. Therefore, level shifters are necessary when signal passes from one block to another block. In this Paper, we mainly present behavior of a multi supply voltage interface circuit with respect to variation in width of the sleep transistor. Optimization of level shifter for low power can lead to overall power reduction of the chip to greater extend[1].

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A level shifter acts as an interface circuit between low and high Voltage Island to shift signal from LOW voltage level to HIGH voltage level and vice versa as shown in figure 1. Many level shifter circuits have been proposed in the literature [7]for MSV architecture chips. But the concept of using dual-VDD level shifter can be used to reduce the power consumption of the circuit on whole to large extent.

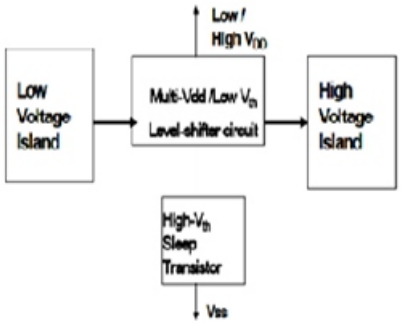

Fig 1- Block Diagram of multi-Vdd with level shifter

2.2Conventional level shifter type-I:

The conventional level shifter type-I using cross-coupled PMOS load is shown in Fig.1 Two transistor are used for the differential input . if input to MN2 is 0 then input to MN1 should 1[7]. Sleep ctrl is always 1 for continuous turn on sleep transistor. If PM2 is off then no output at the output and if PM2 is on Vout is present.PM1, PM2, MN1,MN2 and sleep Transistors are High voltage transistors select it in from gpdk180n foundry[7].

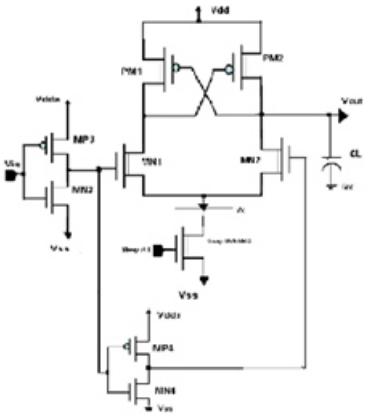

Fig 2- Conventional level shifter-I

3. Proposed System

3.1.Conventional barrel shifter-II

The only difference in this type is MN1 and MN2 are convert in to high voltages that means they are thin gate oxide-transistors.and vdda is 1.65v,vdd is 3.6V operationg at 100MHz along with load 0.01µf. This level shifter is of importance as it can shift voltage levels from high to low and viseversa. It consists of two inverters and flop. The feedback inverter is used for giving inverted logic to MN2. voltage VDD. Sleep transistor is used to provide least resistance path for short circuit and leakage currents. In this paper we mainly focus on behavior of level shifter circuit by varying Aspect ratio. The most important parameter is the threshold voltage[1].

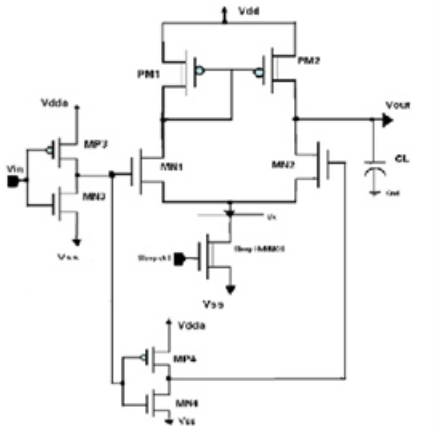

Fig 3-Conventional level shifter-II

4. Result and Discussion:

Level shifter circuit has been simulated for different values of channel width and fixed channel length of L=180nm and L=360 nm. The design parameters chosen for the circuit simulation are as given: CL =0.01pF, Operating frequency fo=100MHZ, Vdda (Low) =1.65V, Vdd(high)=3.6V , temperature=27°C. The input signal given to the circuit is a square waveform of 1.8 volts.

4.1.Transient and Dc Response for the circuit:

Dc response is a response when we applying a constant supply in transient analysis constant supply is vary by applying a square waveform of 1.8v in gpdk180nm technology.

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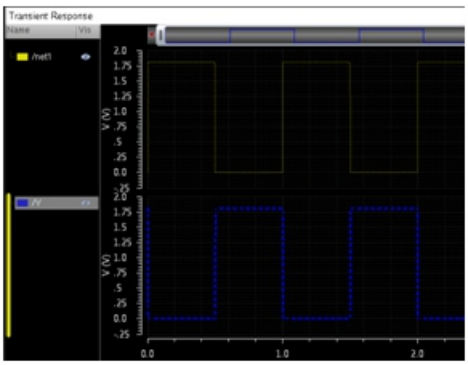

Fig 4-Transient Response for the circuit

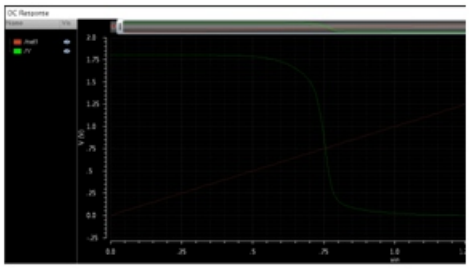

Fig 5-DC Response for the circuit

4.2.Threshold Variation with channel width variation

Table 1 shows the influence of varying channel width on threshold voltage.

Sr no.	Channel width in µm	Vth(mv) for 180nm	Vth(mv) for 180nm
1	1.5	515.039	645.420
2	2	481.674	612.056
3	5	422.180	552.563
4	10	402.509	532.891
5	15	395.969	526.351
5	20	392.303	523.084
6	30	389.439	519.820
7	40	387.807	518.188
8	50	386.828	517.210

Table.1- Variation of Threshold Voltage with respect to channel width of Sleep transistor

4.CONCLUSION:

The dependency of Vth on Channel width can be exploited to design low power, high performance circuits. Multi-Vdd are becoming very popular giving rise to other design issues, From above results we conclude and propose that, the variation in threshold voltage by changing channel width can be used for Multi-Vdd Circuit designs for Level shifter circuit.

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