



## Buck–Boost Voltage/Current Source Inverter with Space Vector Pulse width Amplitude Modulation.

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### ABSTRACT:

*This paper proposes a space vector pulse width amplitude modulation (SVPWAM) method for a buck–boost voltage/current source inverter. For a voltage source inverter, the switching loss is reduced by 87%, compared to a conventional sinusoidal pulse width modulation (SPWM) method. For a current source inverter, the switching loss is reduced by 60%. In both cases, the power density is increased by a factor of 2 to 3. In addition, it is also verified that the output harmonic distortions of SVPWAM is lower than SPWM, by only using one-third switching frequency of the latter one. A 1-kW boost-converter-inverter prototype has been built and tested using this modulation method. The maximum overall system efficiency of 96.7% has been attained at full power rating. The whole system power density reaches 2.3 kW/L and 0.5 kW/lb. The numbers are remarkable at this power rating. As a result, it is feasible to use SVPWAM to make the buck–boost inverter suitable for applications that require high efficiency, high power density, high temperature, and low cost. Such applications include electric vehicle motor drive or engine starter/alternator.*

*Index Terms—Buck-boost, SVPWAM, switching loss reduction, THD.*

### INTRODUCTION:

Currently, two existing inverter topologies are used for hybrid electric vehicles (HEVs) and electric vehicles (EVs): the conventional three-phase inverter with a high voltage battery and a three-phase pulse width modulation (PWM) inverter with a dc/dc boost front

end. The conventional PWM inverter imposes high stress on switching devices and motor thus limits the motor's constant power speed range (CPSR), which can be alleviated through the dc–dc boosted PWM inverter. Fig. 1 shows a typical configuration of the series plug-in electric vehicle (PHEV). The inverter is required to inject low harmonic current to the motor, in order to reduce the winding loss and core loss. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the switching loss increase in switching device and also the core loss increase in the motor stator. To solve this problem, various soft-switching methods have been proposed. Active switching rectifier or a diode rectifier with small DC link capacitor have been proposed in . Various types of modulation method have been proposed previously such as optimized pulse-width-modulation [improved Space-Vector-PWM control for different optimization targets and applications , and discontinuous PWM (DPWM). Different switching sequence arrangement can also affect the harmonics, power loss and voltage/current ripples. DPWM has been widely used to reduce the switching frequency, by selecting only one zero vector in one sector. It results in 50% switching frequency reduction.

### Existing System:

The principle of an SVPWAM control is to eliminate the zero vector in each sector. The modulation principle of SVPWAM is shown in Fig. 2. In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the

adjacent two sectors. For example, in sector VI and I, phase leg A has no switching at all. The dc-link voltage thus is directly generated from the output line-to-line voltage. In sector I, no zero vector is selected. Therefore,  $S_1$  and  $S_2$  keep constant ON, and  $S_3$  and  $S_6$  are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltage  $V_{ac}$  at this time. Consequently, the dc-link voltage should present a  $6\omega$  varied feature to maintain a desired output voltage. The corresponding waveform is shown in solid line in Fig. 3. A dc-dc conversion is needed in the front stage to generate this  $6\omega$  voltage, where  $\theta \in [0, \pi/3]$  is relative angle from the output voltage vector to the first adjacent basic voltage vector like in Fig. 2. If the time period for each vector maintains the same, the switching frequency will vary with angle, which results in a variable inductor current ripple and multi frequency output harmonics

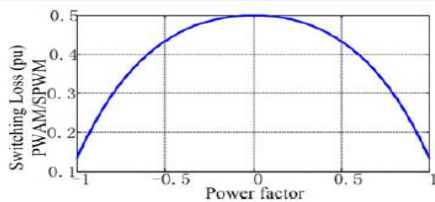


Fig. 6. (SVPWAM power loss/SPWAM power loss) versus power factor in VSI.

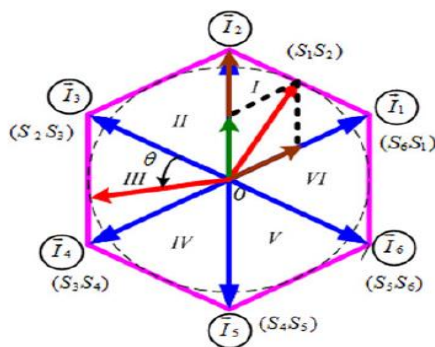


Fig. 7. Conventional CSI and its corresponding SVPWAM diagram.

**Proposed System:**

**Principle of SVPWAM in CSI**

The principle of SVPWA Min CSI is also to eliminate the zero vectors. As shown in Fig. 7, for each sector, only two switches are doing PWM switching, since only one switch in upper phase legs and one switch in lower phase legs are conducting together at any

moment. Thus, for each switch, it only needs to do PWM switching in two sectors, which is one-third of the switching period. Compared to SVPWM with single zero vector selected in each sector, this method brings down the switching frequency by one-third.

**Inverter Switching Loss Reduction for CSI**

In CSI, the current stress on the switch is equal to the dc link current, and the voltage stress is equal to output line-to-line voltage, as shown the shadow area in Fig. 8. Thus, the switching loss for a single switch is determined by. When compared to discontinuous SVPWM, if the half switching frequency is utilized, then the switching loss of it becomes half of the result.

**SPECTRUM ANALYSIS OF SVPWAM**

A fair comparison in switching loss should be based on an equal output harmonics level. Thus, the switching loss may not be reduced if the switching frequency needs to be increased in order to compensate the harmonics. For example, discontinuous SVPWM has to have double switching frequency to achieve the same THD as continuous PWM. So the switching loss reduction is much smaller than 50%. Therefore, for the newly proposed SVPWAM, a spectrum analysis is conducted to be compared with other methods on the basis of an equal average switching frequency.

**Spectrum Comparison Between SVPWAM, SPWM, and SVPWM**

The object of spectrum analysis is the output voltage or current before the filter. The reason is that certain orders of harmonics can be eliminated by sum of switching functions in VSI or subtraction of switching functions in CSI. The comparison is between SVPWAM, DPWM, and continuous SVPWM in VSI/CSI. The switching frequency selected for each method is different, because the comparison is built on an equalized average switching frequency over a whole fundamental cycle, in order to make the harmonics comparable at both low modulation and high modulation range.

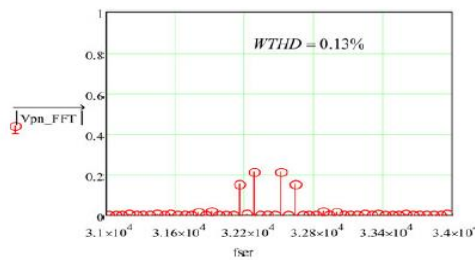


Fig. 14. Spectrum of SVPWAM at switching frequency.

## TOPOLOGIES FOR SVPWAM

Basically, the topologies that can utilize SVPWAM have two stages: dc–dc conversion which converts a dc voltage or current into a  $6\omega$  varied dc-link voltage or current; VSI or CSI for which SVPWAM is applied. One typical example of this structure is the boost converter inverter discussed previously. However, the same function can also be implemented in a single stage, such as Z/quasi-Z/trans-Z source inverter.

## CASE STUDY: 1-KWBOOST-CONVERTER INVERTER FOR EV MOTOR DRIVE APPLICATION

### Basic Control Principle

The circuit schematic and control system for a 1-kW boost converter inverter motor drive system is shown in Fig. 15. A  $6\omega$  dc-link voltage is generated from a constant dc voltage by a boost converter, using open-loop control. Inverter then could be modulated by a SVPWAM method. The specifications for the system are input voltage is 100–200 V; the average dc-link voltage is 300 V; output line-to-line voltage rms is 230 V; and frequency is from 60 Hz to 1 kHz.

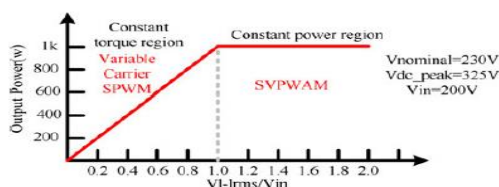


Fig. 16. Operation region of boost-converter-inverter EV traction drive.

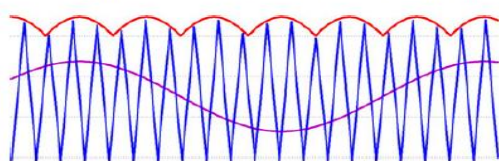


Fig. 17. Variable carrier SPWM control in buck mode.

## CONCLUSION

The SVPWAM control method preserves the following advantages compared to traditional SPWM and SVPWM method.

1) The switching power loss is reduced by 90% compared with the conventional SPWM inverter system.

2) The power density is increased by a factor of 2 because of reduced dc capacitor (from 40 to 6  $\mu$ F) and small heat sink is needed.

3) The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress.

A high-efficiency, high-power density, high-temperature, and low-cost 1-kW inverter engine drive system has been developed and tested. The effectiveness of the proposed method in reduction of power losses has been validated by the experimental results that were obtained from the laboratory scale prototype.

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