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A New Control Scheme for the FCI by Using Dynamic Voltage Restorer

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Abstract:

The paper presents a controlscheme for the purpose of interruptingthe fault current by the DVR (DynamicVoltage Restorer) which is present ondown-stream side of the DVR. Thecontrol scheme provides compensation forthe voltage sags. PLL is not required inthis scheme and it can control themagnitude and phase angle of the injectedvoltage independently.

To estimate themagnitude and phase of the measured voltages, FLES digital filters are used. These are capable of to reduce the impacts of noise and harmonics. The simulation is performed in the MATLAB/simulink software. The proposed scheme i) can interrupt the fault-current within two cycles ii) limits the dc link voltage rise so that no restrictionsiii)gives satisfactory operation under arcing fault conditions also iv) can interrupt the fault current under low dclink voltage conditions.

Index Terms:

Dynamic voltage restorer (DVR),fault current interrupting, multiloop control.

I.INTRODUCTION:

DVR is used to counteract voltage sags by injecting controlled three-phase acvoltages in series with the supply voltageand to enhance the quality of voltage byadjusting voltage magnitude, wave shapeand phase angle [3]-[6]. In general, DVR isbypassed during down-stream fault in orderto protect the components of the DVRagainst the high fault currents [9]-[11].

A control scheme for DVR tofunction as fault current limiter is providedin [9]. The main drawback of this scheme isthat the dc link voltage rise due to real power absorption. The dc link voltage risecan be mitigated at the cost of a slowdecaying dc fault current component usingthe methods proposed in [7] and [12].To overcome the limitations whichare mentioned above, this paper introduces acontrol strategy for DVR such that voltagesag compensation under balanced and unbalanced conditions and a function ofinterrupting the fault current.

The formerfunction has been presented in and the latter is in this paper. Limiting fault current by the DVR disables the main and backupprotection (e.g. over current relay). This canresult in prolonging the duration fault. Thus,it is preferred to reduce the fault current tozero and send a trip signal to the upstreamrelay.

FCI function requires 100% voltageinjection capability. Thus, power ratings ofthe series transformer and the VSC would bethree times the conventional DVR. Thiswould result in more expensive DVRsystem. Economic feasibility of such a DVRdepends on the importance of the loadprotected by the DVR and the cost of DVRitself.

The performance of the proposedcontrol strategy is evaluated throughsimulation in MATLAB/Simulink. Theresults indicate that the proposed scheme i)can interrupt the fault current within two cycles ii) limits the dc link voltage rise so that no restrictions iii)gives satisfactory operation under arcing fault conditions also iv) can interrupt the fault current under low dc link voltage conditions.

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II.PROPOSED SYSTEM:

Fig. 1 represents a s diagram of the test system which is used to evaluate the performance of theproposedDVR control syste different fault conditions, in theMATLAB/ Simulink software. A 525 DVRsystem is installed on the 0.4feeder, to protect a 500-kVA,0.90 laggingpower factor load against voltage sags.

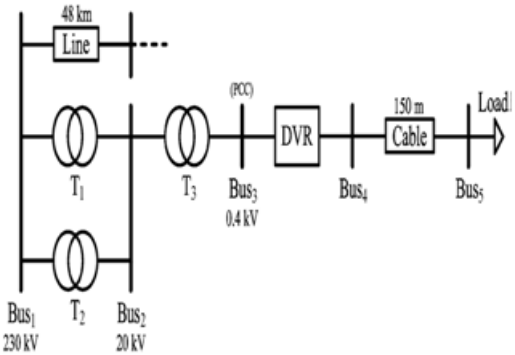

Fig. 1. Single-line diagram of the system used for simulation studies.

THE BASIC ELEMENTS OF A DVR:

• Converter; The converter is most likely a Voltage Source

Converter (VSC),which Pulse Width modulates (PWM) the DC from the DC-link/storage toAC-voltages injected into the system.

• Line-filter; The line-filter is inserted to reduce the switching harmonics generatedby the PWM VSC.

• Injection transformer; In most DVR applications the DVR is equipped withinjection transformers to ensure galvanic isolation and to simplify the convertertopology and protection equipment.

• DC-link and energy storage; A DC-link voltage is used by the VSC to synthesizean AC voltage into the grid and during a majority of voltage dips activepower injection is necessary to restore the supply voltages.

• By-pass equipment; During faults, overload and service a bypasspath for theload current has to be ensured

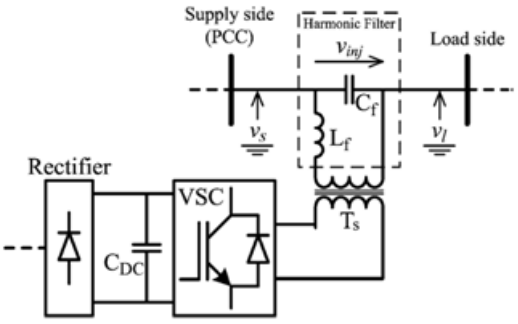

Fig. 2. Schematic diagram of a DVR with a line-side harmonic filter.

III.CONTROL STRATEGY:

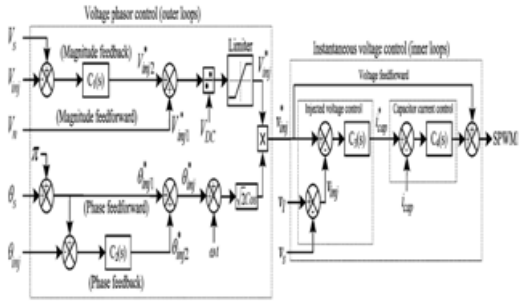

Fig. 3. Per-phase block diagram of the DVR control system in FCI mode.

The DVR converter consists of three independent H-bridge VSCs that are connected to a common dc link capacitor.These VSCs are connected in series to the supply grid. The control scheme consists of three independent and identical controllers' one for each VSC of the DVR.

Assume
supply voltage vs = Vs
load voltage vl = Vl
injected voltage vinj= vl-vs = Vinj
For the estimation of magnitudes and phase angles of the phasors corresponding to v and vinj, two identical least error squares filters are used.

VOLTAGE PHASOR CONTROL SYSTEM:

In the FCI operation mode, the required injected voltage phasor is equal to the source voltage phasor but in phaseopposition. The performance in terms oftransient response, speed and steady-stateerror is enhanced by independent control ofthe magnitude and phase.

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The steady-stateerrors of magnitude and phase of theinjected voltage can be eliminated by usingtwo PI controllers (C1 and C2). Parametersof each controller are determined to achieve a fast response with zero steady-state error. The output of voltage phasor control systemis a reference phasor V*inj.The magnitude- and phase angle of V*inj are independentlycalculated and passed through a limiter. Theresulting magnitude and phase angle areconverted to the sinusoidal signal V*inj andis given as a reference signal to the instantaneous voltage control.

INSTANTANEOUS VOLTAGE CONTROL SYSTEM:

Under ideal conditions, voltage sag compensation is done if the output of the output of the phasor based controller V*inj isdirectly fed to the SPWM unit. However,resonances of harmonic filter can't beeliminated. Therefore, to improve dynamicresponse and stability of the DVR, aninstantaneous injected voltage controller anda harmonic filter capacitor current controllerare used to attenuate resonances. Thegenerated reference signal V*inj is comparedwith the measured injected voltage Vinj andthe error is fed to the voltage controller. Theoutput of the voltage controller i*cap acts as areference signal for the filter capacitorcurrent control loop. This i*cap is comparedwith the measured capacitor current icap, anderror is fed to the current controller.

Thesteady state error of the system is fullyeliminated by the PI controller in the outercontrol loop. Therefore, there is no need forhigher order controllers in the inner controlloop. If a large value of kv is used, it resultsin amplification of the DVR filter resonanceand has adverse impact on the systemstability [18]. Thus, the transient response ofthe DVR is enhanced by feed forward loopand a small proportional gain isutilized asthe voltage controller. A large kc damps theharmonic resonance but it is limited bypractical considerations. Therefore thelowest value of the proportional gain whichcan effectively damp the resonances is used. The output of the current controller is added to the feed forward voltage to derive the signal for the PWM generator. In FCI mode, the injected voltage phasor should be equal to the source voltage phasor but in opposite direction.

The voltage phasor control block consists of two PI controllers(C1 and C2) that are used toeliminate steady state errors of themagnitude and phase of the injected voltage.The output phasor of this block is V*(inj). Tomake the injected voltages free from theeffect of dc-link voltage variations, V*(inj)normalized by Vdc. Ideally voltage sagcanbe compensated effectively if the output ofvoltage phasor control is directly fed to thesinusoidal pulse width modulation(SPWM)unit. However, resonances of harmonic filtercan't be eliminated.Therefore to improvetransient stability and dynamic response ofDVR, an instantaneous injected voltagecontroller and a harmonic filter capacitorcurrent controller are used to attenuateresonances. The generated reference signalfor V*(inj) is compared with the measured injected voltageV(inj) and error is given to voltage controller.

IV SIMULATION RESULTAS:

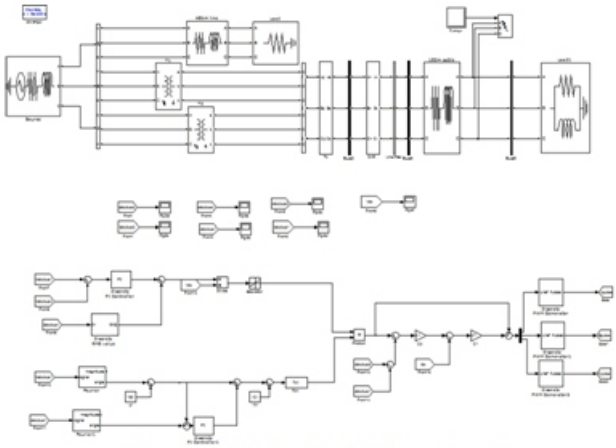

Fig 4 Mat lab simulation circuit

THREE PHASE FAULT WAVEFORMS WHEN THE DVR IS INACTIVE

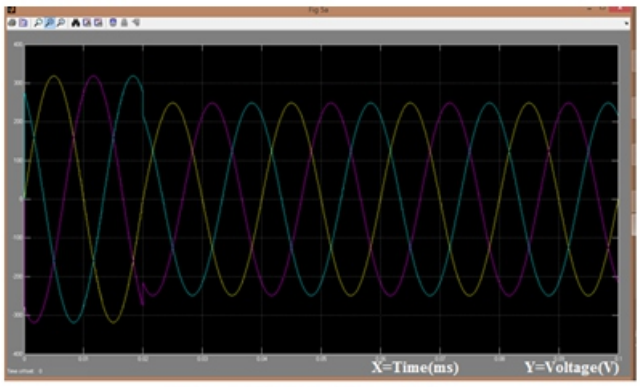

Fig.5 (a) Voltages at Bus3

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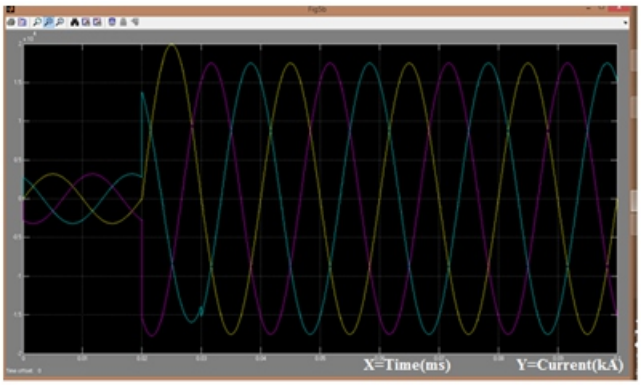

Fig.5 (b) Fault currents, during downstream 3-ph fault when the DVR is inactive (bypassed).

THREE PHASE DOWNSTREAM FAULT WAVEFORMS

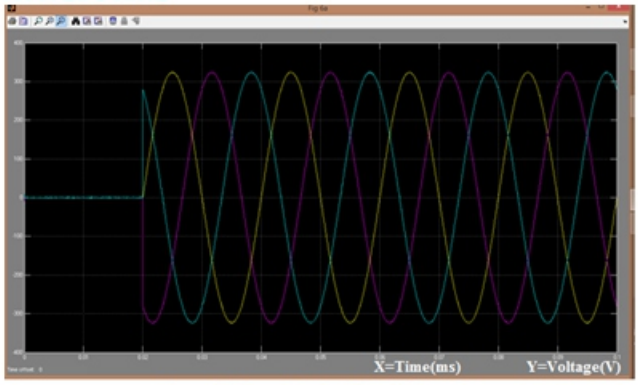

Fig.6 (a) Injected voltages.

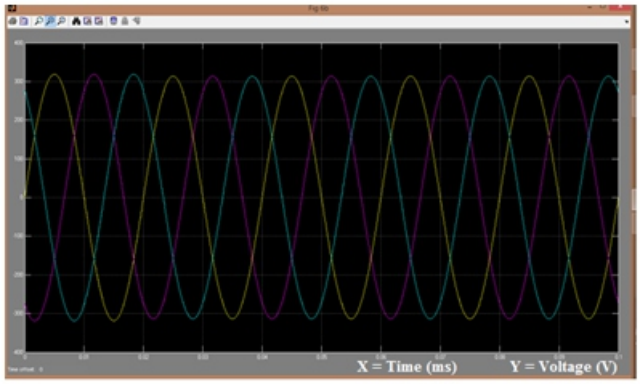

Fig.6 (b) Source voltages

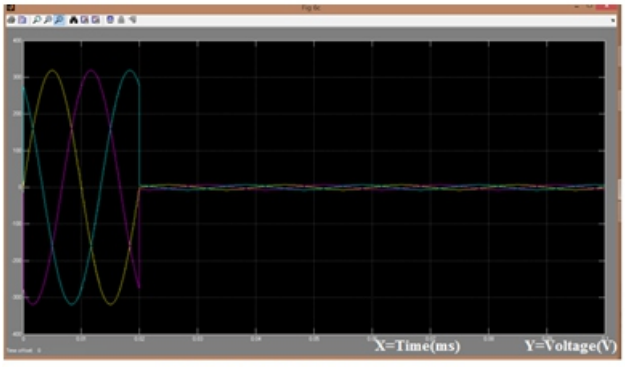

Fig.6 (c) Load voltages.

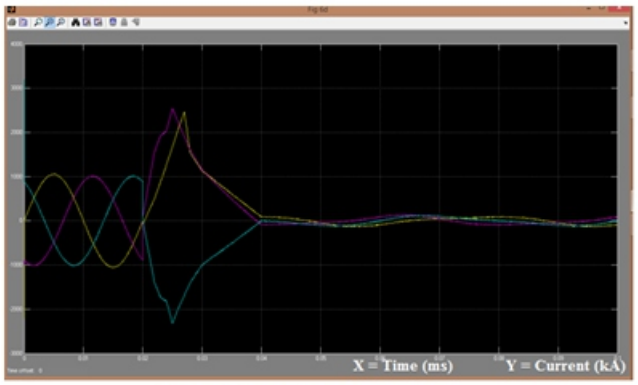

Fig.6 (d) Line currents.

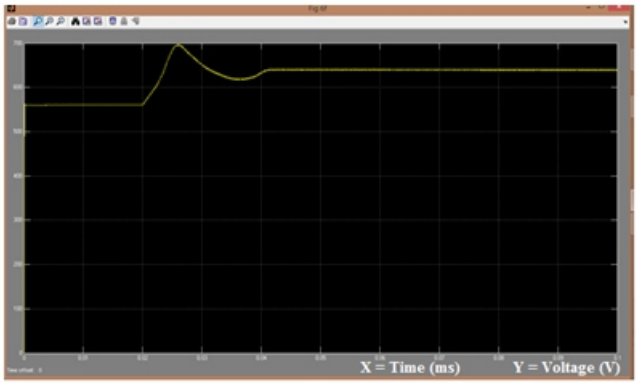

Fig.6 (e) DC-link voltage, during the three-phase downstream fault.

PHASE TO PHASE FAULT WAVEFORMS WHEN DVR INACTIVE

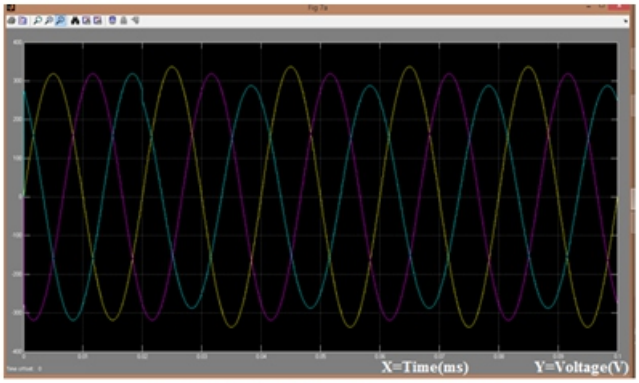

Fig.7 (a) Voltages at Bus3.

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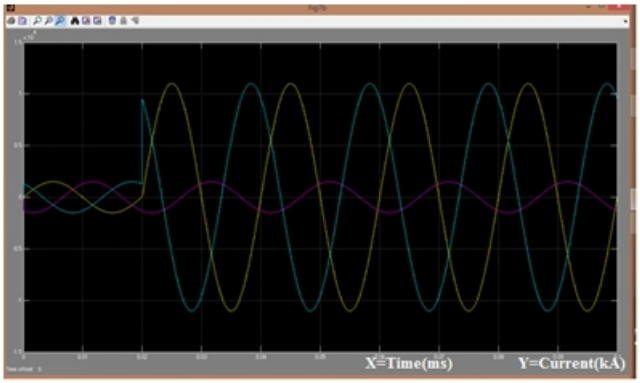

Fig.7 (b) Fault currents, during downstream phase-phase fault when the DVR is inactive (bypassed).

PHASE TO PHASE DOWNSTREAM FAULT WAVEFORMS

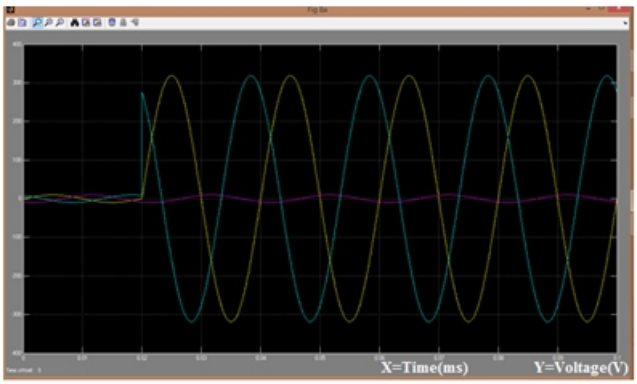

Fig.8 (a) Injected voltages.

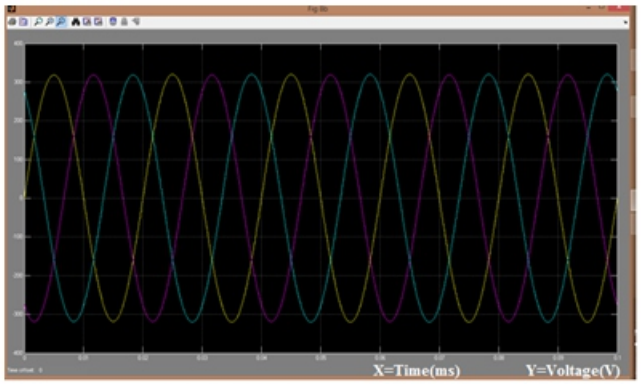

Fig.8 (b) Source voltages.

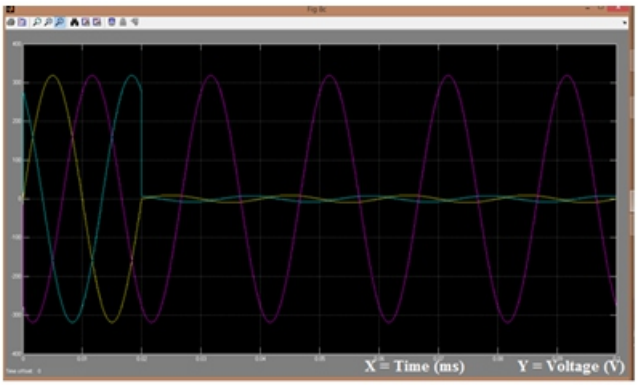

Fig.8 (c) Load voltages.

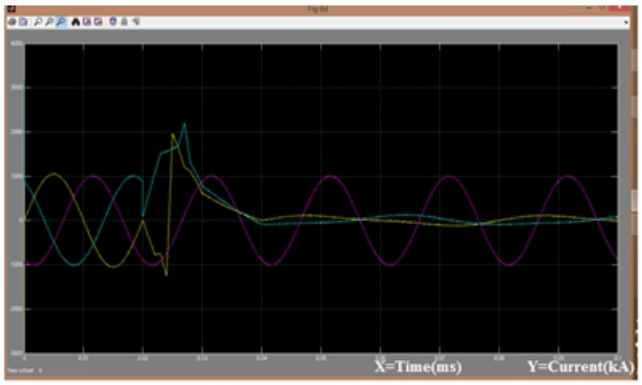

Fig.8 (d) Line currents.

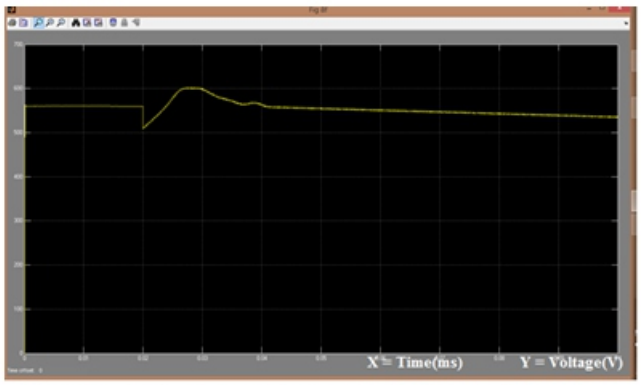

Fig.8 (e) DC-link voltage, during the phase-to-phase downstream fault.

SINGLE PHASE TO GROUND FAULT WAVEFORMS WHEN DVR INACTIVE

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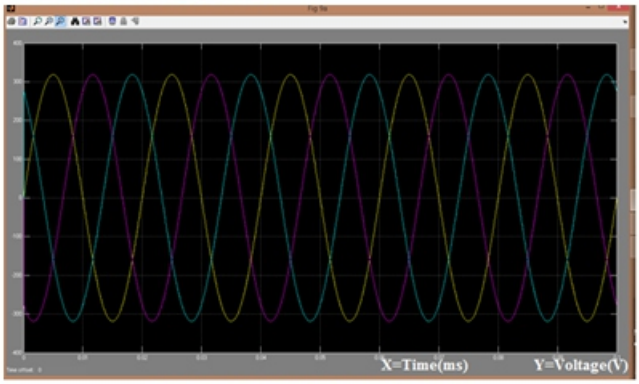

Fig.9 (a) Voltages at Bus3.

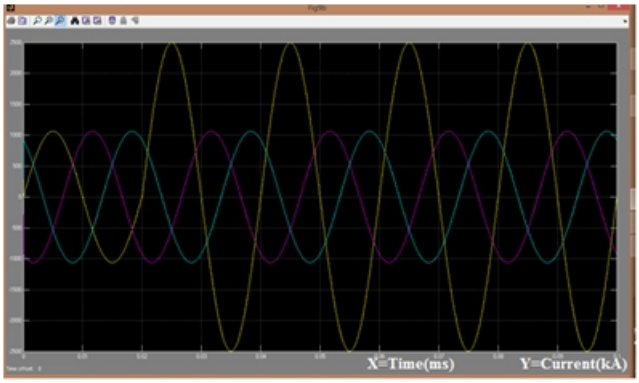

Fig.9 (b) Fault currents, during phase -to-ground downstream fault when DVR is inactive

SINGLE PHASE TO GROUND DOWNSTREAM FAULT WAVEFORMS

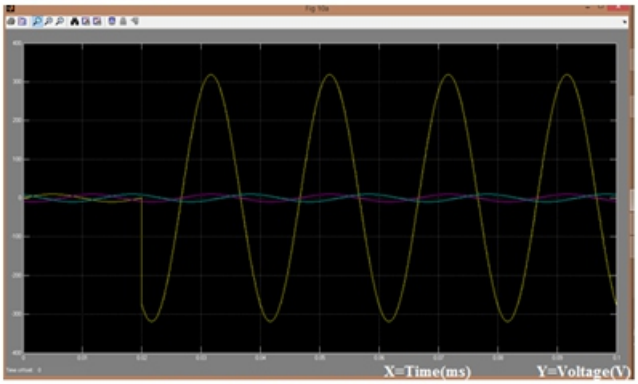

Fig.10 (a) Injected voltages.

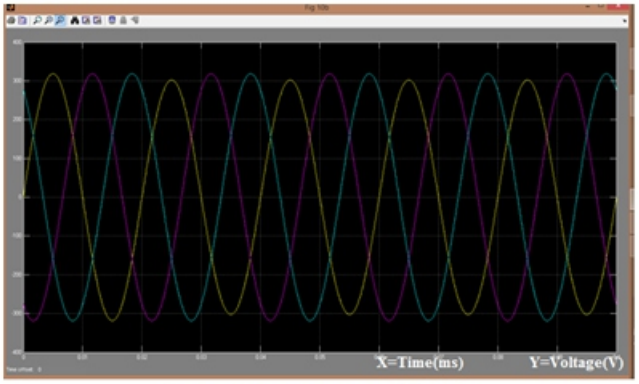

Fig.10 (b) Source voltages.

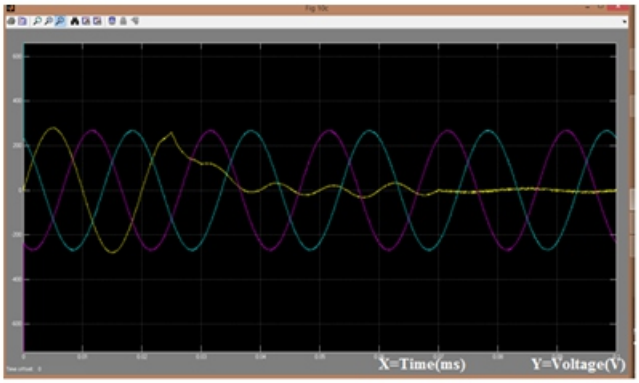

Fig.10 (c) Load voltages.

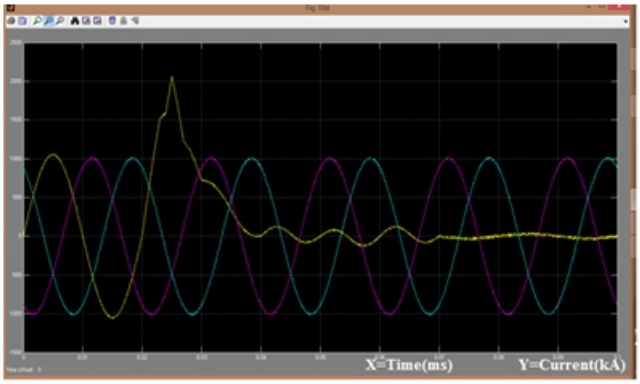

Fig.10 (d) Line currents.

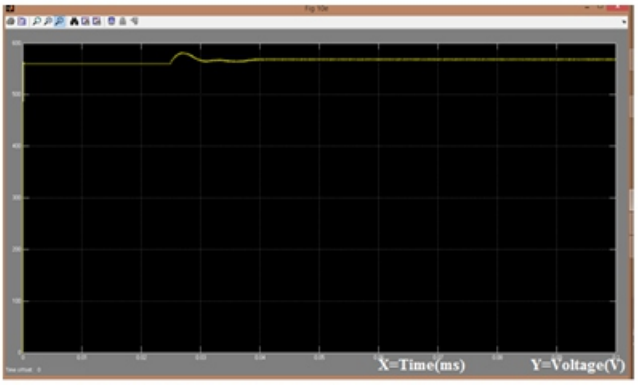

Fig.10 (e) DC-link voltage, during the single-phase-to-ground downstream fault.

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SINGLE PHASE TO GROUND ARCING FAULT WHEN DVR IS INACTIVE

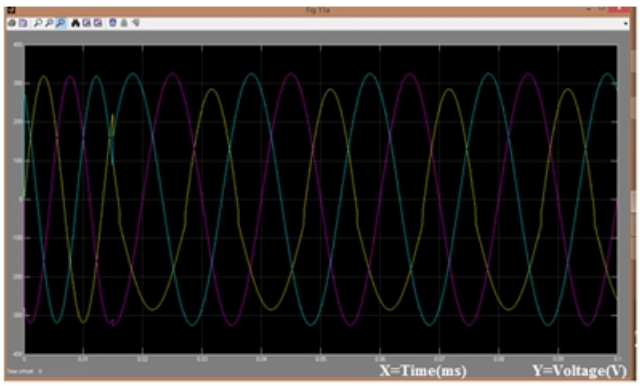

Fig.11 (a) Voltages at Bus3.

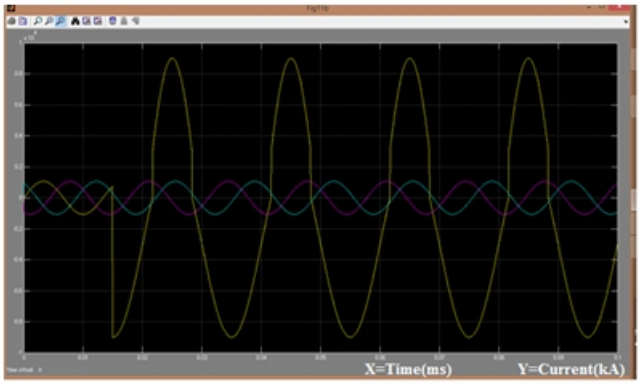

Fig.11 (b) Fault currents, during phase -ground downstream fault when DVR is bypassed.

EFFECT OF THE FAULT V-I CHARACTERISTICS WAVEFORMS

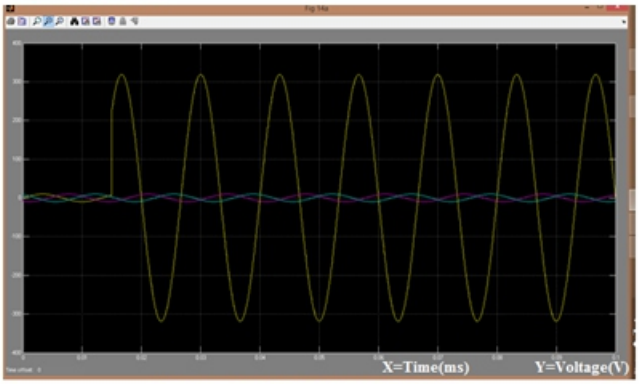

Fig.12 (a) Injected voltages.

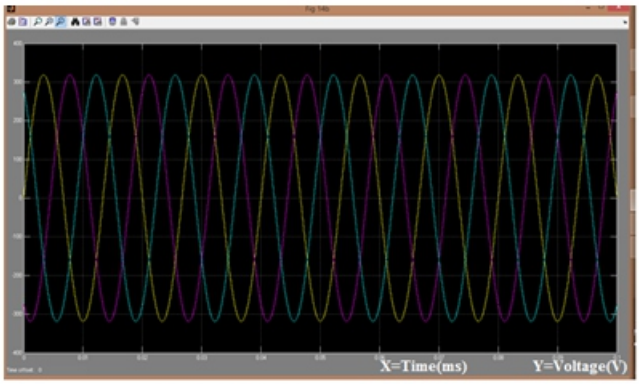

Fig.12 (b) Source voltages.

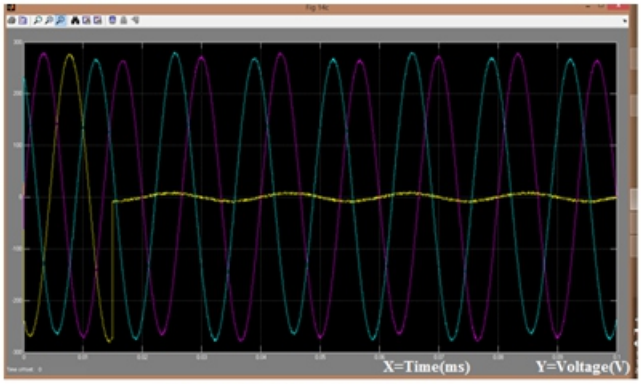

Fig.12 (c) Load voltages.

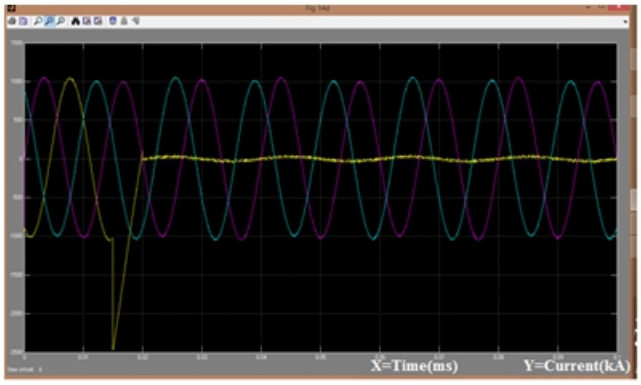

Fig.12 (d) Line currents.

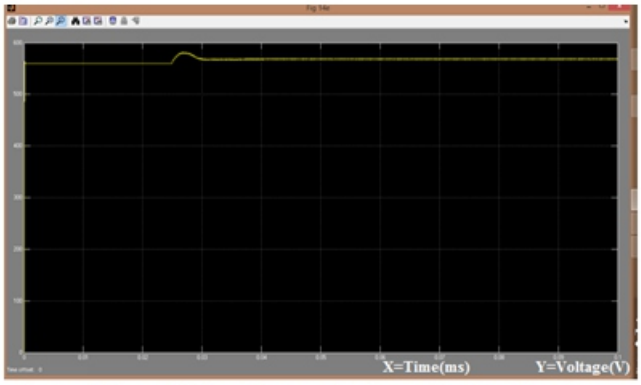

Fig.12 (e) DC-link voltage, during the single-phase-to-ground downstream arcing fault.

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SIMULTANEOUS FCI OPERATION AND SAG COMPENSATION WAVEFORMS

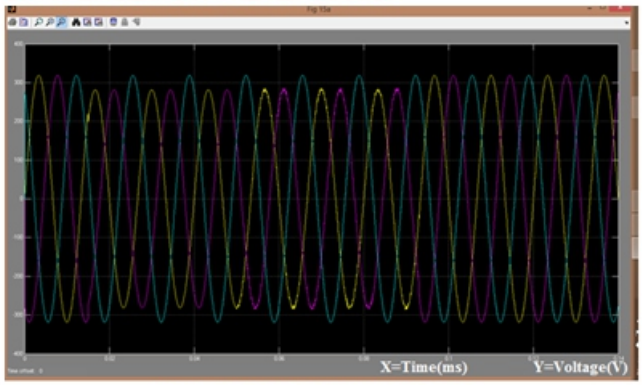

Fig.13 (a) Source voltages

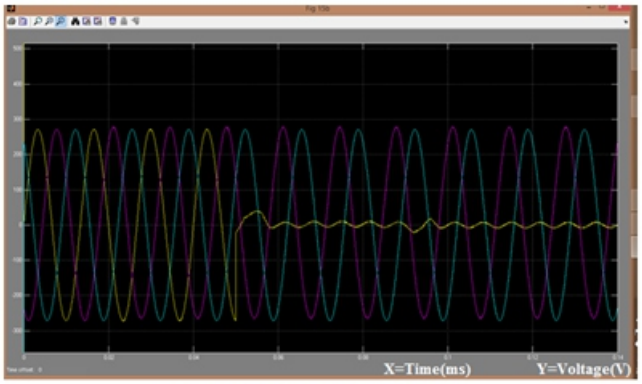

Fig..13 (b) Load voltages.

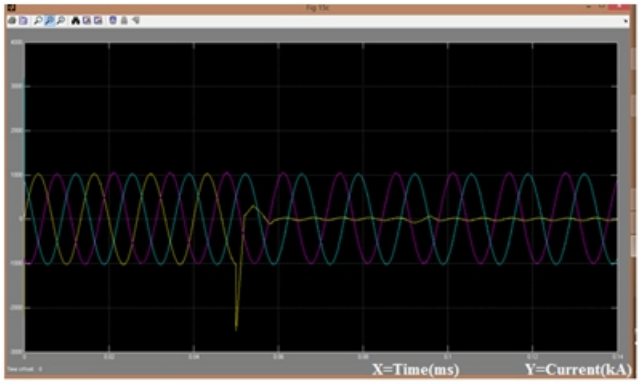

Fig..13 (c) Line currents.

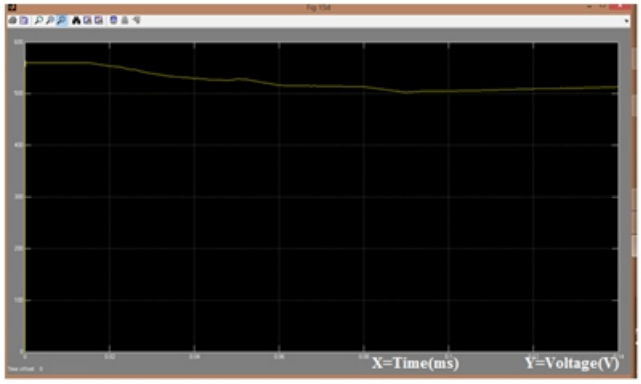

Fig.13 (d) DC-link voltage, during phase-A to ground downstream fault which takes place during sag compensation in phases A and B.

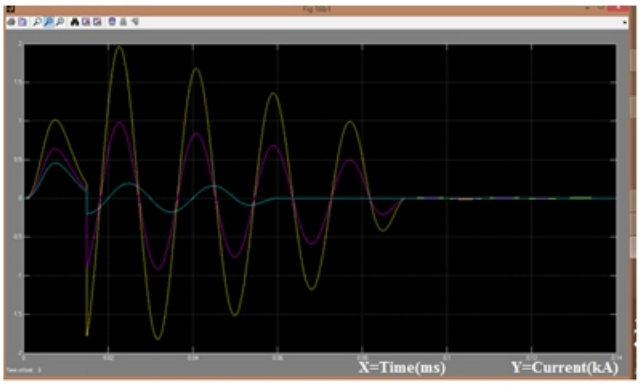

Fig.14 (a) Line current of phase-A

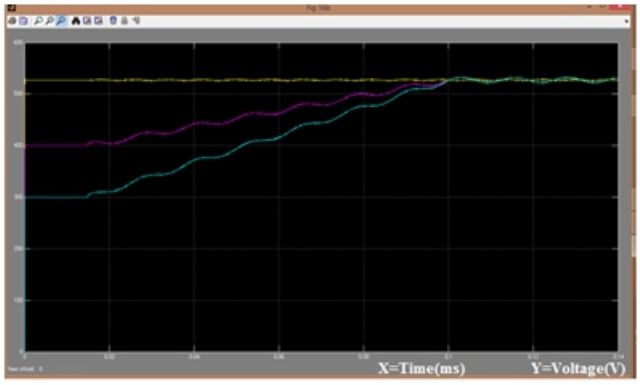

Fig.14 (b) dc-link voltage, for different initial values of the dc-link voltage, during downstream phase-A-to-ground fault.

V. CONCLUSION:

In this paper, the simulation of a DVR is done using MATLAB SIMULINK software. Thus it became easier to construct the large distribution network and analyse the performance DVR under different fault conditions. The controlling of DVR is done with the help of PI controller. The simulation results clearly showed the performance of the DVR in improving the quality of voltage due to faults in distribution system. DVR is one of the fast and effective custom power device has shown the efficiency and effectiveness on voltage sag and swell compensation hence it makes DVR to be an effective power quality improvement Device. This has been proved through simulation implementation.

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