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A novel SVPM for vehicle Buck–Boost Voltage Inverter

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Abstract:
This paper proposes a space vector pulse width amplitude modulation (SVPWAM) method for a boost voltage source inverter. For a VSI, the switching loss is reduced when compared to a conventional sinusoidal pulse width modulation (SPWM) method. The output harmonic distortion of SVPWAM is lower than that of the SPWM, by using only one-third of the switching frequency compared to the latter one. As a result, it is feasible to use SVPWAM to make the boost inverter suitable for applications that needs high power density, high efficiency and low cost. The application includes DC power source utilization, power grid, induction heating and electric vehicle motor drive.

I. INTRODUCTION

In recent days the grid tie inverter technology has a vast development. Here the solar power which is a dc is converted to ac for tying with the grid. The inverter is required to inject low harmonic current to, in order to increase the efficiency. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the increase in switching loss in the switching device.

To rectify this problem, different types of soft-switching methods have been proposed in [1]–[3].A diode rectifier with small DC link capacitor have been proposed in [4], [5], [8]–[12]. various types of modulation techniques have been proposed previously such as optimized pulse-widthmodulation

in [13], improved Space-Vector-PWM control for different optimization targets and applications [14]–[16], and discontinuous PWM (DPWM) [17]. Different switching sequence arrangement can also affect the harmonics, power loss and voltage/current ripples [18]. DPWM has been widely used to reduce the switching frequency, by selecting only one zero vector in one sector. It results in 50% switching frequency reduction. However, if the same output THD is required, DPWM cannot reduce switching loss compared to SPWM. It will also worsen the device heat transfer because the temperature variation. A double 120 flattop modulation method has been proposed in [6] and [7] to reduce the period of PWM switching to only 1/3 of the whole fundamental period. In addition to that, the method is only specified to a fixed topology, which cannot be applied widely. Fig. 1 shows a typical configuration of the series plug-inelectric vehicle (PHEV). The inverter is required to inject lowharmonic current to the motor, in order to reduce the windingloss and core loss. For this purpose, the switching frequency ofthe inverter is designed within a high range from 15 to 20 kHz,resulting in the switching loss increase in switching device andalso the core loss increase in the motor stator. To solve thisproblem, various soft-switching methods have been proposed[1]–[3]. Active switching rectifier or a diode rectifier with small

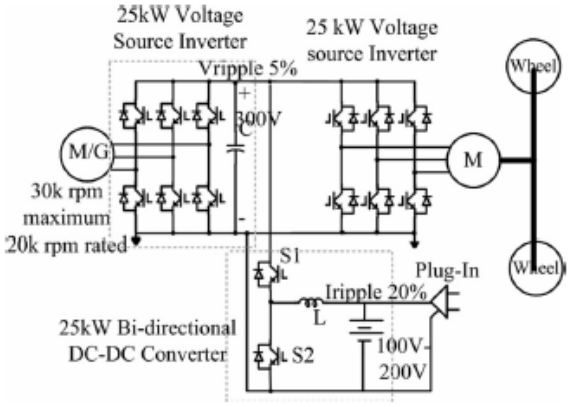

Fig.1. Typical configuration of a series PHEV.

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DC link capacitors have been proposed in [4], [5], [8]–[12].Varies types of modulation method have been proposed previouslysuch as optimized pulse-width-modulation [13], improvedSpace-Vector-PWM control for different optimization targetsand applications [14]–[16], and discontinuous PWM (DPWM)[17]. Different switching sequence arrangement can also affectthe harmonics, power loss and voltage/current ripples [18].DPWMhas been widely used to reduce the switching frequency,by selecting only one zero vector in one sector. It results in50% switching frequency reduction. However, if an equal outputTHD is required, DPWM cannot reduce switching lossthan SPWM. Moreover, it will worsen the device heat transferbecause the temperature variation. A double 120 flattop modulationmethod has been proposed in [6] and [7] to reduce theperiod of PWM switching to only 1/3 of the whole fundamentalperiod. However, these papers didn't compare the spectrumof this method with others, which is not fair. In addition, themethod is only specified to a fixed topology, which cannot beapplied widely.

This paper proposes a novel generalized space vector Pulsewidth amplitude modulation (SVPWAM) method for thebuck/boost voltage source inverter (VSI) and current source inverter(CSI). By eliminating the conventional zero vectors inthe space vector modulation, two-third and one-third switchingfrequency reduction can be achieved in VSI and CSI, respectively.If a unity power factor is assumed, an 87% switchingloss reduction can be implemented in VSI, and a 74% reductioncan be implemented in CSI. A 1-kW boost-converter invertersystem has been developed and tested based on the SVPWAMmethod. A 90% power loss reduction compared to SPWM hasbeen observed. The two stage efficiency reaches 96.7% at thefull power rating. The power volume density of the prototype is2.3 kW/L. The total weight of the system is 1.51 lb. Therefore, a High-efficiency, high-power density, high-temperature, and lowcost1-kW inverter is achieved by using an SVPWAM method.

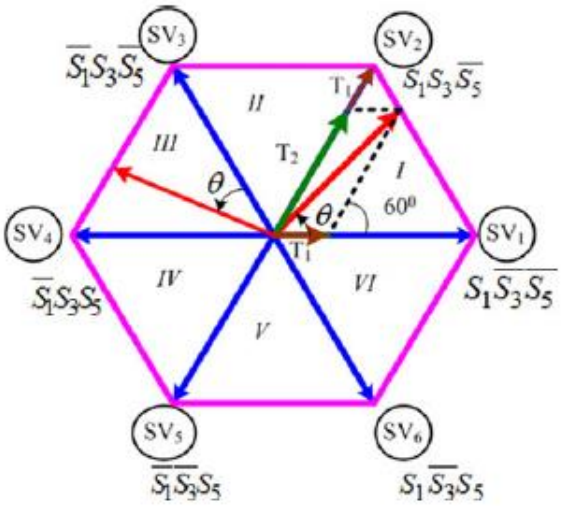

Fig.2. SVPWAM for VSI.

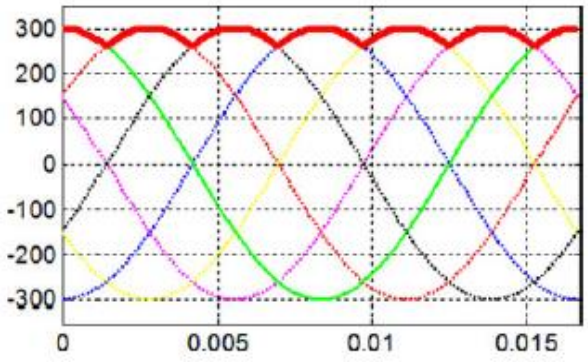

Fig.3. DC-link voltage of SVPWAM in VSI.

2. SVPWAM for VSI

A. Principle of SVPWAM Control in VSI

The principle of an SVPWAM control is to eliminate the zero vectors in each sector. The modulation principle of SVPWAM is shown in Fig.2. In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the adjacent two sectors. For example, in sector VI and I, phase leg A has no switching at all. The dc-link voltage thus is directly generated from the output line-to-line voltage. In sector I, no zero vector is selected. Therefore, S1 and S2 keep constant ON, and S3 and S6 are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-

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line voltage Vac at this time. Consequently, the dc-link voltage should present a 6ω varied feature to maintain a desired output voltage. A dc–dc conversion is needed in the front stage to where θ ∈[0, π/3] is relative angle from the output voltage vector to the first adjacent basic voltage vector like in Fig. 2. If the time period for each vector maintains the same, the switching frequency will vary with angle, which results in a variable inductor current ripple and multi frequency output harmonics.

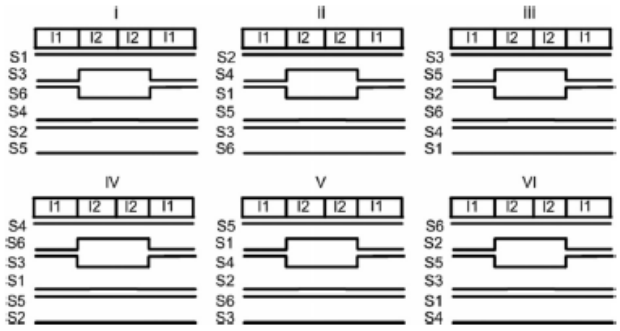

Fig.4.Vector placement in each sector for VSI.

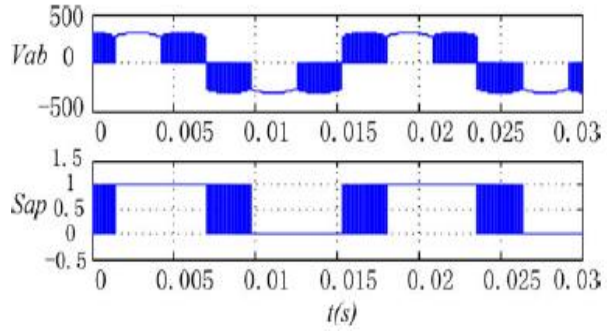

Fig.5. Theoretic waveforms of dc-link voltage, output line-to-line voltageand switching signals.

Where θ ∈ [0, π/3] is relative angle from the output voltagevector to the first adjacent basic voltage vector like in Fig. 2. Ifthe time period for each vector maintains the same, the switchingfrequency will vary with angle, which results in a variableinductor current ripple and mutifrequency output harmonics.Therefore, in order to keep the switching period constant butstill keep the same pulsewidth as the original one, the new timeperiods can be calculated as

$$T_1'/T_s = T_1/(T_1+T_2) \qquad (2)$$

The vector placement within one switching cycle in eachsector is shown in Fig. 4. Fig. 5 shows the output line-to-linevoltage and the switching signals of S1.

B. Inverter Switching Loss Reduction for VSI

For unity power factor case, the inverter switching loss isreduced by 86% because the voltage phase for PWM switchingis within [−60◦, 60◦], at which the current is in the zero-crossingregion.

In VSI, the device voltage stress is equal to dc-link voltageVDC, and the current stress is equal to output current ia. Thusthe switching loss for each switch is

$$P_{SW\_I} = \frac{1}{2\pi}\left[\int_{-\pi/6}^{\pi/6} E_{SR}\frac{|I_m\sin(\omega t)|\cdot V_{DC}}{V_{ref}I_{ref}}\cdot f_{sw}\,d\omega t + \int_{5\pi/6}^{7\pi/6} E_{SR}\frac{|I_m\sin(\omega t)|\cdot V_{DC}}{V_{ref}I_{ref}}\cdot f_{sw}\,d\omega t\right] = \frac{2-\sqrt{3}}{\pi}\cdot\frac{I_m V_{DC}}{V_{ref}I_{ref}}E_{SR}\cdot f_{sw}, \qquad (3)$$

WhereESR, Vref , Iref are the references.

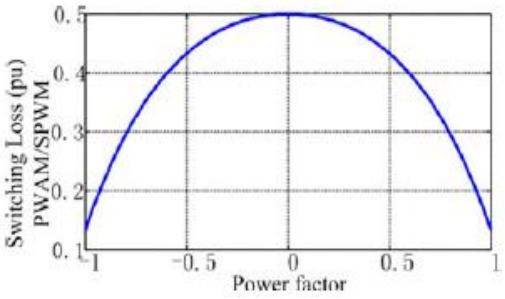

Fig.6.(SVPWAMpower loss/SPWM power loss) versus power factor in VSI.

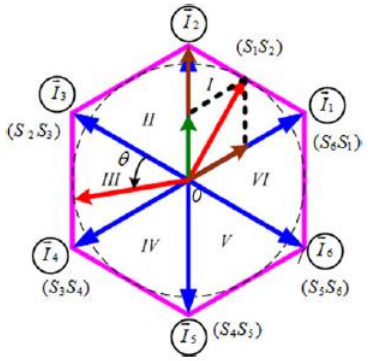

Fig.7.Conventional CSI and its corresponding SVPWAM diagram.

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Since the SVPWAM only has PWM switching in two 60◦sections, the integration over 2π can be narrowed down intointegration within two 60◦

$$P_{SW\_I} = (2\sqrt{3})/\pi \cdot (I_m V_{DC}/(V_{ref} I_{ref})) \cdot E_{SR} \cdot f_{sw}. \quad (4)$$

The switching loss for a conventional SPWM method is

$$P_{SW\_I'} = (2/\pi) \cdot (I_m V_{DC}/(V_{ref} I_{ref})) \cdot E_{SR} \cdot f_{sw}. \quad (5)$$

In result, the switching loss of SVPWAM over SPWM isf = 13.4%.

However, when the power factor decreases, the switchingloss reduction amount decreases because the switching current increase as Fig.6 shows.

As indicated, the worst case happens when power factor isequal to zero, where the switching loss reduction still reaches50%. In conclusion, SVPWAM can bring the switching lossdown by 50–87%.

III. SVPWAM FOR CSI

A. Principle of SVPWAM in CSI

The principle of SVPWAMin CSI is also to eliminate the zerovectors. As shown in Fig. 7, for each sector, only two switchesare doingPWMswitching, since only one switch in upper phaselegs and one switch in lower phase legs are conducting togetherat any moment. Thus, for each switch, it only needs to do PWM

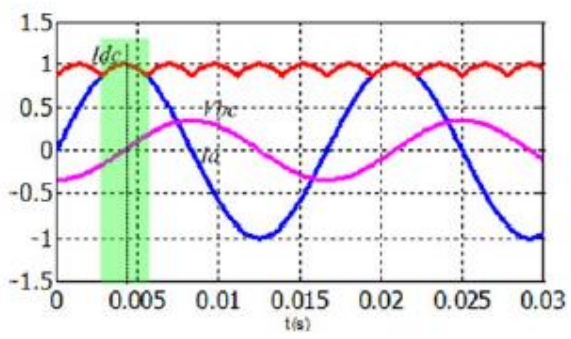

Fig.8. Switching voltage and current when pf = 1.

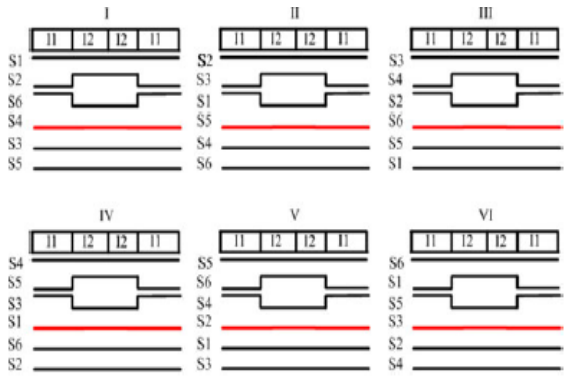

Fig.9. Vector placement for each sector for CSI.

Switching in two sectors, which is one-third of the switching period. Compared to SVPWM with single zero vector selectedin each sector, this method brings down the switching frequencyby one-third.

Similarly, the dc-link current in this case is a 6ω variedcurrent. It is the maximum envelope of six output currents:

Ia, Ib, Ic, −Ia, −Ib, −Ic, as shown in Fig. 8. For example, insector I, S1 always keeps ON, so the dc-link current is equal toIa . The difference between dc-link current in CSI and dc-linkvoltage in VSI is dc-link current in CSI is overlapped with thephase current, but dc-link voltage in VSI is overlapped with theline voltage, not the phase voltage

The time intervals for two adjacent vectors can be calculatedin the same way as (1) and (2). According to diagram in Fig. 7,the vector placement in each switching cycle for six switchescan be plotted in Fig. 9.

The SVPWAM is implemented on conventional CSI throughsimulation. Fig. 10 shows the ideal waveforms of the dc currentIdc, the output phase ac current and the switching signals ofS1. The switching signal has two sections of PWM in positivecycle, but no PWM in negative cycle at all.

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B. Inverter Switching Loss Reduction for CSI

In CSI, the current stress on the switch is equal to the dclinkcurrent, and the voltage stress is equal to output line-to-linevoltage, as shown the shadow area in Fig. 8 Thus, the switchingloss for a single switch is determined by

$$P_{SW\_CSI} = \frac{2-\sqrt{3}}{\pi}\frac{\overline{i_{dc}}\cdot V_{l-lpeak}}{V_{ref} I_{ref}} E_{SR} f_{sw}. \qquad (6)$$

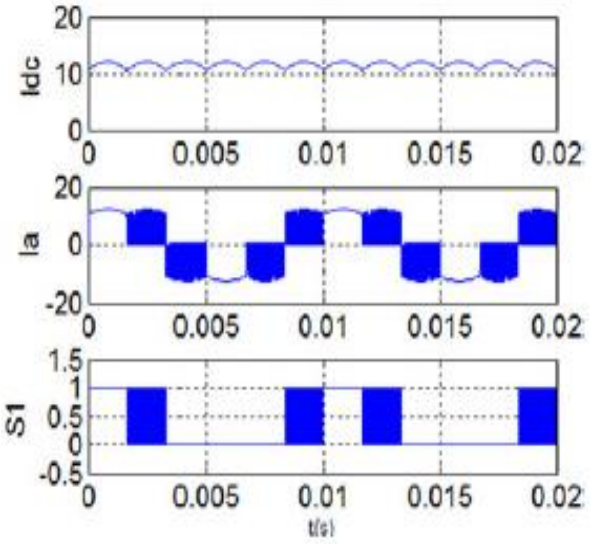

Fig.10. Theoretic waveforms of dc-link current, output line current andswitching signals.

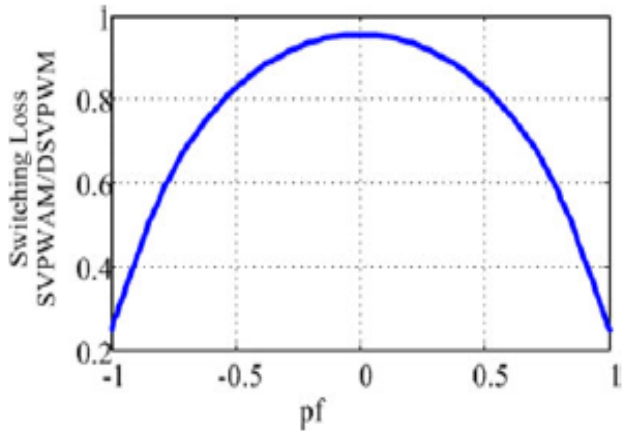

Fig.11.CSI switching loss ratio between SVPWAM and discontinuousSVPWM versus power factor.

When compared to discontinuousSVPWM,if the half switchingfrequency is utilized, then the switching loss of it becomeshalf of the result in (6). The corresponding switching loss ratiobetween SVPWAM and discontinuous SVPWM is shown inFig. 11.

IV. SPECTRUM ANALYSIS OF SVPWAM

A fair comparison in switching loss should be based on anequal output harmonics level. Thus, the switching loss may notbe reduced if the switching frequency needs to be increased inorder to compensate the harmonics. For example, discontinuousSVPWM has to have double switching frequency to achieve thesame THD as continuous PWM. So the switching loss reductionis much smaller than 50%. Therefore, for the newly proposed SVPWAM, a spectrum analysis is conducted to be comparedwith other methods on the basis of an equal average switchingfrequency, which has not been considered in paper [16].

A. Spectrum Comparison Between SVPWAM,

SPWM, and SVPWMThe object of spectrum analysis is the output voltage or currentbefore the filter. The reason is that certain orders of harmonicscan be eliminated by sum of switching functions inVSI or subtraction of switching functions in CSI. The comparisonis between SVPWAM, DPWM, and continuous SVPWMin VSI/CSI. The switching frequency selected for each methodis different, because the comparison is built on an equalized

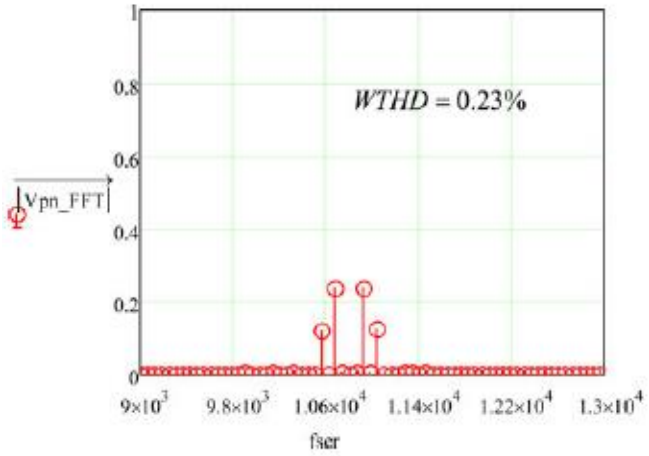

Fig.12. Spectrum of SPWM at switching frequency.

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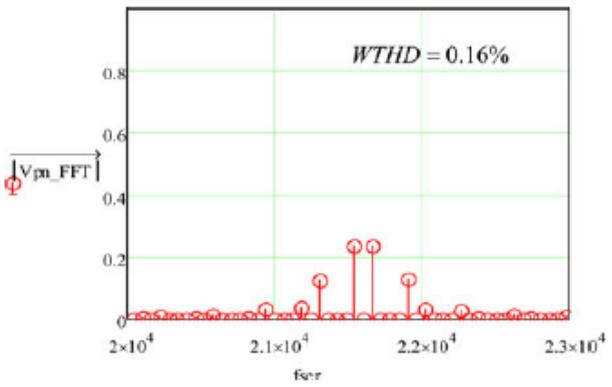

Fig.13. Spectrum of discontinuous SVPWM at switching frequency.

average switching frequency over a whole fundamental cycle,in order to make the harmonics comparable at both lowmodulation and high modulation range. Assume that the basefrequency is f0 = 10.8 kHz. Thus, 3f0 should be selected forSVPWAM, and f0 should be selected for continuousSVPWMinVSI. In CSI, 3f0, 2f0 , and f0 should be selected for SVPWAM,discontinuous SVPWM, and continuous SVPWM, respectively.

The modulation index selected here is the maximum modulationindex 1.15, since the SVPWAM always only has themaximum modulation index. Theoretically, theTHD varies withmodulation index. The dc-link voltage is designed to be a constantfor SVPWM and an ideal 6ω envelope of the output sixline-to-line voltages for SVPWAM. Thus, the harmonic of theSVPWAM here does not contain the harmonics from the dc–dcconverter output. It is direct comparison between two modulationmethods from mathematics point of view.

Figs. 12–14 show the calculated spectrum magnitude at firstside band of switching frequency range for three methods. It canbe concluded that the ideal switching function of SVPWAM hasless or comparable harmonics with SPWM and DPWM.

V. TOPOLOGIES FOR SVPWAM

Basically, the topologies that can utilize SVPWAM have twostages: dc–dc conversion which converts a dc voltage or currentinto a 6ω varied dc-link voltage or current; VSI or CSI for whichSVPWAM is applied. One typical example of this structure isthe boost converter inverter discussed previously. However, thesame function can also be implemented in a single stage, suchas Z/quasi-Z/trans-Z source inverter [37]–[40].

The front stage can also be integrated with inverter to forma single stage. Take current-fed quasi-Z-source inverter as an

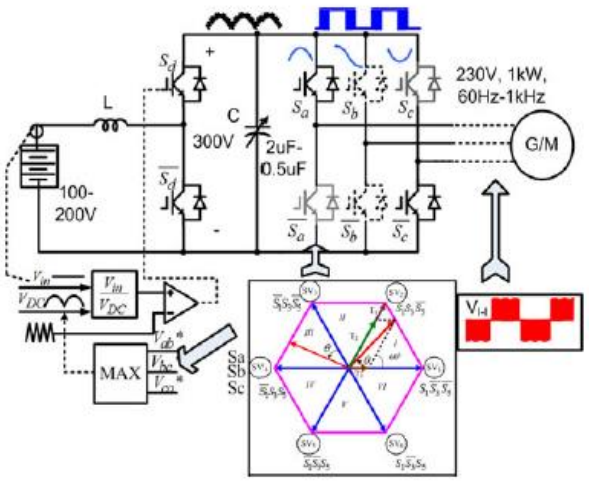

Fig.15. SVPWAM-based boost-converter-inverter motor drive system.

Example. Instead of controlling the dc-link current Ipn to havea constant average value, the open zero state duty cycle Dopwill be regulated instantaneously to control Ipm to have a 6ωfluctuate average value, resulting in a pulse type 6ω waveform
at the real dc-link current Ipn, since I1 is related to the input dccurrent Iin by a transfer function

$$I_1 = \frac{1 - D_{op}}{1 - 2D_{op}} I_{in} \qquad (9)$$

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VI. CASE STUDY: 1-KWBOOST-CONVERTER INVERTERFOR EV MOTOR DRIVE APPLICATION

A. Basic Control Principle

The circuit schematic and control system for a 1-kW boostconverterinverter motor drive system is shown in Fig. 15. A6ω dc-link voltage is generated from a constant dc voltage bya boost converter, using open-loop control. Inverter then couldbe modulated by a SVPWAM method. The specifications forthe system are input voltage is 100–200 V; the average dc-linkvoltage is 300 V; output line-to-line voltage rms is 230 V; andfrequency is from 60 Hz to 1 kHz.

B. Voltage Constraint and Operation Region

It is worth noting that the SVPWAM technique can onlybe applied when the batteries voltage falls into the regionVin ≤√√32 Vl−l due to the step-up nature of boost converter.The constraint is determined by the minimum point of the 6ωdc-link voltage. Beyond this region, conventional SPWM canbe implemented. However, the dc-link voltage in this case stillvaries with 6ω because of the small film capacitor we selected.Thus, a modified SPWM with varying dc-link voltage will beadopted during the motor start up as shown in Fig. 16. Hence,the system will achieve optimum efficiency when the motor isoperating a little below or around nominal voltage. When themotor demands a low voltage during start up, efficiency is thesame as the conventional SPWM-controlled inverter.

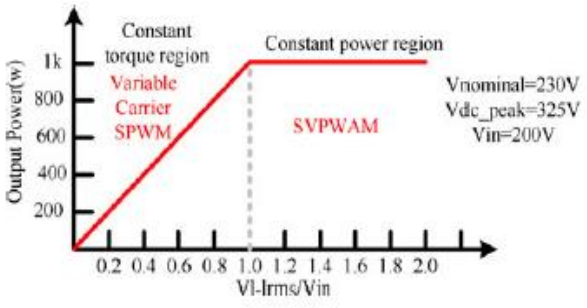

Fig.16. Operation region of boost-converter-inverter EV traction drive.

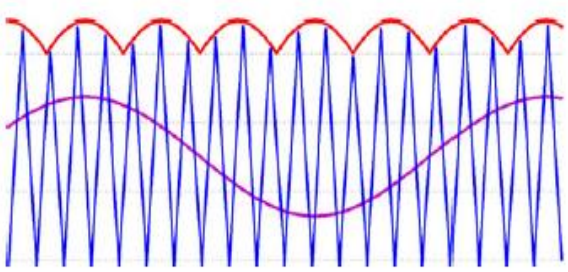

Fig.17.Variable carrier SPWM control in buck mode.

In SVPWAM control of boost mode, dc-link voltage varieswith the output voltage, in which the modulation index is alwayskept maximum. So, when dc-link voltage is above the batteryvoltage, dc-link voltage level varies with the output voltage. Thevoltage utilization increased and the total power stress on thedevices has been reduced.

C. Variable DC-Link SPWM Control at High Frequency

When the output needs to operate at a relative high frequency,like between 120 Hz and 1 kHz, it is challenging to obtain a 6ωdc-link voltage without increasing the switching frequency ofa boost converter. Because the controller does not have enoughbandwidth.

Furthermore, increasing boost converter switching frequencywould cause a substantial increase of the total switching loss,because it takes up more than 75% of the total switching loss.The reason is because it switches at a complete current region.Also a normal SPWM cannot be used in this range because thecapacitor is designed to be small that it cannot hold a constantdc link voltage. Therefore, the optimum option is to controlthe dc link voltage to be 6ω and do a variable dc link SPWMmodulation, as explained in Fig. 17.

In this variable dc-link SPWM control, in order to get better utilization of the dc-link voltage, an integer times betweenthe dc-link fundamental frequency and output frequency is preferred.When the output frequency is in [60 Hz, 120 Hz], a 6ωdc link is chosen; when the frequency is in [120 Hz, 240 Hz], a

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3ω dc link is chosen; when the frequency is in [240 Hz, 360 Hz],a 2ω dc link is chosen.

D. Experiment Results

1) Experiment Setup: A 1-kW boost-converter inverter prototypehas been built in the laboratory to implement theSVPWAM control at 60 Hz and SPWM control at 1 kHz, in

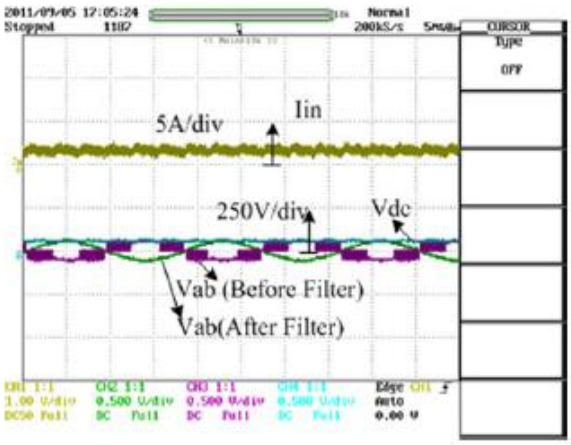


Fig.19. Output voltage and input current at Vin = 20 V, Vdc avg = 60 V,Vlrms = 46 V, Po = 40 W, fo = 60 Hz, fsw = 20 kHz.

order to demonstrate their merits in reducing power loss and reducingthe size compared to traditional methods. The picture ofthe hardware is shown in Fig. 18. It includes a DSP board, a gatedrive board, a boost converter, a three-phase inverter, heat sink,and a fan cooling system. The dimension is 11 cm × 8 cm ×5 cm, and the total weight is 1.5 lb.

The parameters used in the test are rated power: 1 kW; batteryvoltage: 100–200 V; rated line voltage rms: 230 V; dc-linkvoltage peak: 324 V; switching frequency: 20 kHz; output frequency:60 Hz–1 kHz

2) SVPWAM Control at 60 Hz: Figs. 19–20 show the outputand input voltage, current waveform when input voltageincreases from 20 to 100 V, while keeping the boost ratio constant.In this case, the output voltage increases linearly with inputvoltage increase. The output power increases in proportion to square of the input voltage.

Fig. 21 shows the efficiency test results by YOKOGAWAWT1600 series power meter when the input voltage increasesfrom 100 to 200 V, while keeping the output power constantat 1 kW. The output line-to-line voltage rms keeps at 230 V,and the dc-link voltage is a 6ω varied waveform with 325 Vpeak value. In the data record on the power meter, Umn6, Umn4,and Umn1 represent the phase line voltages; Irms6, Irms4, andIrms1 represent ten times of phase currents, because ten circlesof wires have been wound on the current transducer core of

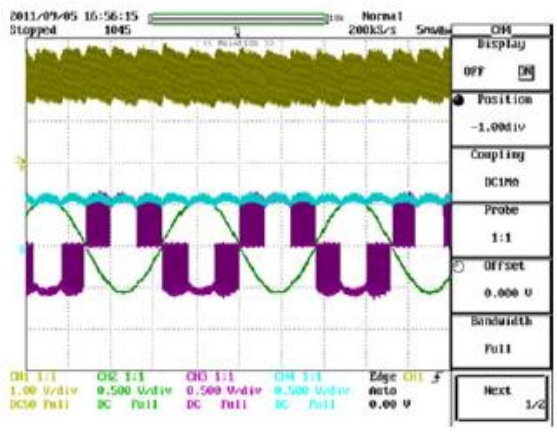
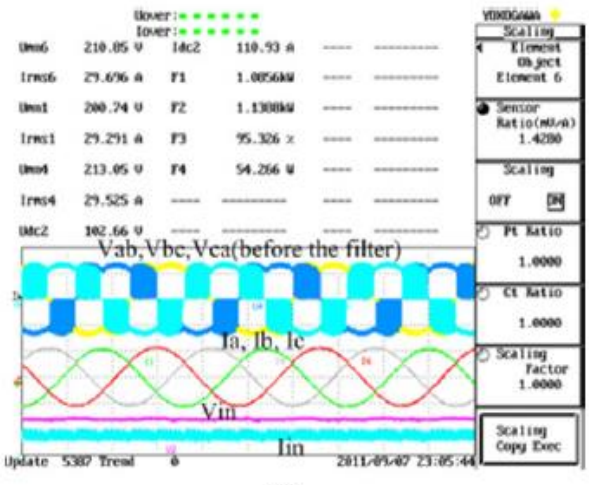


Fig.20. Output voltage and input current at Vin = 100 V, Vdc avg = 300 V,Vlrms = 230 V, Po = 1 kW, fo = 60 Hz, fsw = 20 kHz.



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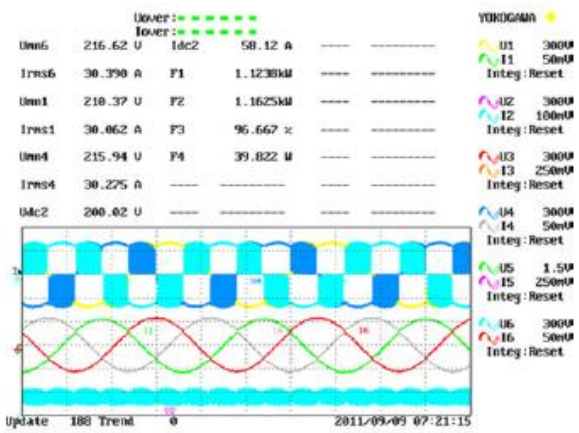
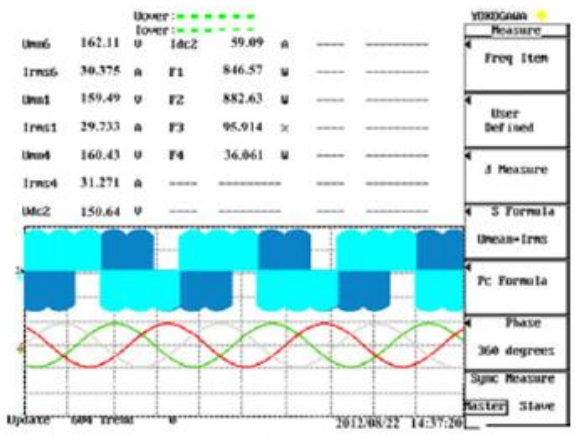


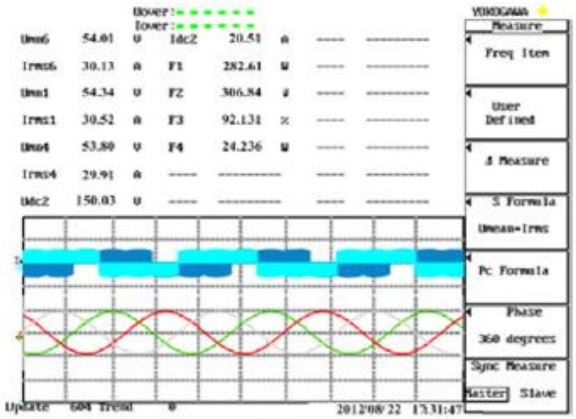
(b)

Fig. 21. Results of efficiency test at constant full power rating 1 kW butdifferent input voltage by YOKOGAWA WT1600 series power meter.

Waveformsfrom the top to bottom: output line-to-line voltage before LC filter, outputcurrent, input voltage, input current. The numbers displayed on the screen represent:Umn6, Umn1, Umn4 : RMS value of output line-to-line voltage before LCfilter, like the first waveform shows; Irms6 , Irms1 , Irms4 : ten times of outputline current; Udc2 : input voltage; Idc2 : 10 times of input current; F1: outputpower; F2: input power; F3: efficiency calculated from F1/F2; F4: total powerloss: (a) Vin = 150 V, Vdc avg = 300 V, Vlrms = 230 V, Po = 1 kW, fo =60 Hz, fsw = 20 kHz; (b) Vin = 200 V, Vdc avg = 300 V, Vlrms = 230 V, Po= 1 kW, fo = 60 Hz, fsw = 20 kHz.



(a)



(b)

Fig. 22. Results of efficiency test at constant torque region by YOKOGAWAWT1600 series power meter.

Waveforms from the top to bottom: output lineto-line voltage before LC filter, output current. The input voltage keeps at200 V constant; the dc-link voltage keeps at 300 V 6ω voltage; the outputvoltage changes from 54 to 162 V, thus the power also changes from 280 to850 W proportionally. When power is equal to 1 kW, the voltage reaches at Nominal value 230 V. (a) Vin = 200 V, Vdc avg = 300 V, Vlrms = 162 V,Po = 850 W, fo = 60 Hz. (b) Vin = 200 V, Vdc avg = 300 V, Vlrms = 54 V,Po = 280 W, fo = 60 Hz.

The power meter. Udc2 is input dc voltage and Idc2 is ten timesof average input dc current. F1 and F2 are the measured outputand input power, respectively. F3 is the efficiency that iscalculated using F1/F2. F4 is the overall power loss. Fig. 22shows the efficiency test results when the power increases inproportional to output voltage below the maximum power whilekeeping the input voltage and dc-link voltage constant, which iscorresponding to the constant torque region in Fig. 16. The inputvoltage keeps at 300 V 6ω voltages; the output voltage changesfrom 54 to 162 V; thus, the power also changes from 280o 850 W proportionally. When power is equal to 1 kW, the voltagereaches at nominal value 230 V; this waveform is shown inFig. 21(b).

3) Output Three-Phase Voltage at 1 kHz: When the output

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Frequency increases to 1 kHz, the measured voltage and currentwaveforms and efficiency are shown in Fig. 23 at input voltage

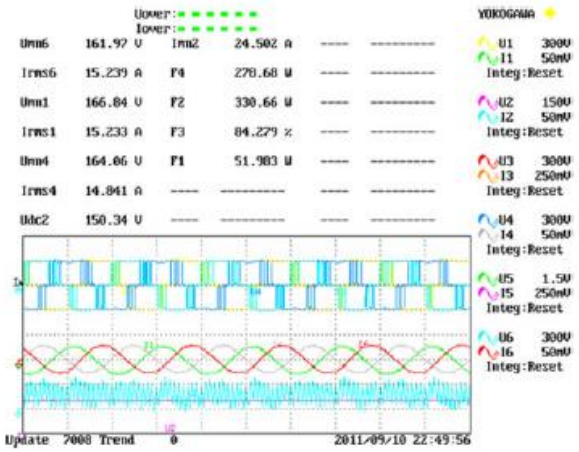
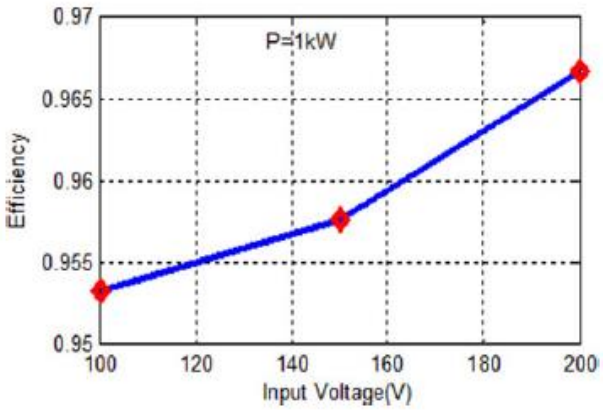
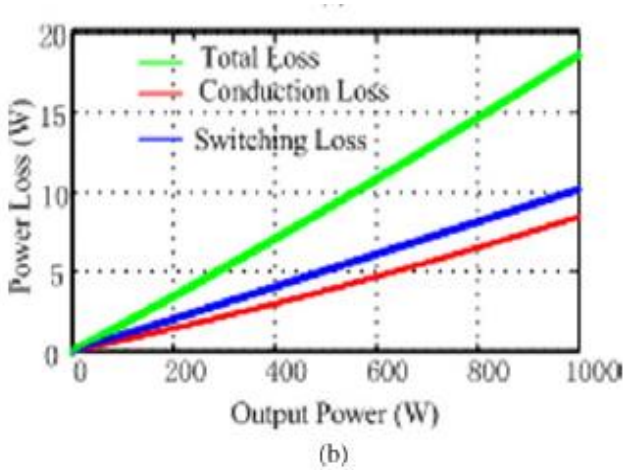


Fig.23. the efficiency test at Vin = 150 V at fo = 1 kHz: from top to bottom:output line voltage, output current, and input current.





(b)

Fig. 26. Comparison between inverter power losses in the condition that dclinkvoltage changes from 0 to full rating at 300 V: (a) SVPWAM, (b) SPWM.

Increases from 0 to full rating under two methods. Since theresearch target is only inverter, the test condition is based onvarying the output power by changing output voltage from 0to 230 V. It is observed that in the SVPWAM method, conductionloss accounts for 80% of the total power loss, but in theSPWM method, switching loss is higher than conduction loss.The switching loss is reduced from 10 to 1.4 W from SPWMto SVPWAM. An estimated 87% switching loss reduction hasbeen achieved.

VII. CONCLUSION

The SVPWAM control method preserves the following advantagescompared to traditional SPWM and SVPWM method.

1) The switching power loss is reduced by 90% comparedwith the conventional SPWM inverter system.

2) The power density is increased by a factor of 2 becauseof reduced dc capacitor (from 40 to 6 μF) and small heatsink is needed.

3) The cost is reduced by 30% because of reduced passives,heat sink, and semiconductor stress.

A high-efficiency, high-power density, high-temperature, and0 low-cost 1-kW inverter engine drive system has been developedand tested. The effectiveness of the proposed method in reductionof power losses has been validated by the experimental Results that were obtained from the laboratory scale prototype.

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