ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A Proposed RAISIN for BISR for RAM's with 2D Redundancy

Vadlamani Sai Shivoni
MTech Student
Department of ECE
Malla Reddy College of Engineering and Technology

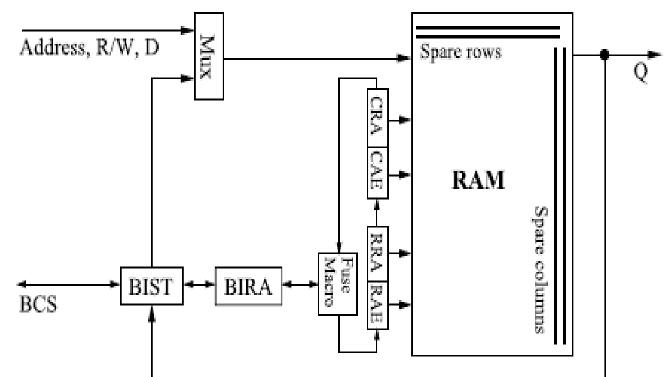
Anitha Patibandla, MTech (PhD)
Associate Professor
Department of ECE
Malla Reddy College of Engineering and Technology

Abstract - ***The proposed word oriented memory test methodology for Built-In Self-Repair (BISR) Scheme with 2D Redundancy for High Repair Efficiency (HRE). This allows to use RAMS, e.g. from memory generators, without spare rows and spare columns as used in classic redundancy concepts. The BISR simply adds faulty words to the redundancy as long as spare words are left. This avoids unnecessary external or internal redundancy calculation. The redundancy calculation will not increase the test time of the memory BIST. In addition, it is possible to add new faulty addresses to faults that have already been detected during former runs. The presented memory test allows a memory BlSR even if parts of the redundancy is already configured. The fuse box can be connected to a scan register to stream in and out data during test and redundancy configuration. A built-in redundancy analyzer (BIRA) for allocating the redundancy.***

Key Words: ***Built-In Self-Repair, BIST, 2-D redundancy, BIRA,HRE.***

1. Introduction

With the advance of VLSI technology, the capacity and density of memories is rapidly growing. The yield improvement and testing issues have become the most critical challenges for memory manufacturing. Conventionally, redundancies are applied so that the faulty cells can be repairable. Redundancy analysis using external memory testers is becoming inefficient as the chip density continues to grow, especially for the system chip with large embedded memories. A BISR scheme for RAMs with 2-D redundancy, i.e., spare rows and spare columns/IOs, typically consists of a built-in self-test (BIST) circuit, a built-in redundancy analyzer (BIRA),and a reconfiguration mechanism. The BIST is used to detect and locate faulty cells of the RAM under test. The reconfiguration mechanism is used to swap the defective element with the spare element. The BIRA is used for optimizing the allocation of the 2-D redundancy. The BIRA can collect fault information during the test process and allocate the available redundancies on the fly. Therefore, the BIRA has a heavy impact on the repair efficiency of the BISR scheme. The complexity of the redundancy allocation for RAM with 2-D redundancy is an non-deterministic polynomial-time-hard problem .However, the number of redundancies of a RAM typically is small. Thus, it is still feasible to allocate redundancies using an exhaustive search algorithm.



Typical BISR scheme for a repairable RAM [16].

2. BIST (Built in Self Test)

The BIST generates test patterns for the RAM. When a fault in the RAM is detected, the information of the fault is sent to the BIRA. The BIRA first checks if the fault has been stored in the bitmap or repaired. If not, the fault is stored in the bitmap. Then, the BIRA checks if the bitmap is full or not. A bitmap is called full if either its CAR or RAR has no space for storing a fault. If yes, the BIRA allocates the redundancies according to the stored

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

fault information and the implemented RA algorithm. If the test process is completed, the BIRA checks if the bitmap is empty or not. A bitmap is called empty if no fault information of faulty cells is stored in the bitmap. If not, the BIRA performs the redundancy allocation process to repair the remained faults. Once the BIRA process is completed and the RAM is repairable, the repaired addresses are stored in the fuse macro.

BIST is basically same as off-line testing using ATE where the test pattern generator and the test response analyzer are on-chip circuitry (instead of equipments). As equipments are replaced by circuitry, so it is obvious that compressed implementations of test pattern generator and response analyzer are to be designed. The basic architecture of BIST is shown in Figure 1.

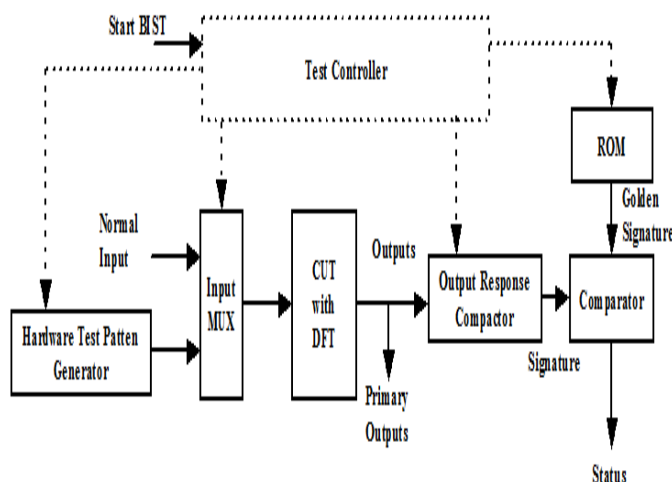


Figure 1. Basic architecture of BIST

BIST circuitry comprises the following modules (and the following functionalities)

2.1 Hardware Test Pattern Generator: This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs (of the CUT). As the test pattern generator is a circuit (not equipment) its area is limited. So storing and then generating test patterns obtained by ATPG algorithms on the CUT (discussed in Module XI) using the hardware test pattern generator is not feasible. In other words, the test pattern generator cannot be a memory where all test patters obtained by running ATPG algorithms (or random pattern generation algorithms) on the CUT are stored and applied during execution of the BIST. Instead, the test pattern generator is basically a type of register which generates random patterns which act as test patterns. The main emphasis of the register design is to have low area yet generate as many different patterns (from 0 to 2^n , if there are n flip-flops in the register) as possible.

2.2 Input Mux: This multiplexer is to allow normal inputs to the circuit when it is operational and test inputs from the pattern generator when BIST is executed. The control input of the multiplexer is fed by a central test controller.

2.3 Output response compactor: Output response compacter performs lossy compression of the outputs of the CUT. As in the case of off-line testing, in BIST the output of the CUT is to be compared with the expected response (called golden signature); if CUT output does not match the expected response, fault is detected. Similar to the situation for test pattern generator, expected output responses cannot be stored explicitly in a memory and compared with the responses of the CUT.

So CUT response needs to be compacted such that comparisons with expected responses (golden signatures) become simpler in terms of area of the memory that stores the golden signatures.

2.4 ROM: Stores golden signature that needs to be compared with the compacted CUT response.

2.5 Comparator: Hardware to compare compacted CUT response and golden signature (from ROM).

2.6 Test Controller: Circuit to control the BIST. Whenever an IC is powered up (signal start BIST is made active) the test controller starts the BIST procedure. Once the test is over, the status line is made high if fault is found. Following that, the controller

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

connects normal inputs to the CUT via the multiplexer, thus making it ready for operation.

3 MBISR (Memory Built in Self Repair)

The memory BISR(MBISR) concept contains an interface between memory BIST(MBIST) logic and redundancy wrapper for storing faulty addresses. This allows using already existing MBIST solutions. The MBIST controller output must provide three signals to the wrapper logic during test.

- A fail signal to store data in the fuse register.
- The expected data that is compared to the results of RAM data.
- The failing address.

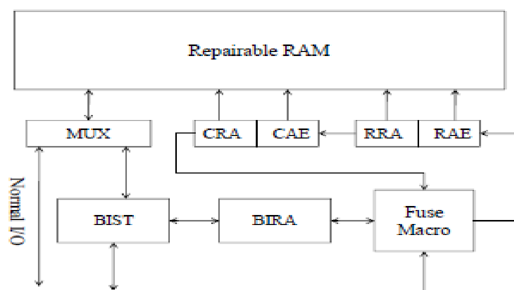


Figure 2. MBISR scheme for embedded rams

4 . Repairable RAM

A RAM with redundancies and reconfiguration circuit is called as a repairable RAM. Figure 7.2 depicts an example of an 8*8 bit-oriented RAM with 1 spare row and 1 spare column. If a spare row is allocated to replace a defective row, then the row address of the defective row is called row repair address (RRA).

Then a decoder decodes the RRA into control signals for switching row multiplexers to skip the defective row if the row address enable (RAE) signal is asserted. The reconfiguration of the defective column and the spare column is performed in a similar way, i.e., give a column repair addresses (CRA) and assert the column address enable signal to repair the defective column using the spare column.

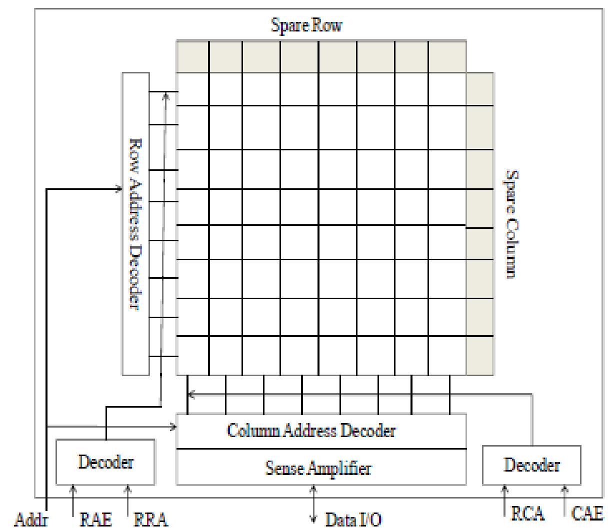
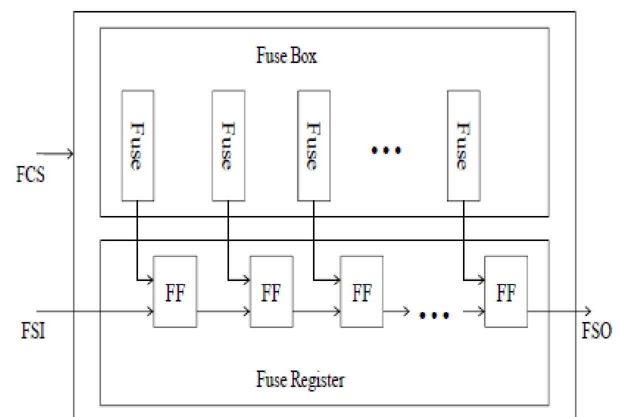


Figure 3. conceptual diagram of an 8*8 bit oriented repairable ram

5. Fuse Macro

It stores repair signatures of RAMs under test. Figure 4. shows the conceptual block diagram of a typical implementation of fuse macro. The fuses of the fuse box can be implemented in different technologies, e.g., laser blown fuses, electronic-programmable fuses, etc. The fuse register is the transportation interface between the fuse box and the repair register in the repairable RAM.



FCS: Fuse Control Signals;

FSI: Fuse Scan In ;

FSO: Fuse Scan Out

Figure 4. conceptual block diagram of fuse macro

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

6. Architecture of HRE-BISR Scheme

The BIRA of a BISR circuit for a RAM with 2-D redundancy typically has a bitmap for storing fault information during the process of redundancy allocation. The bitmap is a cache-like element which has the parallel comparison and storing functions. Since the bitmap is only used in test mode for RA, we can modify it into a spare memory in normal mode. Fig. 5 shows the block diagram of the proposed HRE-BISR scheme for RAMs by reusing then bitmap as a spare memory. Here, we assume that the RAM has 2-D redundancy, e.g., spare rows and columns, and the reconfiguration of redundancies is done by shift redundancy technique [33]. The BIRA consists of a multiple-fault-bit detector (MFBD), a finite state machine (FSM), a repaired fault checker (RFC), a repair signature register (RSR), and a modified bitmap. The FSM realizes the RA algorithm. The MFBD is used to check if the number of faulty bits of a detected faulty word are larger than 2. The RSR is used to store the repaired addresses during the process of RA. Once the BIST detects a fault, the RFC checks if the detected fault has been stored in the RSR. If yes, the detected fault has been repaired. The modified bitmap is used to collect fault information in test mode and serves as spare bits in normal mode.

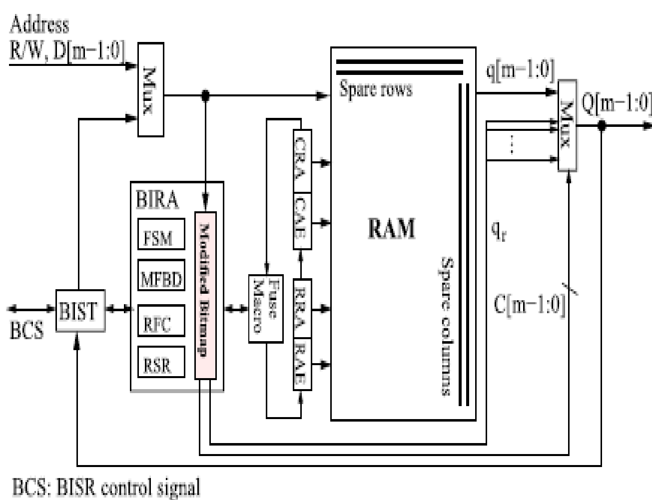


Figure 5. Block diagram of HRE-BISR

7. Simulation Results

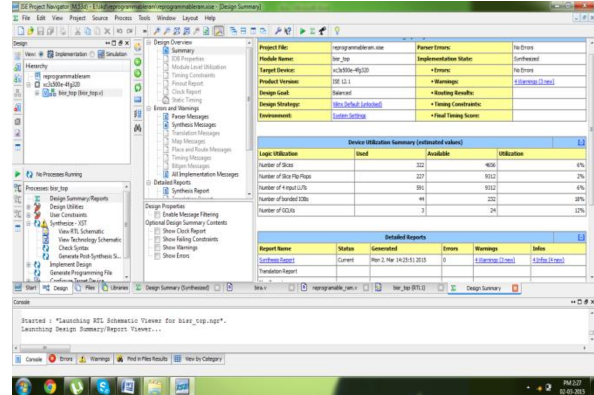


Figure 6. AREA CALCULATION

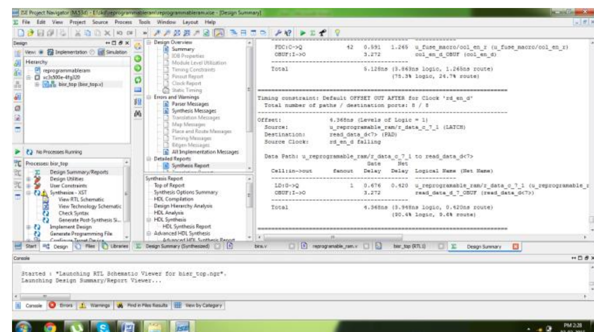


Figure 7. DELAY CALCULATION

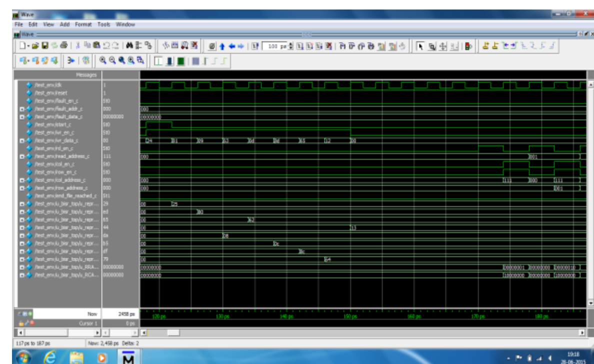


Figure 8. Waveforms

8. Conclusion and Future Scope

In this paper, we have proposed a HRE-BISR scheme for RAMs with 2-D redundancy. By reusing the bitmap for the RA to serve spare bits in normal mode, the HRE-BISR scheme can enhance the RR. To support the redundancy allocation of RAMs with 2-D and spare-bit redundancies, a RCB-RA algorithm has also been proposed. Simulation results show that the HRE-BISR scheme only incurs about 0.08-ns delay penalty for a

512 × 16 × 32-bit RAM using 3 × 3-bit bitmap for RA. In addition, the RCB-RA algorithm can provide 0.48%–11.95% increment of RR for different fault distributions. Furthermore, only about 0.44% additional hardware overhead is needed to modify the bitmap as spare-bit redundancy.

Future Scope:

In this paper we are using LFSR for generating random patterns instead we can use LT-LFSR or MSIC.

9. References

[1] M. Lin, Ed., "1997 Semiconductor Industry Annual Report," (in Chinese), Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, ITIS project report, 1997.

[2] I. Voyiatzis, A. Paschalis, D. Gizopoulos, N. Kranitis, and C. Halatsis, "A concurrent BIST architecture based on a selftesting RAM," *IEEE Trans. Rel.*, vol. 54, no. 1, pp. 69–78, Mar. 2005.

[3] A.Vishnupriya & Mr.J.Madan Kumar, An Efficient Architecture for BISR (Built-In Self-Repair) Using Extended Essential Spare Pivoting (EESP) Algorithm, http://www.ijmetmr.com/olapril2015/Vishnupriya-JMadanKumar-46.pdf, Volume No: 2, Issue No: 4

[4] K. K. Saluja, R. Sharma, and C. R. Kime, "A concurrent testing technique for digital circuits," *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, vol. 7, no. 12, pp. 1250–1260, Dec. 1988.

[5] R. Sharma and K. K. Saluja, "Theory, analysis and implementation of an on-line BIST technique," *VLSI Design*, vol. 1, no. 1, pp. 9–22, 1993.

[6] K. K. Saluja, R. Sharma, and C. R. Kime, "Concurrent comparative built-in testing of digital circuits," Dept. Electr. Comput. Eng., Univ. Wisconsin, Madison, WI, USA, Tech. Rep. ECE-8711, 1986.

[7] I. Voyiatzis, T. Haniotakis, C. Efstathiou, and H. Antonopoulou, "A concurrent BIST architecture based on monitoring square windows," in *Proc. 5th Int. Conf. DTIS*, Mar. 2010, pp. 1–6.

[8] M. A. Kochte, C. Zoellin, and H.-J. Wunderlich, "Concurrent self-test with partially specified patterns for low test latency and overhead," in *Proc. 14th Eur. Test Symp.*, May 2009, pp. 53–58.

[9] S. Almukhaizim and Y. Makris, "Concurrent error detection methods for asynchronous burst mode machines," *IEEE Trans. Comput.*, vol. 56, no. 6, pp. 785–798, Jun. 2007.

[10] S. Almukhaizim, P. Drineas, and Y. Makris, "Entropy-driven parity tree selection for low-cost concurrent error detection," *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, vol. 25, no. 8, pp. 1547–1554, Aug. 2006

[11] C.-T. Huang, C.-F. Wu, J.-F. Li, and C.-W. Wu, "Built-in redundancy analysis for memory yield improvement," *IEEE Trans. Rel.*, vol. 52, no. 4, pp. 386–399, Dec. 2003.

[12] J.-F. Li, J.-C. Yeh, R.-F. Huang, and C.-W. Wu, "A built-in self-repair design for RAMs with 2-D redundancies," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 742–745, Jun. 2005.

Authors:

Anitha Patibandla is an Associate Professor at Malla Reddy College of Engineering and Technology, Hyderabad. She received her Bachelor degree in Electronis and Communication Engineering from Osmania university College Of Engineering, Hyderabad, M.Tech, V.L.S.I System Design from J.N.T.U.H affiliated college. She is presently pursuing Ph.D at JNTUH. Her research interest is Low power VLSI Design.

Vadlamani Sai Shivoni has completed her B.Tech in Electronics and Communication Engineering from City Womens College of Engineering and Technology, J.N.T.U.H affiliated college in 2013.She is pursuing her M.Tech in VLSI and Embedded Systems from Malla Reddy College of Engineering and Technology , J.N.T.U.H affiliated college.