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Implementation of OFDM System Using FFT and IFFT

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Abstract:

A fast Fourier transform (FFT) is an algorithm to compute discrete Fourier transform. A Fourier transform convert's time domain signal information into frequency domain. As a result, FFT is a widely used in DSP technique and in many applications such as communication. FFT has been described as most important numerical algorithm. FFT is one of the rudimentary operations in the field of digital signal and image processing. Using FFT is indispensable in most signal processing application. In this paper we propose to use efficient multiplication technique to reduce the partial product which is happened in conventional multiplication technique therefore the FFT and inverse fast Fourier transform (IFFT) with efficient multiplication and with increased speed is used for Orthogonal Frequency Division Multiplexing (OFDM) Modulator and Demodulator blocks. In many applications high speed and efficient multiplication is desired. For this purpose conventional multicarrier technique are usually chosen, but this results in lower spectrum efficiency. So, the principles of OFDM are used. This proposed work will be processing block of an OFDM system, which are applied to FFT and IFFT. Actually, in entire architecture all the mathematical manipulation takes place in transmitter and receiver block i.e. IFFT and FFT block respectively. The speed enhancement is the key contribution of the main processing blocks in OFDM system.

I INTRODUCTION:

Orthogonal Frequency Division Multiplexing (OFDM) is a special case of multicarrier transmission, where a single data stream is transmitted over a number of lower rate subcarriers. The main reason to use OFDM is to increase the robustness against the selective fading or narrowband interference. In single carrier system if signal get fade or interfered then entire link gets failed where as in multicarrier system only a small percentage of the subcarriers will be affected. The total signal bandwidth, in a classical parallel data system, can be divided into N non-overlapping frequency sub-channels. Each sub-channel is modulated a separate symbol and then N sub-channels are frequency multiplexed. The general practice of avoiding spectral overlap of sub-channels was applied to eliminate inter-carrier OFDM is a combination of modulation and multiplexing. Multiplexing generally refers to independent signals, those produced by different sources. In OFDM the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create the OFDM carrier. OFDM is a special case of Frequency Division Multiplex (FDM). Orthogonal frequency division multiplexing (OFDM) has recently become a key modulation technique for both broadband wireless and wire-line applications.

It has been adopted for digital audio broadcasting (DAB) and digital terrestrial television broadcasting (DVB). OFDM is a special case of Multicarrier transmission, where a single data stream is transmitted over number of lower rate Subcarrier. The problem of inter symbol interference (ISI) introduced by multipath channel is significantly reduced in OFDM by using the cyclic prefix (CP) as a guard interval between OFDM blocks. The proposed work would be a brief overview of IFFT & FFT algorithm to be effectively used in OFDM system. OFDM is a special case of multicarrier transmission, where a single data stream is transmitted over a number of lower rate subcarriers. The main reason to use OFDM is to increase the robustness against the selective fading or narrowband

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interference. The OFDM transmitter and receiver contain Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT), respectively[6]. The IFFT/FFT algorithms are chosen due to their execution speed, flexibility and precision [3]. For real time systems the execution speed is the main concern. The IFFT block provides orthogonality between adjacent subcarriers. The orthogonality makes the signal frame relatively secure to the fading caused by natural multipath environment. As a result OFDM system has become very popular in modern telecommunication systems. The main objective of this paper is to design IFFT/FFT blocks for OFDM, because these are main blocks for modulation and demodulation in OFDM transmitter and receiver [2]. The OFDM signal is generated by implementing the Inverse Fast Fourier Transform (IFFT) at the transmitter which is used to convert frequency domain to time domain and Fast Fourier Transform (FFT) which is used to convert time domain to frequency domain at the receiver side is implemented.

In single carrier system if signal get fade or interfered then entire link gets failed whereas in multicarrier system only a small percentage of the subcarriers will be affected. The total signal bandwidth, in a classical parallel data system, can be divided into N nonoverlapping frequency sub-channels. Each subchannel is modulated a separate symbol and then N sub-channels are frequency multiplexed. The general practice of avoiding spectral overlap of sub-channels was applied to eliminate inter-carrier interference (ICI). This is shown in Fig. 1(A). This resulted in insufficient utilization of the existing spectrum. An idea was proposed in the mid1960's to deal with this wastefulness through the development of frequency division multiplexing (FDM) with overlapping sub-channels. The sub-channels were arranged so that the sidebands of the individual carriers overlap without causing ICI. This principle is shown in Fig 1(B). To achieve this, the carriers must be mathematically orthogonal. From this constraint the idea of OFDM was born. OFDM is a combination of modulation and multiplexing.

Multiplexing generally refers to independent signals, those produced by different sources. In OFDM the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create the OFDM carrier. OFDM is a special case of FDM

2. OFDM Basics

OFDM is a wideband wireless digital communication technique that is based on block modulation. It is known as block modulation because the OFDM frame is split into blocks and each block has Ts duration. These blocks contain one or more symbols. Each symbol or group of symbols will be assigned a separate carrier. The OFDM arranges the subcarriers in such a way that they do not overlap and maintain the orthogonality between them. These subcarriers are modulated independently. All the split information is then transmitted in parallel through multiple carriers [17]. In OFDM the carriers can be placed as near as possible maintaining the orthogonality, thereby making better utilization of the spectrum. The width of the pulse puts the limit on the sub-carrier spacing. The subcarrier spacing will be inversely proportional to the symbol duration, where symbol duration is denoted by Ts. Longer is the symbol duration, better is the performance [18].

Orthogonal frequency division multiplexing (OFDM) is also very effective technique to mitigate intersymbol interference (ISI) in handling time dispersion of multipath fading channels. This is the fundamental problem for communication systems. OFDM also prevents ICI (inter carriers interference) by making all the subcarriers orthogonal to each other [19]. OFDM is a special case of multicarrier transmission in which a single information bearing stream is transmitted over many lower rate sub channels. It has various applications in optical communication also. It has been recently proposed for use in radio-over-fiber based links, in free space optical communication, in long haul optical communication systems, in multimode fiber links etc. For understanding the OFDM operation, it is essential to understand the concept of orthogonality.

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Orthogonality is also defined as the two coexisting signals are independent of each other in specified time interval and do not interact with each other as shown in fig 2.3. Here the six sub carriers are placed orthogonally such that the peak of one subcarrier occurs when other subcarriers are at zero. This is achieved practically with help of Inverse Fast Fourier Transform (IFFT) technique. Orthogonality is a property that allows multiple information signals to be transmitted perfectly over a common channel, thereby making better spectrum utilization. The signal is detected without interference. Ultimately ISI is conquered.

Loss of orthogonality results in blurring between the information signals and degradations in communications. Two periodic signals are orthogonal when the integral of their product, over one period, is equal to zero and they have integral number of cycles in the fundamental period. Orthogonality of subcarriers is crucial for OFDM system. If orthogonality is destroyed, the receiver will have a serious bit error rate due to (ICI). A cyclic extension of the signal in time domain called cyclic prefix (CP) is inserted between each OFDM symbol to eliminate ISI almost completely for it is larger than maximum of time delay, which keeps orthogonality between each subcarriers as well [20, 21].

3. Proposed OFDM Transceivers its Simulation:

The proposed design has been presented in this section. Figure 1 shows the diagram of proposed OFDM design. Radix-2 serialized FFT algorithm is used. The FFT block implements the Decimation-in-Time (DIT) FFT algorithm. It is composed of 9 stages of radix-2 butterfly units. These FFT stages are pipelined which further enhances its speed and is simulated up to 227.355 MHZ frequency. A serial FFT implemented in this model uses only one butterfly resource for each stage of implementation. With help of this area factor is also taken care of. Hence there is an optimized design in terms of both speed and area. As shown in the fig. 1, the proposed design consists of various stages.

QAM modulator modulates the signal using QAM (Quadrature amplitude modulation). QAM block is followed by insert pilot block. To generate OFDM successfully, some additional subcarriers, called pilot subcarriers, are added to create the reference at the receiver end, which carries out the channel estimation procedure to remove channel impairments.

II. OFDM

A. OFDM System with Multiplier:

Mathematically modulating a waveform and adding it is equivalent to taking an IFFT. This is because the time domain representation of OFDM is made up of different orthogonal sinusoidal signals which are nothing but inverse Fourier transform. The block diagram of digital OFDM system is shown in Fig 2.

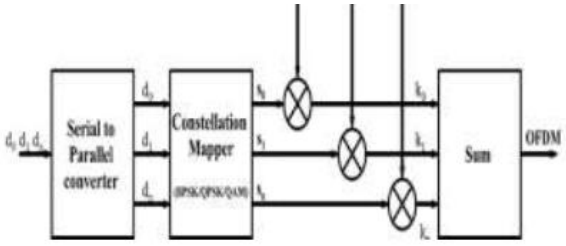

Fig. 1 Implementation of Analog OFDM system

B. Fast Fourier Transform:

The fast Fourier transform (FFT) and inverse fast Fourier transform (IFFT) are derived from the main function, which is called discrete Fourier transform (DFT). In DFT, the computation for N-points of the DFT will be calculated one by one for each point. While for FFT/IFFT, the computation is done simultaneously and this method saves quite a lot of time. The equations for FFT/IFFT function can be derived from the general DFT equation

$$X(k) = \sum_{n=0}^{N-1} x(n)\, e^{\frac{-j2\pi nk}{N}}$$

X(k)represents the DFT frequency output at the k-the spectral point where k ranges from 0 to (N-1). The quantity N represents the number of sample points in the DFT data frame. The quantity x(n) represents the nth time sample, where n also ranges from 0 to N-1. In general equation, x(n) can be real or complex. The input can be grouped into odd and even number.

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From fig. 3, the FFT computation is accomplished in five stages. The X(0) until X(31) variables are denoted as the input values for FFT computation and Y(0) until Y(31) are denoted as the outputs. There are two operations to complete the computation in each stage. The upward arrow will execute addition operation while downward arrow will execute subtraction operation. The subtracted value is multiplied with twiddle factor value before being processed into the next stage. This operation is done concurrently and is known as butterfly process.

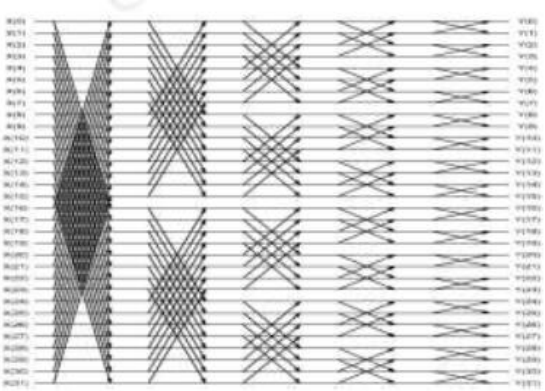

Fig. 2 32-point DIF-FFT

C. OFDM using FFT and IFFT:

The aim is to design an OFDM transmitter and receiver using FPGA. At the transmitter end, the OFDM signal is generated by implementing the IFFT. At the receiver end, the FFT is implemented.. Fig. 4 Implementation of Digital OFDM The objective is to use High-Speed-Integrated-Circuit to produce VHDL codes that carry out FFT and IFFT function.

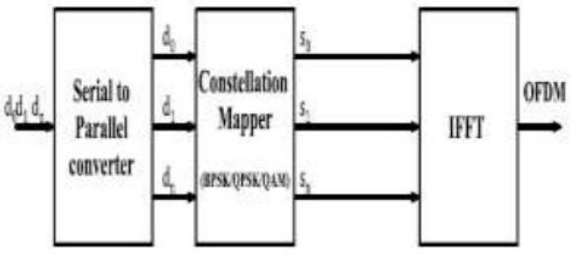

Fig. 4 Implementation of Digital OFDM

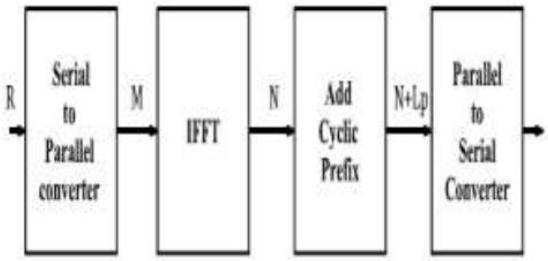

Fig. 4 OFDM Transmitter

Fig. 4 shows the OFDM transmitter communication system. The main focus is the FFT and IFFT part of the OFDM system. The input symbols are fed to the transmitter in series at R symbols/second. These symbols pass through a serial to parallel converter and output data on M lines in parallel. The M symbols are sent to an IFFT block that performs Npoint IFFT operation. The IFFT transform a spectrum (amplitude and phase of each component) into a time domain signal. An IFFT converts a number of complex data points, of length that is power of 2, into the same number of points in time domain.

The output is N time-domain samples. In order to preserve the sub-carrier orthogonality a cyclic guard interval is introduced. In this case, assumed a cyclic prefix of length Lp samples is pre-pended to the N samples. For example, assume N=4 and Lp=2; if the outputs of a 4 point inverse Fourier transform is [1 2 3 4], the cyclic prefix will be [3 4]. The cyclically extended symbol would be [3 4 1 2 3 4]. Therefore, the length of the transmitted OFDM symbol is N+Lp. Prepending the cyclic prefix aids in removing the effects of the channel at the receiver. ISI can occur when multi path channel cause delayed version of previous OFDM symbol to corrupt the current received symbol. If the value of Lp is greater than or equal to the size of the transmission channel, the ISI will only affect the cyclic prefix

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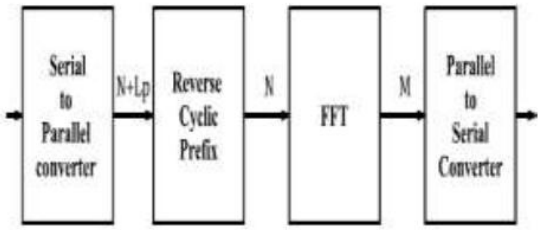

Fig. 5 OFDM Receiver

The received symbol is in time domain and it is distorted due to the effect of the channel. The received signal goes through a serial to parallel converter and cyclic prefix removal. After the cyclic prefix removal, the signals are passed through an N205 point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first M samples of the output. The work of the project is focused on the design and implementation of FFT for a FPGA kit. The direct mathematical derivation method is used for this design. In this project the coding is done in VHDL & the FPGA synthesis and logic simulation is done using Xilinx ISE Design Suite.

In 2013 M.Viswanadh, M.Harshavardhan Reddy and Naveena Boppana has given research paper on an efficient pipelined FFT Processor for OFDM communication systems. This paper will specifically address the power-efficient design of an FFT processor as it relates to emerging OFDM communications such as cognitive radio. In 2013, Nilesh Chide, Et. Al. [4] Proposed The Design Of OFDM System Using IFFT And FFT Blocks And Simulation Was Done On XILINX ISE. They Implemented The OFDM Block By Block And Finally Incorrect All Of Them Together To Form Complete OFDM Circuit.

Finally Their Aim Is To Implement The Core Signal Processing Blocks Of OFDM System Using VHDL Language. In 2012, Pradeepa M. and Gowtham P. [5] proposed an optimized implementation of the 8-point FFT processor with radix-2 algorithm in R2MDCarchitecture.The butterfly Processing Element (PE) used in the 8-FFT processor reduces the multiplicative complexity by using a real constant multiplication in one method and eliminates the multiplicative complexity by using add and shift operations in the proposed method. So they proposed conventional FFT algorithm by using butterfly technique and then proposed algorithm has been implemented by using R2MDC architecture. Then the analysis and design of FFT is done using VHDL. In 2012 International conference Tze-Yun Sung and Hsi-Chin Hsin has published a paper on Reconfigurable VLSI Architecture for FFT Processor This paper presents a CORDIC (Coordinate Rotation Digital Computer)-based split-radix fast Fourier transform (FFT) core for OFDM systems These FFT processors outperform the conventional ones in terms of both power consumption and core area.

In 2012, Manjunath Lakkannavar and Ashwini Desai [6] implemented the core processing blocks of an OFDM system, namely FFT and IFFT. The FFT and IFFT have been chosen to implement the design instead of the DFT and IDFT because they offer better speed with less computational time. The FPGA implementation of the project is performed using VHDL. The performance of the coding is analyzed from the result of timing simulation using Xilinx. In 2011, Pawan Verma and Harpreet Kaur [7] developed FFT &IFFT algorithms to be used in OFDM systems. The speed enhancement is the key contribution of the main processing blocks in OFDM system so they have successfully implemented the 8- point IFFT & FFT algorithm using VHDL to be used in the architecture of OFDM transmitter & receiver In 2011, K. Harikrishna and T. Rama Rao proposed Pipeline architecture for WiMAX technology using Radix-4Decimation in frequency FFT algorithm [1].

They proposed a memory based recursive FFT design which has much less gate counts, lower power consumption and higher speed. The proposed architecture has three main advantages: fewer butterfly iteration to reduce power consumption, pipeline of radix–22butterfly to speed up clock frequency, and even distribution of memory access to make utilization efficiency in SRAM ports.

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They coded this design in Verilog hardware description language with increase in speed & performance of OFDM. In 2011 Janne Janhunen work on Programmable Mimo Detectors ,The multiple-input multiple-output (MIMO) technique combined with an orthogonal frequency division multiplexing (MIMO--OFDM) has been introduced as a promising approach for the ever increasing capacity and quality of service (QoS) requirements for wireless communication systems. An efficient radio spectrum utilization expects a flexible transceiver solution, which has been the reason for the development of the software defined radio (SDR) technologies which in their turn are expected to enable the creation of cognitive radios. As a result, any radio solution could be invoked on demand on any platform.

We have studied detector algorithms and programmable processor architectures in order to find practical solutions for the futurewireless systems. A programmable receiver canreduce the energy dissipation of the receiver by changing the detection algorithm based on the current channel realizations. To provide a realistic aspect to the implementations in different channel realizations, we present a wide state-of-the-art detector comparison. In addition, they present an extensive number arithmetic and word length study in order to evaluate realistic hardware complexity and energy dissipations of the implementations. The study includes a comprehensive design chain from the algorithm development to the actual processor design and finally programming software for the platforms.

In 2010, Mounir Arioua et. al. [2] proposed an optimized implementation of 8-point FFT processor with radix-2 algorithm in R2MDC architecture. The main issue in FFT operation is the complex multiplication so, they tried to reduce the complexity one of two proposed methods replaces the expensive complex multiplication. Then they have proposed a novel 8-point FFT processor based on pipeline architecture with no complex multiplication and compared to Cooley-Tukey and R2MDC processor.

The proposed architecture gives an advantage in terms of area, complex multiplication reduction approach for Large Points FFT. In 2010 Chen-Fong Hsiao, Yuan Chen, Member, IEEE, and Chen-Yi Lee, Member, IEEE has work on a generalized mixed-radix algorithm for memorybased FFT Processors .It proposed for memorybased fast Fourier transform (FFT) processors to support prime-sized and traditional 2n-point FFTs simultaneously. It transforms the index to a multidimensional vector for efficient computation. By controlling the index vector to satisfy the "vector reverse" behavior, the GMR algorithm can support not only in-place policy for both computation and I/O data for continuous data flow to minimize the memory size but also multibank memory structures to increase the maximum throughput without memory conflict. Finally, a low-complexity implementation of an index vector generator is proposed for algorithm. In 2007, N. Madhavi, and R. Teymourzadeh [8] proposed an efficient algorithm using parallel and pipelining methods to implement high speed and high resolution FFT algorithm. Latency reduction is an important issue to implement the high speed FFT on FPGA.

The Proposed FFT algorithm shows the latency of 5131 clock pulse when N refers to 1024 points. For new architecture of the Radix-2 FFT algorithm, Verilog code was written and simulated by MATLAB software. In 2005, Zheng Wang Et. Al. [3] Simplified The Complex Multiplication Operation In The Design Of The FFT Structure For More General Case In Which The FFT Point Is Only Power Of Two Rather Than Four. They Discussed Theoretical Analysis Of The Delay In R2MDC Structure. In 2003 Jonas Claeson has work on design and implementation of an asynchronous pipelined FFT Processor FFT processors are today one of the most important blocks in communication equipment. They are used in everything from broadband to 3G and digital TV to Radio LANs. This thesis will deal with pipelined hardware solutions for FFT processors with long FFT transforms, 1k to 8k points. These processors could be used for instance in OFDM communication systems. The final implementation of the processor uses a

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GALS (Globally Asynchronous Locally Synchronous) architecture that implements the SDF (Single Delay Feedback) radix-22 algorithm.

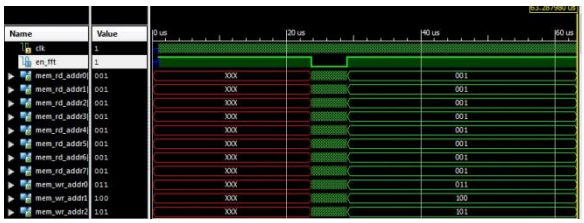

Figure 6 Simulation Result FFT output

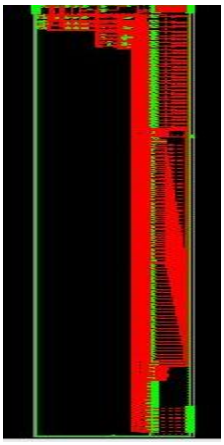

Figure 7 RTL Symatric of OFDM

IV. CONCLUSION:

We could propose a 32-point FFT & IFFT design for communication application like OFDM. The main objective of proposed architecture is to design efficient multiplication of FFT & IFFT using Vedic multiplication. It has numerous advantages such as: increase the speed, efficient timing, and better resource utilization parameter. In summary, speeds performance of our design easily satisfies most application requirements based on OFDM modulated wireless communication system.

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