ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design of Reversible Comparators with Priority Encoding Using Verilog HDL

B.Chaitanya Latha
M.Tech (VLSI SD),
Alfa College of Engineering and Technology.

V.Praveen Kumar, M.Tech (DSP)
Associate Professor,
Alfa College of Engineering and Technology.

Abstract:

Reversible computing is a model of computing where the computational process to some extent is reversible. A necessary condition for reversibility of a computational model is that the relation of the mapping states of transition functions to their successors should at all times be one-to-one. Reversible logic has emerged as an alternate design technique to the conventional logic, resulting in lower power consumption and lesser circuit area. Comparators are a key element in most digital systems. In this paper we propose two new reversible comparator designs based on the concept of priority encoding. The designs consist of mainly the Toffoli gates with both positive and negative control lines. The designs are optimized to reduce the quantum cost and delay. The proposed designs offer more than 40% improvement in delay over the existing serial comparator and the equation based comparator. We also propose modifications to the existing serial comparator and the equation based comparator for optimized performance.

Keywords:

Reversible logic, comparators, priority encoding, quantum cost, delay, logic depth.

I. INTRODUCTION:

Reversible logic has emerged as one of the key strategies for reducing the power dissipation occurring in the conventional logic circuits. In the conventional logic circuits, there is no one-to-one mapping between input and output. As a result, once the computation is completed, there is no way of recovering the exact inputs from the outputs. R. Landauer has shown that for every information bit lost during a computation, there is an energy dissipation of KTln2 Joules (K is the Boltzmann's constant and T is absolute temperature). Bennett later proved that the KTln2 Joules of dissipation can be avoided if the logic circuits are built using reversible logic gates. One-to-one mapping between input and output results in a unique output for each input combination, and hence the inputs can be recovered from the outputs after computation of results. One important restriction of the reversible designs is that fan-out is not allowed; every individual copy of a signal has to be uniquely generated. Reversible logic finds its application in the areas of quantum computing, nanotechnology and optical information processing. The design parameters for reversible logic circuits are the quantum cost, quantum delay, garbage outputs, constant inputs, and number of gates/gate count.

Comparators are an important element in most of the digital computation systems like microprocessors and microcontrollers, communication systems, encryption and decryption devices, and many more. Though the logic for comparing any two numbers is straight forward, the extensive use of comparators demands a low power and high speed operation. Various reversible comparator architectures have been proposed which are aimed at reducing the delay and the quantum cost of the circuit.In this paper we propose two new reversible designs which use the concept of priority encoding, and also modifications to the existing designs in [3] and [4] for optimizing the quantum cost and delay. The use of negative control lines in a Toffoli gate is explored in the designs; as a result the designs proposed in this work use only the standard reversible gates for which the synthesis

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

algorithms are available in literature[7],[8]. The proposed priority encoding based designs are based on the techniques described in [5] and [6]. These designs significantly reduce the delay and quantum cost when compared to the existing serial and equation based designs.The rest of the paper is organized into following sections: Section II gives a description of reversible logic gates and their design parameters. Section III presents some of the existing reversible comparator designs. The proposed designs are described in section IV and section V presents the comparison of different designs, conclusion and references follow.

II. REVERSIBLE LOGIC:

A Reversible logic gate is defined as a circuit with equal number of inputs and outputs and one-to-one mapping from input to output. In a reversible gate, in addition to obtaining outputs from the inputs one can retrieve the inputs for a particular output. The ancilla inputs, also called constant inputs, are the inputs maintained constant at either 0 or l in order to synthesize the given logical function. The Garbage outputs are the outputs which do not represent the required function. Garbage outputs are required to make the overall circuit reversible. Quantum cost of the circuit is the total number of primitive gates in the circuit. Controlled NOT, C- V, and C-V+ are the two input primitive gates,and inverter is one input primitive gate.The basic reversible gates are shown in fig l with their output functions, quantum cost, delay and the circuit symbol.

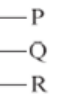
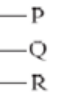
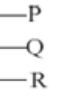
Reversible gate with output function	*Quantum Cost and Delay*	*Circuit Symbol*
Not Gate $P = \bar{A}$	1,1Δ	
Feynman Gate $P = \bar{A}$, $Q = A\ xor\ B$	1,1Δ	
Toffoli Gate $P = A, Q = B$, $R = AB\ xor\ C$	5,5Δ	
Negative Controlled Toffoli (NCT) $P = A, Q = B$, $R = \bar{A}\bar{B}\ xor\ C$	6,6Δ	
Fredkin gate $P = A$, $Q = \bar{A}B + AC$, $R = AB + \bar{A}C$	5,5Δ	

Figure l: Basic Reversible Gates

III. Existing Reversible Comparator Designs

A serial computation based reversible comparator design is presented in [4]. It consists of a l-bit comparator cell repeated N times, and one output stage. Each comparator cell, consisting of 9 inverters and 6 Toffoli gates, compares one bit of first number A with corresponding bit of second number B, and generates two outputs , Li & Gi, indicating whether Ai<Bi and Ai>Bi. The outputs of one – bit cell at the last stage, L & G, indicate A<B and A>B respectively. The final output stage, consisting of inverters and Toffoli gates, uses the L & G outputs from the previous stage, and generates three signals L, G & E indicating A<B, A>B and A=B respectively.

The l-bit comparator cell has quantum cost of 39, quantum delay of 24ǻ. It requires 6 constant inputs and produces 8 garbage outputs. The output stage has a quantum cost of 9 and quantum delay of 7ǻ. The logic depth of l-bit comparator cell is 8 and that of output circuitry is 3.A 4-bit reversible comparator circuit is proposed in [3]. In this design, the outputs A=B, A>B, and A<B are realized using the following equations.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

$$(A = B) = x3\ x2\ x1\ x0. \quad (1)$$

$$(A > B) = A3\ B3' + x3\ A2\ B2' + x3\ x2\ A1\ B1' + x3\ x2\ x1\ A0\ B0'. \quad (2)$$

$$(A < B) = A3'\ B3 + x3\ A2'\ B2 + x3\ x2\ A1'\ B1 + x3\ x2\ x1\ A0'\ B0. \quad (3)$$

$$xi = Ai\ Bi + Ai'\ Bi', for\ i = 0,1,2,3. \quad (4)$$

The equations of A=B and A>B are implemented using reversible not gate, TR gate, n-bit Toffoli gates. At the output stage, a BJN gate [l2] is used to generate the A<B output from A=B and A>B. The 4 – bit circuit has a quantum cost of l34 and a delay of ll6ấ and a logic depth of 9.

VI. PROPOSED DESIGNS:

In this section, we present the design methodology of the proposed reversible comparators. Fourdesigns are proposed in the paper, among which two are modification of existing reversible comparators, and the other two designs are based on the technique of priority encoding.

A. Modified serial comparator:

This design is a modification of the design in [4]. As shown fig 2, the one – bit cell has a total of 9 inverters and 6 Toffoli gates. The inverters are replaced by making use of negative control lines in the Toffoli gates. From this technique, for a one – bit cell the quantum cost is reduced by 7 and the delay by 3a.

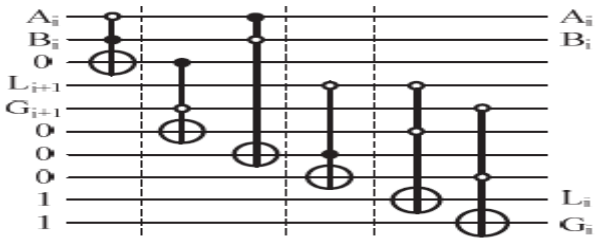


Figure 2: Modified one – bit comparator cell.

With the same technique extended for a 4 – bit comparator, the quantum cost reduces to l34, delay to 90a,and logic depth to 25.

B. Equation based modified comparator

The design proposed in [3] is modified by implementing all the functions using family of Toffoli gates. The TR gate at the input is replaced by a Toffoli gate with one negative control line and a Feynman gate. The n – bit controlled NOT gates are replaced using Toffoli gates. This results in a reduction of delay and quantum cost of the circuit. The BJN gate at the output is replaced using an NCT. The modified design of reversible 4 – bit equation based comparator is shown in the fig 3. The circuit has a quantum cost of 84, delay of 45a, and a logic depth of 9.

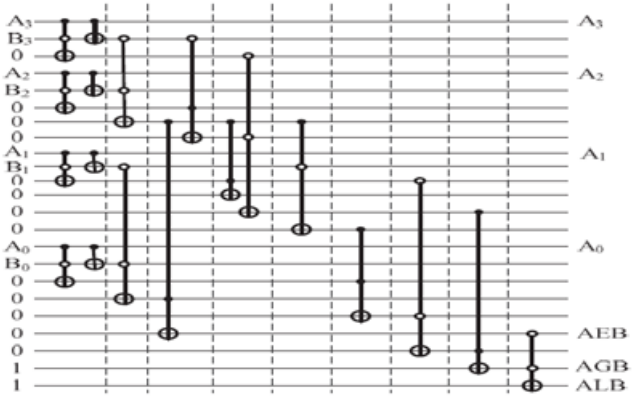


Figure 3: Equation based modified 4 – bit comparator

C. Priority Encoding based design – I:

The design proposed here is based on the logic described in [5]. Initially bit-wise XOR operation is performed on the input signals to generate an N – bit signal. Then a priority encoding scheme is employed such that only most significant logical high bit of the XOR result is set, and the rest are reset. Then a logical AND of this encoded signal with each of the inputs is performed individually. The output of this ANDoperation is then ORed to obtain the comparison result. The priority encoded signal is obtained using the set of equations given in equation 5 for a 4-bit comparator.

$$\begin{aligned} EP[3] &= Uneq_3 \\ EP[2] &= \overline{Uneq_3} \cdot Uneq_2 \\ EP[1] &= \overline{Uneq_3} \cdot \overline{Uneq_2} \cdot Uneq_1 \\ EP[0] &= \overline{Uneq_3} \cdot \overline{Uneq_2} \cdot \overline{Uneq_1} \cdot Uneq_0 \end{aligned} \quad (5)$$

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

This design requires Feynman gates, and Toffoli gates with both positive and negative control lines. The reversible circuit for a 4 – bit comparator is shown in fig 4. It has quantum cost of l33, delay of 58a, and logic depth of l2.

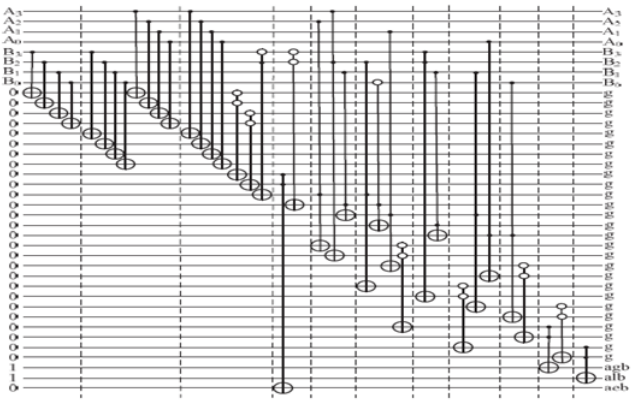


Figure 4: Reversible four - bit comparator circuit of the proposed Priority encoding based design – I

D. Priority encoding based design – II

This design is based on the logic presented in [6]. Initially a bitwise comparison is performed on the input bits. Then the bitwise comparison results are encoded into two N – bit buses corresponding to A>B and A<B. Then the N – bits in each bus are ORed together to obtain the final comparison result for A>B and A<B. The result for A=B is obtained by taking the NOR of A>B and A<B. The N – bit buses are such that there is only one bit which is logical high. This occurs at the position corresponding to the first unequal bit. The logical high value is obtained in only one of the two N – bit buses indicating whether A is greater or B is greater.The reversible comparator circuit is designed using Feynman, NCT, Fredkin, and Toffoli gates. The quantum circuit for 4 – bit comparator is shown in fig 5. It has quantum cost of ll9, delay of 5lå, and logic depth of l0.

V. RESULTS AND ANALYSIS

In this section the proposed comparator designs are compared with the existing designs. A generalized formula is derived for the N-bit comparison for all the proposed designs.

For the serial based design presented in [4], the l-bit comparator is used for designing the 4 – bit comparator, which has quantum cost of l65, delay of l03å. For the 4 – bit comparator with the proposed modification as described in section III.A, the quantum cost is{4*(39-7)+(9-3)=134} and the quantum delay is {4*(24-3)+(7-1)=90}.The modified circuit has 24 garbage outputs and a logic depth of l7. The comparison of the parameters of existing serial design with the modified one is shown in table I for a 4- bit comparator. For N-bit comparator, the quantum cost can be derived as 32N+6,and delay as 21N+6.

The garbage output is given as 6N,the logic depth as 4N+1.For the equation based design presented in [3], the quantum cost and delay are not discussed by the authors, but can be calculated as l34 and ll6a respectively.Though the gate count is less, the higher values of cost and delay are due to the N-bit Controlled NOT gates used in the design. The modification to design proposed in section III.B is mainly aimed at reducing the delay and cost of the circuit with a trade-off in garbage outputs and ancilla inputs.

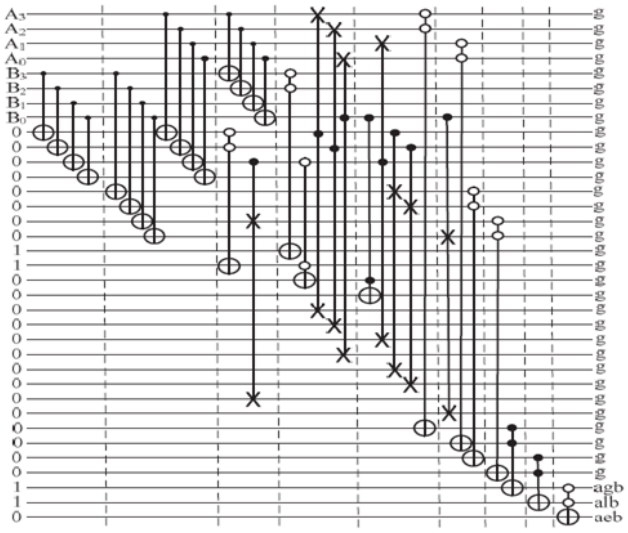


Figure 5: Reversible four- bit comparator circuit of the proposed Priority encoding based design – II.

TABLE I. COMPARISON OF 4-BIT SERIAL COMPARATOR

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

	Cost	Delay	No. of gates	Logic depth
Serial design[4]	165	103	65	35
Modified Serial design	**134**	**90**	**25**	**17**
% Improvement	18.8	12.62	61.54	51.43
Modified Serial design for N-bit inputs	32N+6	21N+6	6N+1	4N+1

The comparison of the parameters of existing equation based design with the modified one is shown in table II for a 4-bit comparator. The N-bit comparator of the equation based modified design is obtained by expanding the equations (l) to (4) for N-bit operands. The quantum cost for such circuit is derived as 27.5N-10, and delay as 3N +33+6$\log_a\Delta$. The term 6$\log_{aN}$ is applicable only for N > 8.

TABLE II. COMPARISON OF EQUATION BASED 4-BIT COMPARATOR

	Quantum Cost	Quantum Delay
Equation based design[3]	134	116
Modified design	**84**	**45**
% improvement	37.3	61.2
Equation based Modified design for N-bit inputs	27.5N - 10	$3N + 33 + 6\log_8 N$

The 4-bit comparator circuit of proposed priority encoding based design-I has l6 Feynman gates and 22 Toffoli family gates as shown in fig 4. The circuit requires 30 ancilla inputs and produces 27 garbage outputs. The N-bit comparator based on this design can be obtained either by extending set of equations in (5) or by grouping suitable number of 4-bit comparators. For an N-bit comparator, the quantum cost and delay are given as 43.5N-41 and 4N=42=6 l0g_aNΔ respectively. The term 6$\log_a$N is applicable only for N > 8.

The 4-bit comparator circuit of proposed priority encoding based design-II has l6 Feynman gates, 8 Fredkin gates, and ll Toffoli family gates as shown in fig 5. The priority encoding scheme in this design is the same as that used in priority encoding based design-I. However instead of using the AND operation with input bits, here multiplexers are used. The circuit requires a logic depth of l0, and 25 constant inputs, and has 30 garbage outputs for 4-bit comparator. The same logic can be extended to N-bit comparator in two ways similar to design-I.

The quantum cost for N-bit comparator is given as 33.5N-21 and delay is given as 4N+35Δ. The improvement in quantum cost and delay for the proposed priority encoding based reversible 4-bit comparators are summarized in the table III.

TABLE III. COST AND DELAY COMPARISON OF 4-BIT PRIORITY ENCODING BASED REVERSIBLE COMPARATORS

	Quantum Cost	Quantum Delay (Δ)
Serial design[4]	165	103
Equation based design[3]	134	116
Priority encoding based design I	**133**	**58**
Priority encoding based design II	**113**	**51**
% improvement of Priority encoding based design I w.r.t [4]	*19.4*	*43.7*
% improvement of Priority encoding based design II w.r.t [4]	*31.52*	*50.48*
% improvement of Priority encoding based design I w.r.t [3]	-	*50*
% improvement of Priority encoding based design II w.r.t [3]	*15.67*	*56.03*

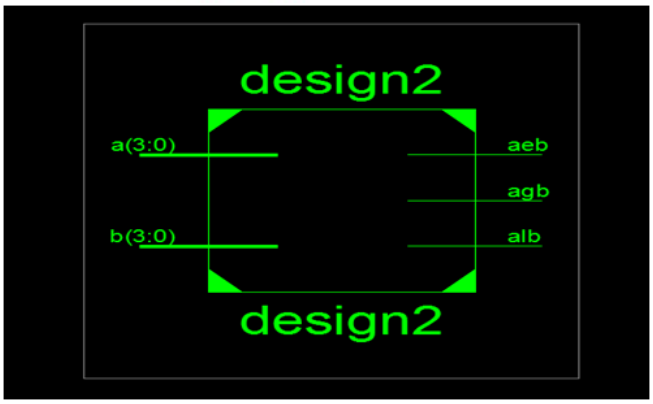
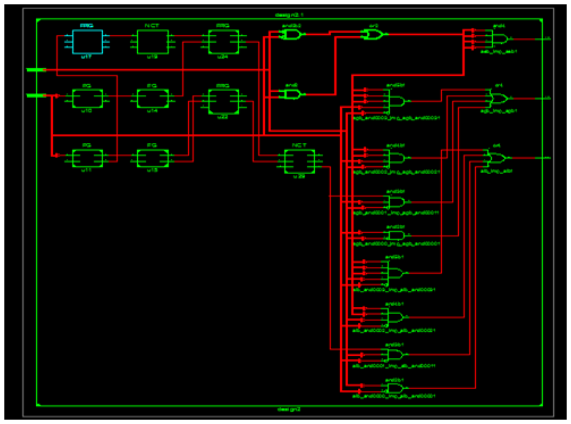


Figure 6: RTL schematic of Reversible four- bit comparator circuit of the proposed Priority encoding based design – II.



ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Figure 7: RTL schematic of Reversible four- bit comparator circuit of the proposed Priority encoding based design – II.

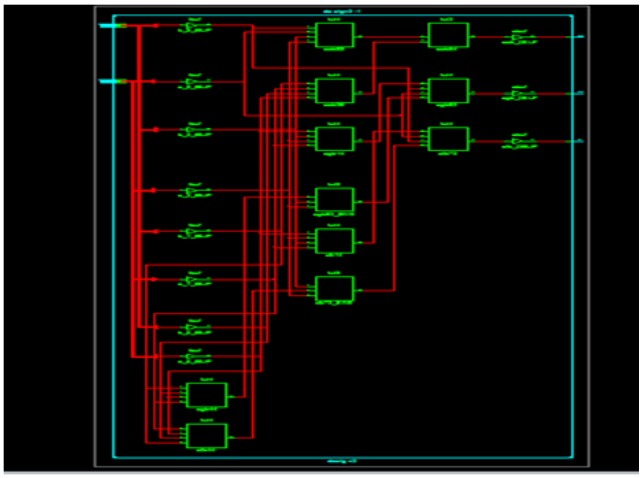


Figure 8: Technology schematic of Reversible four- bit comparator circuit of the proposed Priority encoding based design – II.

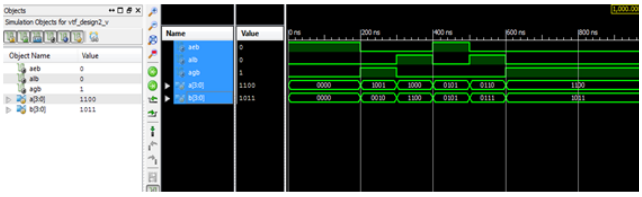


Figure 9: Simulation results of Reversible four- bit comparator circuit of the proposed Priority encoding based design – II.

CONCLUSION:

This paper presents modifications to two existing reversible comparator designs and two new designs based on Priority encoding technique. The circuits were designed in Verilog, and verified using XilinxISE. From the results it is evident that the proposed Priority encoding based designs have a maximum of 56.03% reduction in delay and 3l.52% reduction in quantum cost with trade-offs in other design parameters. Further work can be focussed on multiple parameters optimization.

REFERNCES

[l]R. Landauer, "Irreversibility and heat generation in the computational process", IBM J. Res. Develop., vol. 5, pp. l83-191,1961.

[2]C. H. Bennet, "Logical reversibility of computation", IBM J. Res. Develop., vol. l7, no. 6, pp. 525- 532, l973.

[3]Soolmaz Abbasalizadeh, Behjat Forouzandeh, and Hossein Aghababa, "4 Bit Comparator Design Based on Reversible Logic Gates", Lecture Notes on Information Theory Vol. l, No. 3, September 20l3, Engineering and Technology Publishing.

[4]A. N. Al-Rabadi, "Closed-system Quantum Logic Network implementation of the Viterbi Algorithm," Facta universitatis- Ser.:Elec. Energ., vol. 22, no. l, pp. l–33, April 2009.

[5]Chung-Hsun Huang, Jinn-Shyan Wang, "High-Performance and Power-Efficient CMOS Comparators", IEEE Journal of Solid-State Circuits, Vol. 38, No. 2, February 2003.

[6]Saleh Abdel-Hafeez, Ann Gordon-Ross, and Behrooz Parhami,"Scalable Digital CMOS Comparator Using a Parallel Prefix Tree", IEEE Transactions On Very Large Scale Integration (VLSI) Systems Vol. 2l, No. ll, November 20l3.

[7]R. Feynman, "Quantum Mechanical Computers," Foundations of Physics, vol. l6, issue 6, l986.

[8]T. Toffoli, "Reversible computing," MIT Lab for Computer Science, Tech. Rep. Tech memo MIT/LCS/TM-151, l980.

[9]Nagamani A N, Jayashree H V, H R Bhagyalakshmi, "Novel Low Power Comparator Design using Reversible Logic Gates ", Indian Journal of Computer Science and Engineering (IJCSE), Vol. 2 No. 4 Aug -Sep 20ll.

[l0]Kamalika Datta et.al, "Exploiting Negative Control Lines in the Optimization of Reversible Circuits", Springer-Verlag, pp.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[ll]Wille, R., Soeken, M., Przigoda, N., Drechsler, R, "Exact synthesis of Toffoli gate circuits with negative control lines", International Symposium on Multi-valued Logic (ISMVL), pp.

[l2]Raghava Garipelly, P.Madhu Kiran, A.Santhosh Kumar, "A Review on Reversible Logic Gates and their Implementation", International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 3, March 20l3.

[l3]Mona Arabzadeh, Mehdi Saeedi, RCViewer+, version 2.5,20l3,available at

http://ceit.aut.ac.ir/QDA/RCV.htm