ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Implementation of Reversible Arithmetic and Logic Unit (ALU)

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Abstract:
In low power circuit design, reversible computing has become one of the most efficient and prominent techniques in recent years. In this paper, reversible Arithmetic and Logic Unit (ALU) is designed to show its major implications on the Central Processing Unit (CPU).In this paper, two types of reversible ALU designs are proposed and verified using Altera Quartus II software. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed design 1, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the proposed ALU design 2. Both proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design.

Index Terms:
Reversible ALU design, reversible full adder, propagation delay.

I. INTRODUCTION:

For the past decades, there were numerous of difficulties and problems occurred in the development of conventional computing technologies. The major problem of the conventional computing technologies is power dissipation which is an important issue in today's computer chip [1].

The advancement in Very Large Scale Integrated (VLSI) designs especially in portable device technologies lead to faster, smaller and more complex electronic system design [2]. In VLSI design, the conventional logic circuits dissipate more power. In the conventional logic circuits, every bit of information loss will generate kTlog2 joules of heat energy [3]. In the conventional logic circuit design, information loss occurs due to the total number of output signals is less than the total number of input signals applied to the logic circuit.Reversible computing is a promising method in low power dissipating circuit design for current technologies such as low power Complementary Metal Oxide Semiconductor (CMOS) design, cryptography, optical information processing, quantum computing and nanotechnology [4]. Reversible logic can be defined as thermodynamics of information processing. Hence, it is used to reduce the power dissipation by preventing the loss on information. It is shown in [5, 6] that the circuit which designed using reversible logic can eliminate the heat dissipation due to information loss. This is due to the amount of energy dissipated in a system which bears a direct relationship to the number of bits erased during computation. The difference between the reversible circuits and conventional logic circuits is that the reversible circuits are built from reversible logic gates.Arithmetic and Logic Unit (ALU) works as a data processing unit which is an important part in the central process unit (CPU) of any computer architecture. ALU is a multi-functional circuit that performs one of a few possible functions on two operands and which depends on the

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control inputs [7]. ALU needs to continually perform during the life-time of any computational devices such as a computer or a hand held device such as hand phone. Thus, reversible logic can be implemented in designing ALU to reduce the power dissipation and propagation delay in the circuits [8].In this paper, two new reversible ALU designs are proposed using two different reversible full adder logic circuits. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed reversible ALU design 1, Peres Full Adder Gate (PFAG) is used in the design, HNG gate [9] is used as an adder logic circuit in the proposed reversible ALU design 2. The proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay.

A short review on few existing reversible gates is detailed in section-II of the paper. Section-III introduces the proposed ALU designs. The simulations results are shown in section-IV where comparison between the existing ALU designs with the proposed architecture is presented and finally the paper is concluded in section-V.

II REVERSIBLE LOGIC GATE:

A reversible logic gate is said to be reversible if the number of inputs is equal to the number of outputs. In order to achieve a synthesized low power circuits, the reversible logic gate circuits should have the following specifications which are minimum number of reversible gate or gate count, minimum number of garbage outputs, minimum propagation delay and minimum quantum cost [11]. In the proposed ALU designs, R-I, Feynman, Fredkin and Peres reversible gates are used. The quantum implementations of the three gates are described in the following subsections.

A. Feynman gate

Feynman gate is also known as controlled-Not gate (CNOT).It is a reversible of 2*2 gate with 2 inputs and 2 outputs. The quantum cost of Feynman gate is one. This is proven since it has mapping input of A and B to output of P and Q as shown in the Fig.1[12]. Feynman gate is made from one EX-OR gate.

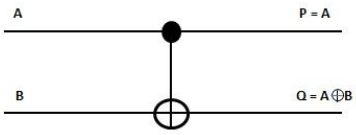

Fig.1:Quantum implementation of Feynman gate

B. Fredkin gate

Fredkin gate is a reversible of 3*3 gate with 3 inputs and 3 outputs. The quantum implementation of the gate is shown in the Fig.2 that the inputs (A, B, C) are mapped to the outputs (P, Q, and R) and the quantum cost of Fredkin gate is five. The two dotted rectangles in the Fig. 2 is equivalent to a 2*2 Feynman gate with the quantum cost of one for each dotted rectangle. The other 3 quantum cost comes from one V and two CNOT gates [12].

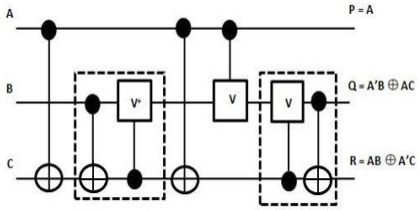

Fig2:Quantum implementation of fredkin gate

C. R-I gate

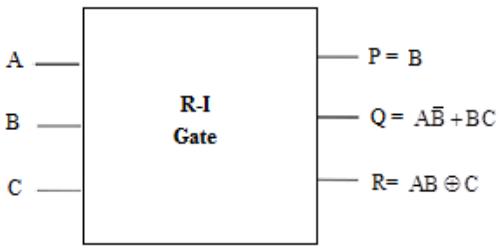

Fig 3:Qunatum implementation of R-I gate

R-I gate is a reversible of 3*3 gate with three inputs and three outputs. The Fig. 3 shows the proposed R-I reversible gate. The outputs are defined by P=B, Q= AB + BC , R=AB ⊖ C. R-I

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gate requires only 7 transistors for the transistor level implementation. A single block of R-I gate can be realized as, Multiplexer, De-Multiplexer, XOR, AND, OR, NOT etc. R-I gate is made from one EX-OR, one OR, one NOT and three AND gate.

III. PROPOSED ALU DESIGN:

ALU works as a data processing components which is an important part in the central process unit(CPU).Besides, it is an main performer in any computing devices.ALU is a multi-functional circuit that performs one of a few possible functions on two operands of A and B which is depending on the control inputs.

A. Conventional ALU Design

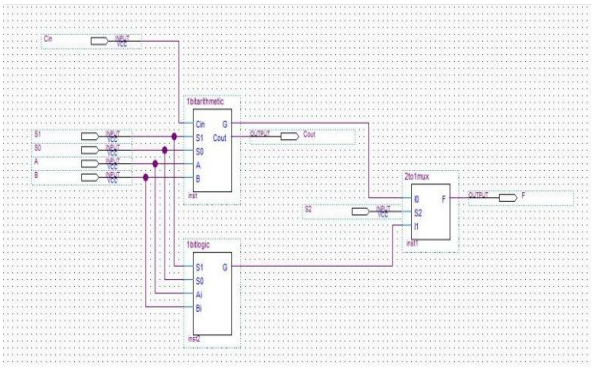

Fig 4: Block diagram of 1-bit conventional ALU design in Quartus II software

As show in Fig.4, the S_2, S_1 and S_0 are the selection lines while C_{in} is the input carry. Input A and B are the data input for the ALU design. Based on the truth table shown in Table 1, when selection line S_2 is equal to zero, the circuit performs eight arithmetic operations and when selection line S_2 is equal to one, the circuit performs the logic operations of OR, EX-OR, AND and NOT functions.

Table 1:Function table of ALU

S_2	S_1	S_0	C_{in}	Operation	Function
0	0	0	0	F = A	Transfer A
0	0	0	1	F = A+1	Increment A
	0	1	0	F = A+B	Addition
0	0	1	1	F = A+B+1	Add with carry
0	1	0	0	F = A+B’	Subtract with borrow
0	1	0	1	F = A+B’+1	Subtraction
0	1	1	0	F = A-1	Decrement A
0	1	1	1	F = A	Transfer A
1	0	0	X	F = A∨B	OR
1	0	0	X	F = A⊕B	EX-OR
1	0	1	X	F = A^B	AND
1	0	1	X	F = A’	NOT

Fig.4 is the logic circuit design for 1-bit conventional ALU which is implemented in Altera Quartus II software. 4-bits,8-bits and 16-bits of conventional ALU design can be implemented by expanding 1-bit ALU design.

B. Reversible ALU

The proposed reversible ALU is designed to produce the same function as implemented by conventional ALU. Fig.5 is the block diagram of proposed reversible ALU designs. It has two main logic circuit design, namely, control unit and reversible full adder and the proposed design has five constants signals (e.g: C_{input1}, C_{input2}, C_{input3}, C_{input4} and C_{input5}) with a provision for realizing the eight arithmetic operations and four logic operations.

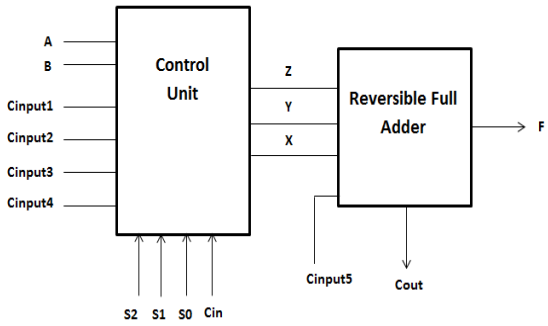

Fig 5: Block diagram of reversible ALU design

1) Control unit

Control unit is a critical part in the reversible ALU design. Control unit performs the arithmetic operations inside the ALU.

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As shown in Fig.6, the proposed control unit design is made up from three Feynman gates, three R-I gates and one Fredkin gate. Four control variables S_2, S_1, S_0 and C_{in} select twelve different operations in the reversible ALU design. The arithmetic and logic operations are differentiated using the variable input of S_2. The control unit has four constant signals. There are eight garbage outputs in the proposed control unit logic circuit.

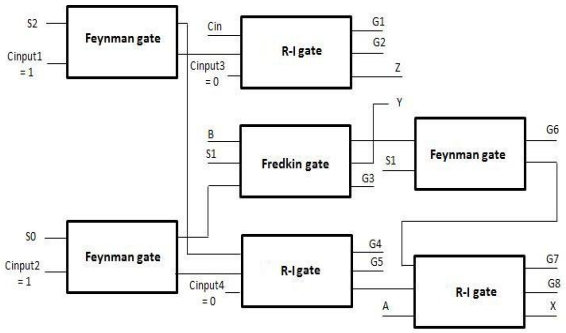

Fig 6: Block diagram of control unit

2) Reversible Full adder:

Full adder is the important building block in ALU unit. Compatible reversible adder implementations is required in the anticipated paradigm shift logic compatible with the optical and quantum. The outputs of the reversible adder are given in the following equations:

Sum=A⊕B⊕Cin
Cout= (A⊕B)Cin⊕AB

a) PFAGGate

The PFAG gate is 4*4 revesible gate. Outputs, P and Q are considered as the garbage output. The output, R and S are represented the function of sum and Cout respectively. The quantum cost of PFAG is 8 since it made from 2 peres gates[13].Fig.7 is the logic circuit design of PFAG gate in Quartus II software.

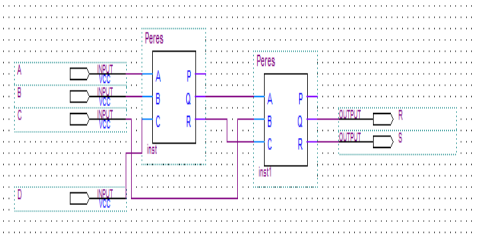

Fig 7: Logic circuit design of PFAG gate in Quartus II software

b) HNG gate:

The HNG gate is 4x4 reversible gate. Outputs, P and Q are considered as the garbage output. The outputs, R and S are represented the function of Sum and Cout respectively. The quantum cost of HNG gate is 6 [14]. Fig.8 is the logic circuit design of HNG gate in Quartus II software.

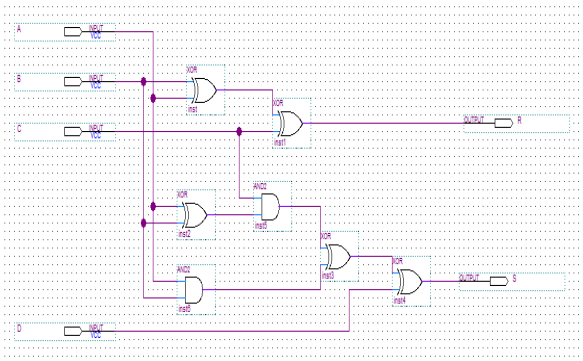

Fig 8: Logic circuit design of HNG gate in Quartus II software

3) Proposed Reversible ALU Design I

Shown in Fig. 9 is the block diagram of the proposed reversible ALU design 1. The proposed ALU design is implemented in Altera Quartus II software which is show in Fig.10.

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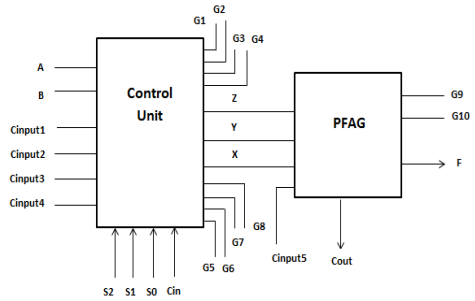

Fig 9: Block diagram of the proposed reversible ALU design I

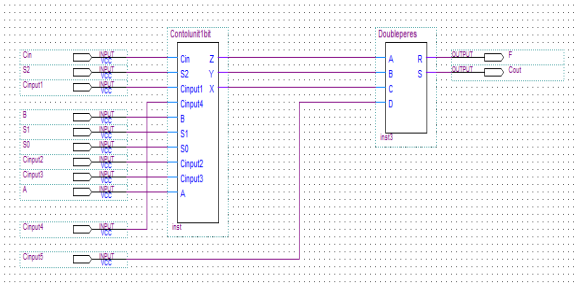

Fig 10: Logic circuit design of proposed reversible ALU design I in Quartus II software

4) Proposed Reversible ALU design2

Shown in Fig. 11 is the block diagram of the proposed reversible ALU design 2

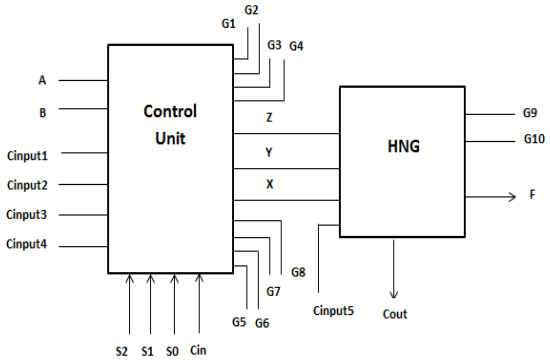

Fig 11: Block design of the proposed reversible ALU design 2

Shown in Fig.12 is the logic circuit design for 1-bit reversible ALU which is implemented in Quartus II software. 4-bits, 8-bits and 16-bits of reversible ALU design can be implemented from 1-bit ALU design.

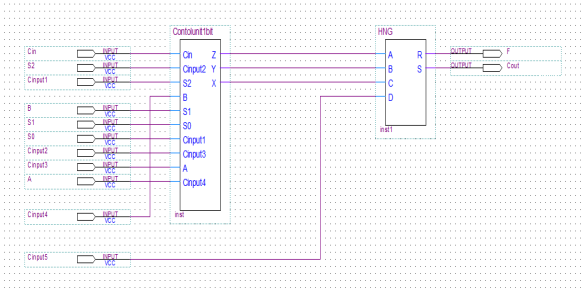

Fig 12: Logic circuit design of proposed reversible ALU design 2in Quartus II software

IV. SIMULATION RESULTS

Shown in Fig.13 is the simulation in QSim waveform simulator for both reversible PFAG and HNG gates and the function of the adder circuits can be verified through the simulations

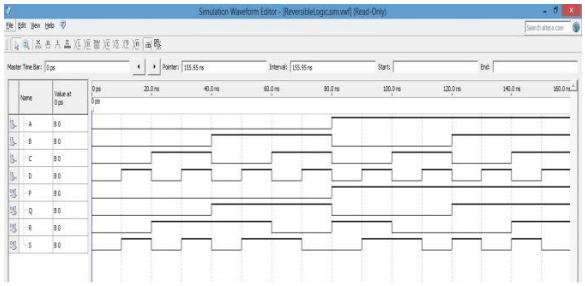

Fig 13: Simulation waveform for reversible full adder

Shown in Fig.14 is the output simulation in QSim waveform simulator for both reversible ALU designs. The output simulations satisfy the function Table 1 for A=0 and B=1.

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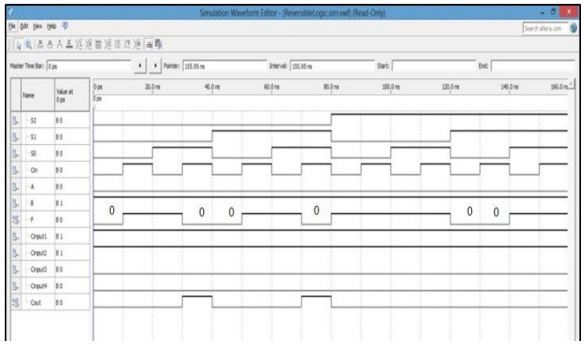

Fig 14: Simulation waveform for reversible ALU design

Table 3 and Table 4 show the performance comparison of the conventional ALU design with the proposed reversible ALU designs. For comparison, number of gate count, garbage output, quantum cost, and propagation delay are considered as the performance matrices

Table 3: Comparison between the proposed reversible ALU design 1 and design 2

Parameter which has to be compared	Gate count	Garbage output	Quantum cost
Design 1:control unit + PFAG	9	10	28
Design 2:control unit + HNG	8	10	26

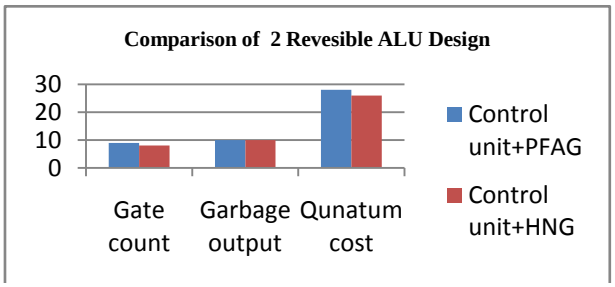

Fig 15 comparison of 2 reversible ALU design based on three parameter

Table 4: comparison of propagation delay between the conventional ALU and reversible ALU design

Number of bits	Reversible ALU design 1(ns)	Reversible ALU design 2(ns)	Conventional ALU(ns)
1-bit	7.75	7.17	8.17
4-bit	8.38	8.13	8.73
8-bit	8.79	8.29	9.43
16-bit	7.39	8.26	9.13

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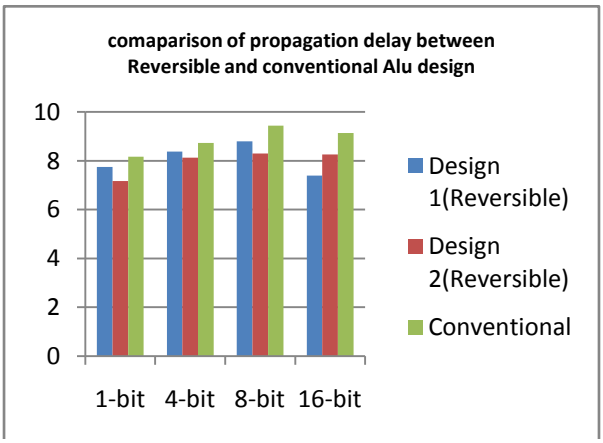

Fig 16: Comparison of propagation delay between the conventional and reversible ALU design

Table 3 shows the comparison between the proposed design 1 and design 2 of the reversible ALU. We can depict from the Fig. 15 that the proposed reversible ALU design 2 is better than the proposed reversible ALU design 1. Based on Table 4, the comparison on propagation delay between two designs of reversible ALU and the conventional ALU is made. Based on the result as shown in Fig. 16, we can conclude that the proposed reversible ALU design 2 shows higher reductions in propagation delay as compared to the proposed design 1. Hence, design 2 of reversible ALU is the best design compared to design 1 which meets the requirements of the reversible logic by having the low propagation delay.

V. CONCLUSION:

In this paper, the reversible ALU design is proposed with two unique design paradigms. The proposed reversible ALU designs are verified using Altera Quartus II software. Both proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The Simulation results illustrate that the proposed reversible ALU design 1 and conventional ALU design.

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