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Low-Power and Area-Efficient Shift Register Using Digital Pulsed Latches

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Abstract:

This paper proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using a 0.18 CMOS process with . The core area is . The power consumption is 1.2 mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops.

I. INTRODUCTION:

ASHIFT register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters [1], communication receivers [2], and image processing ICs [3]–[5]. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register [3]. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register [4]. A 16-megapixel CMOS image sensor uses a 45K-bit shift register [5]. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop [6]–[9]. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

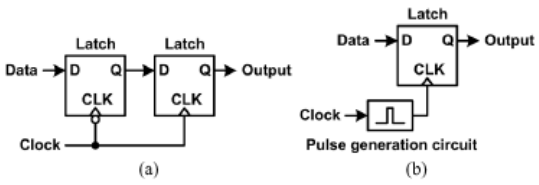

Fig. 1. (a) Master-slave flip-flop. (b) Pulsed latch.

This paper proposes a low-power and area-efficient shift register using pulsed latches.

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The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. The rest of the paper is organized as follows: Section II describes the architecture of the proposed shift register. Section III presents the measurement results of the fabricated chip. Finally, conclusions are drawn in Section IV.

II. ARCHITECTURE:

A. Proposed Shift Register:

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock

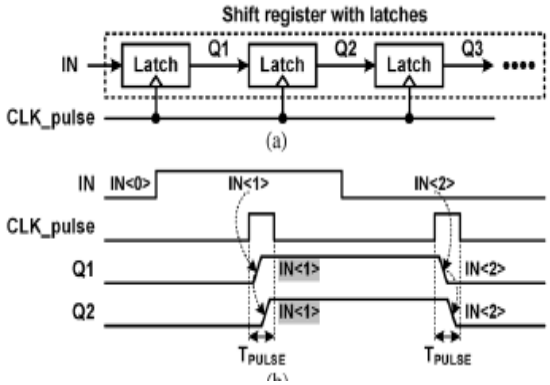

Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.

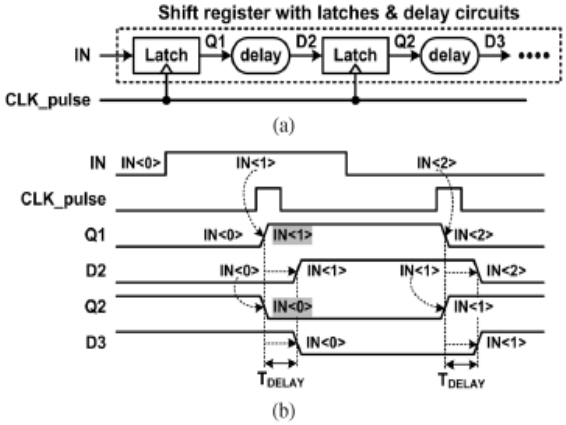

Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms.

pulse and no timing problem occurs between the latches. However,the delay circuits cause large area and power overheads.Another solution is to use multiple non-overlap delaye pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. Fig. 5(a) shows an example the proposed shift register.

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The proposed shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse□ 1:4□ □ and CLK_puls□ T□). In the 4 bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 5(b) shows the operation waveforms in the proposed shift register. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK_pulse□ T□ updates the latch data T1 from Q4. And then, the pulsed clock signals CLK_pulse□ 1:4□ □ update the four latch data from Q4 to Q1 sequentially. The latches Q2–Q4 receive data from their

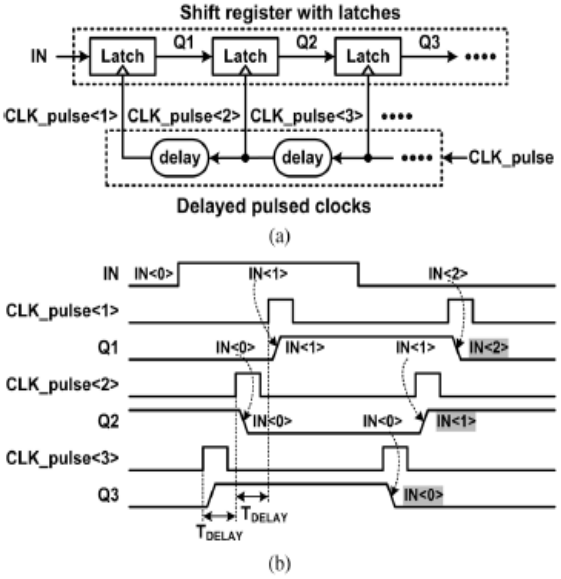

Fig. 4. Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register. The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in Fig. 6 each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an $N-bit$ shift register is divided into $K-\text{bit}$ sub shift registers, the number of clock-pulse circuits is $K+1$ and the number of latches is $N+N/K$. A $K-bit$ sub shift register consisting of $K+1$ latches require $K+1$ pulsed clock signals. The number of sub shift registers (M) becomes N/K , each sub shift register has a temporary storage latch. Therefore, N/K latches are added for the temporary storage latches. The conventional delayed pulsed clock circuits in Fig. 4 can be used to save the AND gates in the delayed pulsed clock generator in Fig. 6.

In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals. The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register (K). K is selected by considering the area, power consumption, speed. The area optimization can be performed as follows. When the circuit areas are normalized with a latch, the areas of a latch and a clock-pulse circuit are 1 and, respectively. The total area becomes $\alpha_A \times (K+1)+N(1+1/K)$. . The optimal $K(=\sqrt{N/\alpha_A})$ for the minimum area is obtained from the first-order differential equation of the total area $(0 = \alpha_A - N/K)$.

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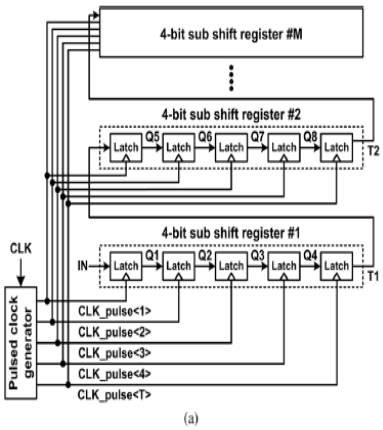

Fig. 5. Proposed shift register. (a) Schematic. (b) Waveforms.

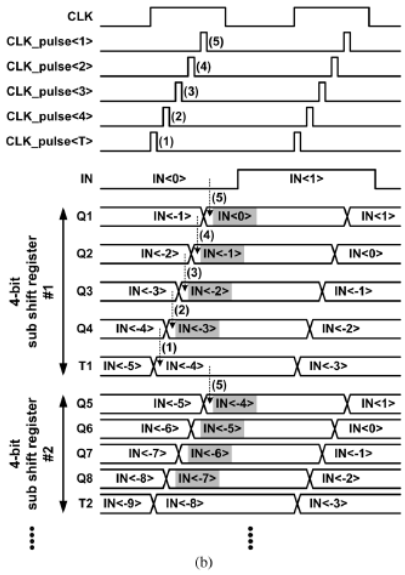

Fig. 5. Proposed shift register. (a) Schematic. (b) Waveforms.

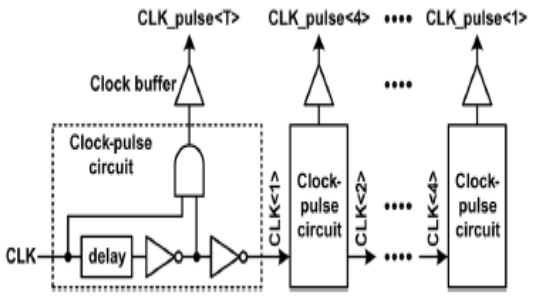

Fig. 6. Delayed pulsed clock generator.

integer K for the minimum area is selected as a divisor of ,which is nearest to $\sqrt{N/\alpha_A}$

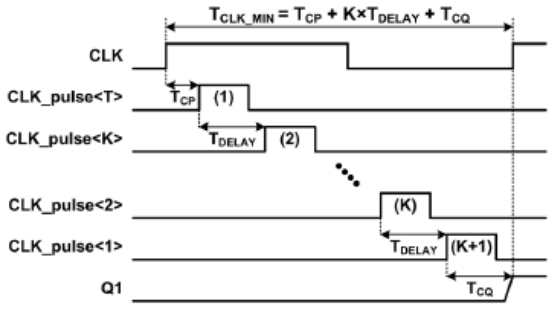

Fig. 7. Minimum clock cycle time of the proposed shift register.

The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are 1 and α_P, respectively. The total power consumption is also $\alpha_P \times (K+1) + N(1+1/K)$. An integer K for the minimum power is selected as a divisor of N, which is nearest to $\sqrt{N/\alpha_P}$. In selection, the clock buffers in Fig. 6 are not considered. The total size of the clock buffers is determined by the total clock loading of latches. Although the number of latches increases from N, to N to $N(1+1/K)$, the increment ratio of the clock buffers is small. The number of clock buffers is K. As K $1/K$ increases, the size of a clock buffer $(M = N/K)$ decreases in proportion to $1/K$ because the number of latches connected to a clock buffer is proportional to . Therefore, the total size of the clock buffers increases slightly with increasing K and the effect of the clock buffers can be neglected for choosing K. The maximum number of K is limited to the target clock frequency. As shown in Fig. 7 the minimum clock

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cycle time is (T_{CLK_MIN}) is $T_{CP} + K \times T_{DELAY} + T_{CQ}$, where T_{CP} is the delay from the rising edge of the main clock signal (CLK) to the rising edge of the first pulsed clock signal (CLK_pulse□ T□), is the delay of two neighbor pulsed clock signals, is the delay from the rising edge of the last pulsed clock signal (CLK_pulse□ 1□) to the output signal of the latch Q1 (T_{CLK_MIN}) is proportional to K. As K increases, the maximum clock frequency $(f_{CLK\_MAX} = 1/T_{CLK\_MIN})$ decreases in proportion to $1/K$. Therefore K, must be selected under the maximum number which is determined by the maximum clock frequency of the target applications. The pulsed clock signals in Fig. 7 are supplied to all sub shift registers. Each pulsed clock signal arrives at the sub shift registers at different time due to the pulse skew in the wire. The $K + 1$ pulse skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock signals have almost the same pulse skews when they arrive at the same sub shift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small.

The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Also, the pulse skew differences between the different sub shift registers do not cause any timing problem, because two latches connecting two sub shift registers use the first and last pulsed clocks (CLK_pulse□ T□ □ and CLK_pulse□ 1□) which have a long clock pulse interval.

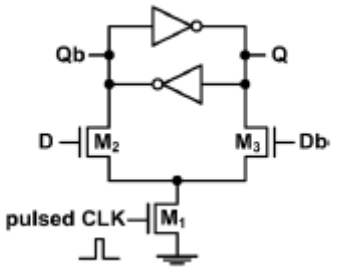

Fig. 8. Schematic of the SSASPL [6].

In a long shift register, a short clock pulse cannot through a long wire due to parasitic capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the maximum clock frequency. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees.

B. Chip Implementation

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flipflops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig. 8, which is the smallest latch, is selected. The original SSASPL with 9 transistors [6] is modified to the SSASPL with 7 transistors in Fig. 8 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal. The SSASPL updates the data with three NMOS transistors $(M_1 - M_3)$ and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data (D and Db). The pull-down current of the NMOS transistors $(M_1 - M_3)$ must be larger than the pull-up current of the PMOS transistors in the inverters.

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The SSASPL was implemented and simulated with a $0.18\ \mu m.$ CMOS process at $V_{DD} = 1.8V$. The sizes (W/L) of the three NMOS transistors are $1\ \mu m/0.18\ \mu m.$. The sizes of the NMOS and PMOS transistors in the two inverters are all $0.5\ \mu m/0.18\ \mu m$. The minimum clock pulse width of the SSASPL to update the data is 62 ps at a typical process simulation (TT) and 54–76 ps at all process corner simulations (FF-SS). The rising and falling times of the clock pulse are approximately 100 ps. The clock pulse shape can be degraded due to the wire delay, signal coupling, supply noise. The clock pulse width (T_{PULSE}) of 170 ps was selected by adding the timing

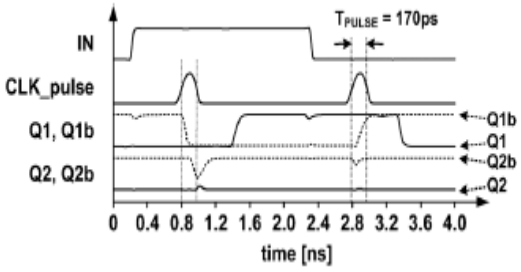
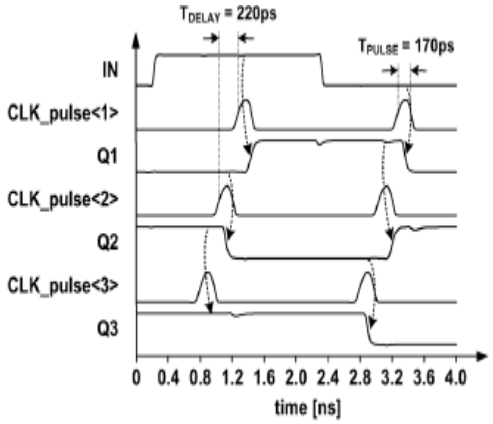


Fig. 9. Simulation waveforms of a shift register with the SSASPLs driven by a pulsed clock signal.



delayed pulsed clock signals. margin to the minimum clock pulse width at the slowest simulation case. Fig. 9 presents the simulation waveforms of a shift register with the SSASPLs driven by the pulsed clock signal in Fig. 2(a).

The output signals of the first latch (Q1 and Q1b) change correctly, because the input signal of the first latch (IN) is constant during the clock pulse width (T_{PULSE}) . On the other hand, the output signals of the second latch (Q2 and Q2b) do not change, because the input signals of the second latch, which are connected to the output signals of the second latch (Q2 and Q2b), change during the clock pulse width. The SSASPL flips the states of the cross-coupled inverters (Q and Qb) by pulling current down through either M_2 or M_3 or during the clock pulse width. The clock pulse width is selected as the minimum time to flip the output signals of the latch (Q and Qb) when its input signals (D and Db) are constant. If the input signals change during the clock pulse width, the time pulling current down through either M_2 or M_3 or becomes shorter than the clock pulse width, so that the latch has not enough clock pulse time to flip the output signals after the input signals change.

Fig. 10 shows the simulation waveforms of a shift register with the SSASPLs driven by the delayed pulsed clock signals. This example has three shift registers (Q1–Q3) and three delayed pulsed clock signals (CLK_pulse□ 1:3□). The pulsed clock delay (T_{PULSE}) is 220 ps by adding the pulse interval of 50 ps between clock pulses to the clock pulse width of 170 ps. The sequence of the pulsed clock signals is in the opposite order of the latches. Each latch has a constant input during its clock pulse so there is no timing problem. Fig. 11 shows the simulated waveforms of the proposed 256-bit shift register with at $K = 4$ at $f_{CLK} = 500$ MHz. . The first 4-bit sub shifter register consisting of five latches (Q1–Q4 and T1) performs the shift operations correctly with five pulsed clock signals (CLK_pulse□ 1:4□ □ and CLK_pulse□ T□). The second 4bit sub shifter register consisting of five latches

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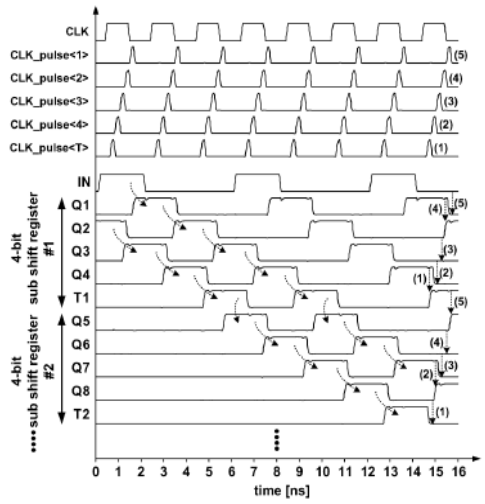

Fig. 11. Simulated waveforms of the proposed 256-bit shift register with at .

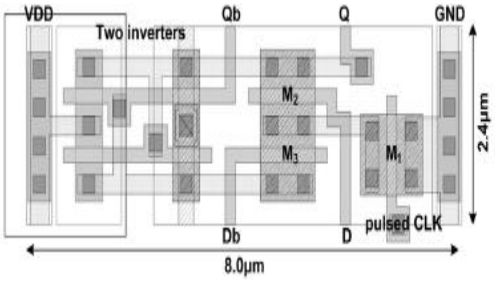

Fig. 12. Layout of the SSASPL.

(Q5–Q8 and T2) receives data from the latch T1 in the first sub shift register and performs the shift operations correctly. The numbers (1)–(5) in Fig. 11 mean the data transition sequence of the latches driven by the sequential pulsed clock signals. Fig. 12 shows the layout of the SSASPL. Its area is $19.2\ \mu\text{m}$. . The SSASPL consumes $3.3\ \mu\text{W}$ at $f_{CLK} = 100\ \text{MHz}$. The power is consumed in the clock loading and data path of the latch. The clock loading of an NMOS transistorm (M_1) consumes $0.73\ \mu\text{W}$. . The data path consumes $2.57\ \mu\text{W}$ when the data transition ratio is 0.5 and the output loading of the latch is only two NMOS transistors M_2 or M_3 (and) of the next latch in the shift register. Each clock pulse circuit occupies $49.5\ \mu\text{m}$ and consumes $27.6\ \mu\text{W}$ at $f_{CLK} = 100\ \text{MHz}$. The word length of the sub shift register K in a 256-bit shift register $(N = 256)$ is selected by considering the area, power, speed. When considering the area optimization, the clock-pulse circuit without the clock buffer is 2.58 times larger than a latch $(\alpha = 2.58)$. The optimal K is 8 which is a divisor of $N(= 256)$ nearest to $9.96(= \sqrt{N/\alpha} = \sqrt{256/2.58})$. When considering the power optimization, the clock-pulse circuit consumes 8.35 times larger power than a latch $(\alpha = 8.35)$. The optimal K is 4 which is a divisor of $N(= 256)$ nearest to $5.54(= \sqrt{N/\alpha} = \sqrt{256/8.35})$.

When considering the speed, the maximum clock frequency is limited to the minimum clock cycle time $(T_{CLK\_MIN} = T_{CP} + K \times T_{DELAY} + T_{CQ})$. . In the

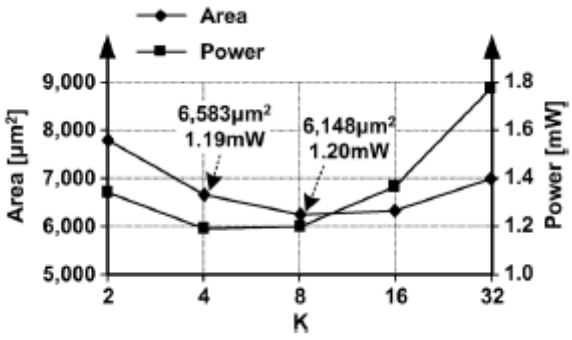

Fig. 13. Area and power consumption of the proposed 256-bit shift register according to K at K at $f_{CLK} = 100\ \text{MHz}$.

Simulation, , , .

$T_{CP} = 180\ \text{ps}, T_{DELAY} = 220\ \text{ps}, T_{CQ} = 130\ \text{ps}.$

When $K = 4$ and $K = 8$, the maximum operating frequencies are 840 MHz and 483 MHz for 5 and 9 pulsed clock delays, respectively. Fig. 13 shows the area and power consumption of the proposed 256-bit shift register according to . When considering both the area and power, the optimal K is 8 but its maximum operating frequency is 483 MHz. In chip fabrication, the 256-bit shift register with $K = 4$ occupies $6600\ \mu\text{m}^2$, consumes 1.19 mW at

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$f_{CLK} = 100$ MHz, $f_{CLK} = 840$ MHz. , operates up to .

C. Performance Comparison

Table I shows the transistor comparison of pulsed latches and flip-flops. The transmission gate pulsed latch (TGPL) [7], hybrid latch flip-flop (HLFF) [8], conditional push-pull pulsed latch (CP3L) [9], Power-PC-style flip-flop (PPCFF) [10], Strong-ARM flip-flop (SAFF) [11], data mapping flip-flop (DMFF) [12], conditional precharge sense-amplifier flip-flop (CPSAFF) [13], conditional capture flip-flop (CCFF) [14], adaptive-coupling flip-flop (ACFF) [15] are compared with the SSASPL [6] used in the proposed shift-register. When counting the total number of transistors in pulsed latches and flip-flops, the transistors for generating the differential clock signals and pulsed clock signals are not included because they are shared in all latches and flip-flops.

The SSASPL uses 7 transistors, which is the smallest number of transistors among the pulsed latches [6]–[9]. The PPCFF uses 16 transistors, which is the smallest number of transistors among the flip-flops [10]–[15]. Two 256-bit area-efficient shift registers using the SSASPL and PPCFF were implemented to show the effectiveness of the proposed shift register. Fig. 14 shows the schematic of the PPCFF, which is a typical master-slave flip-flop composed of two latches. The PPCFF consists of 16 transistors and has 8 transistors driven by clock signals. For a fair comparison, it uses the minimum size of transistors. The sizes of NMOS and PMOS transistors are $0.5\ \mu m/0.18\ \mu m$ and $1\ \mu m/0.18\ \mu m$, respectively. Its layout was drawn compactly by sharing all possible sources and drains of transistors.

All circuits were implemented with a 0.18 μm CMOS process. The powers were measured at $V_{DD} = 1.8$ V and $f_{CLK} = 100$ MHz. . Table II shows the performance comparisons of the PPCFF and SSASPL. The SSASPL is 48.8% smaller and consumes 60.2% less power than the PPCFF.

Table III shows the performance comparisons of the 256-bit shift registers. The conventional shift register using flip-flops was implemented with the PPCFFs. Two types of the proposed shift register using pulsed latches were implemented with the SSASPLs. The proposed shift register achieves a small area and

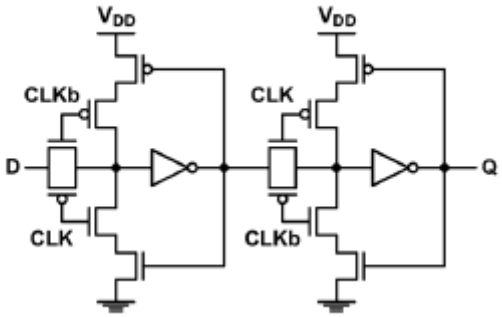

Fig. 14. Schematic of the PPCFF [10].

TABLE I: TRANSISTOR COMPARISON OF PULSED LATCHES AND FLIP-FLOPS

		Total number of transistors	Number of transistors connected to clock
Pulsed latch	**SSASPL [6]**	**7**	**1**
	TGPL [7]	10	4
	HLFF [8]	14	2
	CP3L [9]	26	6
Flip-flip	**PPCFF [10]**	**16**	**8**
	SAFF [11]	18	3
	DMFF [12]	22	5
	CPSA [13]	28	5
	CCFF [14]	28	5
	ACFF [15]	22	4

TABLE II: PERFORMANCE COMPARISONS OF THE PPCFF AND SSASPL

		PPCFF	SSASPL
Type		Flip-flop	Pulsed latch
Number of transistors	Total	16	7
	Clock	8	1
Area		37.5μm² (6.7μm×5.6μm)	19.2μm² (8.0μm×2.4μm) (51.2%)
Power [μW] @f_{CLK}=100MHz	Total	8.29	3.30 (39.8%)
	Data path	3.87	2.57 (66.5%)
	Clock load	4.42	0.73 (16.5%)
Min. clock pulse width [ps]		-	62 @ TT 54-76 @ FF-SS
Clock pulse width (T_{PULSE}) [ps]		-	170
Clock pulse interval [ps]		-	50
Pulsed clock delay (T_{DELAY}) [ps]		-	220
Sizes of transistors (W/L) [μm/μm]		NMOS=0.5/0.18 PMOS=1/0.18	M_1-M_3=1/0.18 NMOS=0.5/1.8 PMOS=0.5/1.8 in inverters

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low power consumption compared to the conventional shift register. The areas of the proposed shift registers with $K = 4$ and $K = 8$ are 63.2% and 59.0%, respectively, compared to that of the conventional shift register. The power consumptions of the proposed shift registers with $K = 4$ and $K = 8$ are 56.3% and 56.5%, respectively, compared to that of the conventional shift register. The total area of N the flip-flops and clock buffer for the N_bit conventional shift register is , where is the total area of $N(1+1/K)$ a flip-flop and a unit clock buffer for driving a flip-flop. The total area of latches and a clock buffer for the N_bit proposed shift register is $N(1+1/K)\times\beta,$, where β is the total area of a latch and a unit clock buffer for driving a latch. The area of $K+1$ clock-pulse γ circuits is $(K+1)\times\gamma,$, where is the area of a clock-pulse circuit. The area ratio of the

TABLE III: PERFORMANCE COMPARISONS OF SHIFT REGISTERS

		Conventional shifter register	Proposed shifter register	
Type		PPCFF (Flip-flop)	SSASPL (Pulsed latch)	
Word length of shift register (N)		256		
Word length of sub shift registers (K)		-	4	8
Total number of flip-flops or pulsed latches		256	320	288
Area [μm^2]	total	10,418	6,583 (63.2%)	6,148 (59.0%)
	Flip-flop or pulsed latch	9,600	6,144	5,530
	Clock buffer	818	192	173
	Clock-pulse	-	248	446
Power [mW] @f_{CLK}= 100MHz	Total	2.123	1.194 (56.3%)	1.199 (56.5%)
	Data path	0.991	0.824	0.741
	Clock load	1.132	0.232	0.210
	Clock-pulse	-	0.138	0.248
Max. Clock frequency		2.8GHz	840MHz	483MHz

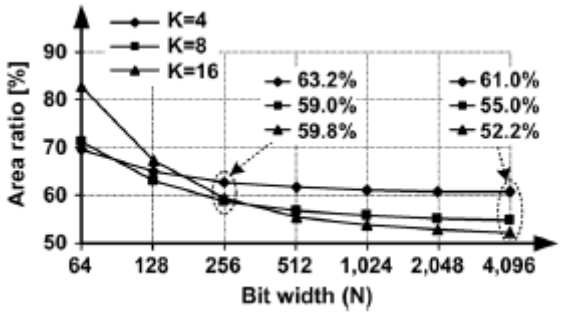

Fig. 15. Area ratio of the proposed shift register to the conventional shift register.

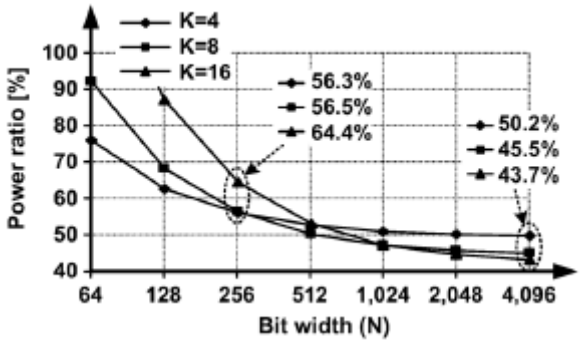

Fig. 16. Power ratio of the proposed shift register to the conventional shift register.

proposed shift register to the conventional shift register can be expressed as

$$\text{Ratio} = \frac{N(1+\frac{1}{K})\times\beta+(K+1)\times\gamma}{N\times\alpha} \qquad (1)$$

$$\text{Ratio} = \frac{\beta}{\alpha}\left(1+\frac{1}{K}\right)+\frac{\gamma}{\alpha}\frac{(K+1)}{N} \qquad (2)$$

As increases, the area ratio is reduced to , as shown in Fig. 15. is 48.7% from the circuit layouts. When and , the area ratio is 52.2%. As N increases, the area ratio is reduced to 51.7% for. When, are the power consumptions instead of the areas, the power ratio of the proposed shift register to the conventional shift register is the same as (2). As increases, the power ratio is reduced to , as shown in Fig. 16.

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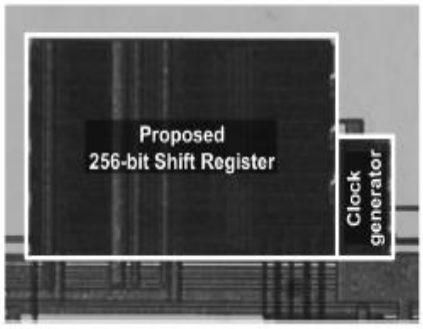

Fig. 17. Chip microphotograph.

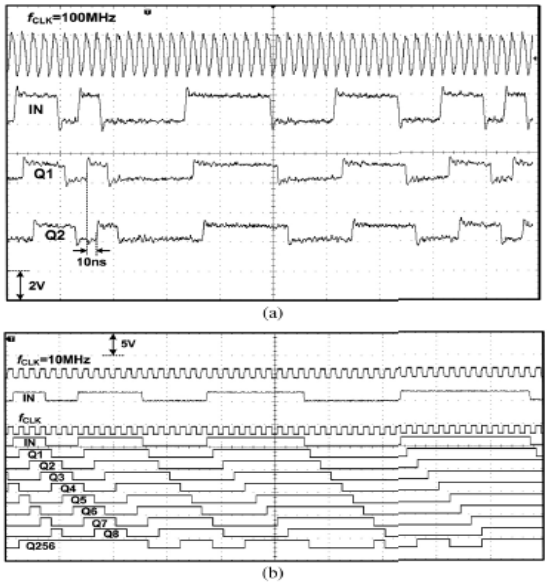

Fig. 18. Measured waveforms of the proposed shift-register at (a) $f_{CLK} = 100$ MHz ; (b) $f_{CLK} = 10$ MHz.

β/α is 39.8% from Table II. When $N = 4096$ and $K = 16$, the power ratio is 43.7%. As increases, the power ratio is reduced to 42.3% for .

III. EXPERIMENTAL RESULTS

The proposed 256-bit shift register with $K = 4$ was fabricated using a $0.18\mu m$ CMOS process. Table IV lists the features of the shift register chip. The chip occupies $6600\ \mu m^2$ and consumes 1.2 mW at $V_{DD} = 1.8$ V and $f_{CLK} = 100$ MHz. . Fig. 17 shows a microphotograph of a chip. Figs. 18(a) and 18(b) show the measured waveforms of the shift-register at $f_{CLK} = 100$ MHz and $f_{CLK} = 10$ MHz, and , respectively. In the simulations, the shift register with $K = 4$ operates up to $f_{CLK} = 840$ MHz, , but in the measurements, the clock frequency was 100 MHz due to the frequency limitation of the experimental equipment. Fig. 18(a) represents a clock signal of 100 MHz, an input signal (IN), two output signals from the first sub shift resister (Q1 and Q2). Fig. 18(b) shows a clock signal of 10 MHz, an input signal (IN), eight output signals

TABLE IV: FEATURES OF THE SHIFT REGISTER CHIP

Type of pulsed latch	SSASPL
Word length of shift register (N)	256
Word length of sub shift registers (K)	4
Total number of pulsed latches	320
Area	6,600μm^2
Power @ f_{CLK}=100MHz	1.2mW
Max. Clock frequency	840MHz @ sim. 100MHz @ meas.

from the first and second sub shift resisters (Q1–Q8), the last output signal of the 256-bit shift register (Q256).

IV. CONCLUSIONS:

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register was fabricated using a 0.18 μm CMOS process with $V_{DD} = 1.8$ V . Its core area is . It consumes 1.2 mW at a 100 MHz clock frequency.

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The proposed shift register saves 37% area $6600\ \mu m^2$. and 44% power compared to the conventional shift register with flip-flops.

REFERENCES:

[1] P. Reyes, P. Reviriego, J. A. Maestro, and O. Ruano, "New protection techniques against SEUs for moving average filters in a radiation environment," IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 957–964, Aug. 2007.

[2] M. Hatamian et al., "Design considerations for gigabit ethernet 1000 base-T twisted pair transceivers," Proc. IEEE Custom Integr. Circuits Conf., pp. 335–342, 1998.

[3] H. Yamasaki and T. Shibata, "A real-time image-feature-extraction and vector-generation vlsi employing arrayed-shift-register architecture," IEEE J. Solid-State Circuits, vol. 42, no. 9, pp. 2046–2053, Sep. 2007.

[4] H.-S. Kim, J.-H. Yang, S.-H. Park, S.-T. Ryu, and G.-H. Cho, "A 10-bit column-driver IC with parasitic-insensitive iterative charge-sharing based capacitor-string interpolation for mobile active-matrix LCDs," IEEE J. Solid-State Circuits, vol. 49, no. 3, pp. 766–782, Mar. 2014.

[5] S.-H. W. Chiang and S. Kleinfelder, "Scaling and design of a 16-megapixel CMOS image sensor for electron microscopy," in Proc. IEEE Nucl. Sci. Symp. Conf. Record (NSS/MIC), 2009, pp. 1249–1256.

[6] S. Heo, R. Krashinsky, and K. Asanovic, "Activity-sensitive flip-flop and latch selection for reduced energy," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 9, pp. 1060–1064, Sep. 2007.

[7] S. Naffziger and G. Hammond, "The implementation of the nextgeneration 64 b itanium microprocessor," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2002, pp. 276–504.

[8] H. Partovi et al., "Flow-through latch and edge-triggered flip-flop hybrid elements," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 138–139, Feb. 1996.

[9] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional push-pull pulsed latch with 726 fJops energy delay product in 65 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2012, pp. 482–483.

[10] V. Stojanovic and V. Oklobdzija, "Comparative analysis of masterslave latches and flip-flops for high-performance and low-power systems," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999. YANG: LOW-POWER AND AREA-EFFICIENT SHIFT REGISTER USING PULSED LATCHES 1571

[11] J. Montanaro et al., "A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor," IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1703–1714, Nov. 1996.

[12] S. Nomura et al., "A 9.7 mW AAC-decoding, 620 mW H.264 720p 60fps decoding, 8-core media processor with embedded forwardbody- biasing and power-gating circuit in 65 nm CMOS technology," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2008, pp. 262–264.

[13] Y. Ueda et al., "6.33 mW MPEG audio decoding on a multimedia processor," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2006, pp. 1636–1637.

[14] B.-S. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, pp. 1263–1271, Aug. 2001.

[15] C. K. Teh, T. Fujita, H. Hara, and M. Hamada, "A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2011, pp. 338–339.